行政院國家科學委員會專題研究計畫 成果報告

後次微米時代新興電子設計自動化技術之研究--子計畫四：應用計算智慧推理處理後深次微米時代電路設計上的可靠度挑戰(3/3)

研究成果報告(完整版)

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報 告 附 件 ： 出席國際會議研究心得報告及發表論文

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中 華 民 國 100 年 10 月 31 日

中文摘要：　在深次微米時代中 CMOS 設計必須要準確地估計電路的統計性的軟性電子錯誤率（SER）。隨著製程變異日漸嚴重，導致軟性電子錯誤的行為有著相當大的不確定性。然而，若考慮製程變異的影響，電壓脈衝寬度在傳遞過程中不再只是像以往被認為的單調遞減。結果顯示，在現今的電子設計中，若以傳統的靜態分析，將會導致嚴重地低估軟性電子錯誤率。

因此，這篇報告提出了三個有效地架構來應對上述之複雜問題。
1)首先，我們利用蒙地卡羅(Monte-Carlo)方法隱性地獲取暫態錯誤之分佈。另外，我們進一步採用準隨機亂數(quasirandom sequences)，成功地解決了蒙地卡羅方法中計算時間冗長的缺點，加快了收斂速度並縮短了運行時間。此外，重要性取樣性(importance sampling)也被加入至此架構當中，以提升計算軟性電子錯誤率之速度。
2)接下來，我們使用支持向量回歸(support-vector-regression)方法精準地建構出製程變異下軟性電子錯誤率行為之模型。然而，支持向量回歸方法也有著建構模型時間以及找尋參數之問題存在，在此架構中，我們也提出二個方法來解決這些問題。
3)第三個方法為閉合形式的分析(closed-form analysis)架構，此架構可以克服準確性及效率之間的權衡問題。此閉合形式的分析架構是利用類似統計靜態時序分析(SSTA)之方法來分析軟性電子錯誤率。此架構底下，可提供精準地一階閉合形式模型，以預測軟性電子錯誤率之行為。

實驗結果證明，所提出之三種方法在 ISCAS85 電路的驗證下，與蒙地卡羅電路模擬相比可以達到平均 107 倍的加速，而只有 2%的誤差。

英文摘要：　CMOS designs in the deep submicron era require statistical methods essential to accurately estimate the circuit soft error rate (SER). However, process variation increases the complexity of statistical characteristics related to transient faults, leading to considerable uncertainty in the behavior of soft errors. Considering the impact of process variations, voltage pulse widths of transient faults are found no longer monotonically diminishing after propagations, as they were formerly considered. As a result, the soft error rates in scaled electronic designs escape from traditional static analysis and are seriously underestimated.

In this report, we formulate the statistical soft error rate (SSER) problem and present three frameworks to cope with the aforementioned sophisticated issues.
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fault distributions implicitly using a Monte-Carlo approach. We further employ a heuristic to customize the use of quasirandom sequences, which successfully speeds up the convergence of simulation error and hence shortens the runtime. Moreover, advanced sampling techniques are also incorporated for variance reduction of SSERs.
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行政院國家科學委員會補助專題研究計畫■ 成 果 報 告
□ 期中進度報告

應用計算智慧推理處理後深次微米時代電路設計上的可靠度挑戰

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林玗璇 林昱澤 許凱華

成果報告類型(依經費核定清單規定繳交)：□精簡報告 ■完整報告

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執行單位：國立交通大學電機工程學系/電信工程研究所
中 華 民 國 100 年 10 月 31 日

摘 要

在深次微米時代中 CMOS 設計必須要準確地估計電路的統計性的軟性電子錯誤率(SER)。隨著製程變異日漸嚴重，導致軟性電子錯誤的行為有著相當大的不確定性。然而，若考慮製程變異的影響，電壓脈衝寬度在傳遞過程中不再只是像以往被認為的單調遞減。結果顯示，在現今的電子設計中，若以傳統的靜態分析，將會導致嚴重地低估軟性電子錯誤率。

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關鍵字：*軟性電子錯誤率 ; 製程變異 ;* 支持向量回歸; 蒙地卡羅; *統計靜態時序分析*

Abstract

CMOS designs in the deep submicron era require statistical methods essential to accurately estimate the circuit soft error rate (SER). However, process variation increases the complexity of statistical characteristics related to transient faults, leading to considerable uncertainty in the behavior of soft errors. Considering the impact of process variations, voltage pulse widths of transient faults are found no longer monotonically diminishing after propagations, as they were formerly considered. As a result, the soft error rates in scaled electronic designs escape from traditional static analysis and are seriously underestimated.

In this report, we formulate the statistical soft error rate (SSER) problem and present three frameworks to cope with the aforementioned sophisticated issues.

1) The table-lookup framework captures the change of transient-fault distributions implicitly using a Monte-Carlo approach. We further employ a heuristic to customize the use of quasirandom sequences, which successfully speeds up the convergence of simulation error and hence shortens the runtime. Moreover, advanced sampling techniques are also incorporated for variance reduction of SSERs.

2) The support-vector-regression framework is applied to tackle the complexity of these natures and build compact yet accurate generation and propagation models for transient fault distributions. Moreover, we also apply two intensified methods to solve the disadvantage of support-vector-regression.

3) The closed-form analysis framework to overcome the trade-off between accuracy and efficiency problem. This framework presents accurate cell models in first-order closed-form, thereby enabling the analysis of SSERs in a block-based fashion similar to statistical static timing analysis (SSTA). These cell models are derived as a closed form in the proposed framework and remain precise under the assumption of a normal distribution for the process parameters.

Experimental results show that the proposed framework increases the SER computation speed by 10^7X, with only 2% accuracy loss compared to the Monte-Carlo SPICE simulation.

Keyword: soft error, process variation, SVM, Monte Carlo, SSTA

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Chapter 1
Introduction

Soft errors have emerged to be the dominant failure mechanism for reliability in modern CMOS technologies. Soft errors result from radiation-induced transient faults latched by memory elements and used to be of concern only for memory units but now becomes commonplace for logic units beyond deep sub-micron technologies. As predicted in [1][2][3], the soft error rate in combinational logic will be comparable to that of unprotected memory cells in 2011. Therefore, numerous studies have been dedicated to modeling of transient faults [4][5][6][7], propagation and simulation/estimation of soft error rates [8][9][10][11] and circuit hardening techniques including detection and protection [12][13][14][15].

Three masking mechanisms shown in Figure 1.1 are indicated by [1] as the key factors to determine if one transient fault can be latched by the memory elements to become a soft error. Logical masking occurs when the input value of one gate blocks the propagation of the transient fault under a specific input pattern. One transient fault attenuated by electrical masking may disappear due to the electrical properties of the gates. Timing masking represents the situation that the transient fault propagates to the input of one memory element outside the window of its clock transition.

Numerous previous works such as [6][16] propagate transient faults through one gate according to the logic function and in the meantime use analytical models to evaluate the electrical change of transient faults. A refined model is presented in [7] to incorporate non-linear transistor current, which is further applied to different gates with different charges deposited. A static analysis is also proposed in [17] for timing masking by computing backwards the propagation of the error-latching windows efficiently.

Moreover, in recent years, circuit reliability in terms of soft error rate (SER) has been extensively investigated. SERA [8] computes SER by means of a waveform model to consider the electrical attenuation effect and error-latching probability while ignoring logical masking. Whereas FASER [9] and MARS-C [18] apply symbolic

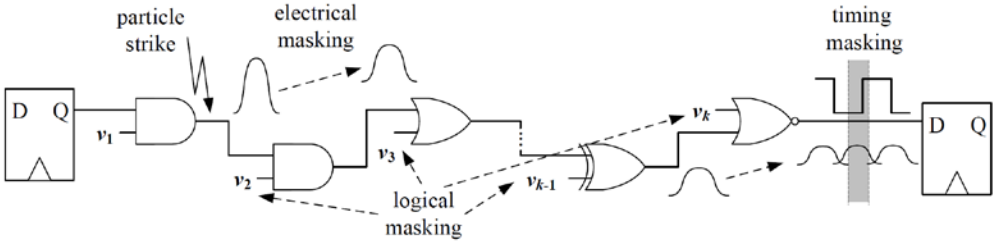


Figure 1.1: Three masking mechanisms for soft errors

techniques to logical and electrical maskings and scale the error probability according to the specified clock period, AnSER [17] applies signature observability and latching-window computation for logical and timing maskings to approximate SER for circuit hardening. SEAT-LA [10] and the algorithm in [11] simultaneously characterize cells, flip-flops and propagation of transient faults by waveform models and result in good SER estimate when comparing to SPICE simulation. However, all of these techniques are deterministic and may not be capable of explaining more sophisticated circuit behaviors due to the growing process variations beyond deep sub-micron era.

Process variations including various manufacturing defects have grown to be one of the major challenges to scaled CMOS designs [19][20]. From [20][21], 25%-30% different on chip frequency are observed. For design reliability, 15%-40% SER variations are reported in [22] under the 70nm technology. Also, authors in [23] proposed a symbolic approach to propagate transient faults considering process variations.

Using the 45nm Predictive Technology Model (PTM) [24], the impact of process variations on circuit reliability is illustrated in Figure 1.2, where SERs are computed by SPICE simulation on a sample circuit c17 from ISCAS 85 under different values (σ_{proc}'s) of process variation applied to perturbing separately the gate width and channel length of each transistor in each cell's geometry. The X-axis and Y-axis denote σ_{proc} and SER, respectively, where FIT (Failure-In-Time) is defined by the number of failures per 10^9 hours. Nominal settings without variation are used in static SPICE simulation, whereas Monte-Carlo SPICE simulations are used to approximate process-variation impacts under different σ_{proc}'s.

As a result, SER from static SPICE simulation is underestimated. Considering different σ_{proc}'s in Monte-Carlo SPICE simulation, all SERs are higher than that from static SPICE simulation. As process variations deteriorate, the discrepancy between

Monte-Carlo and static SERs further enlarges. In Figure 2, (SERmonte –SERstatic)/SERstatic under σ_{proc} = 1%, 2%, 5% and 10% are 6%, 19%, 46% and 117%, respectively. Such result suggests that the impact of process variations to SER analysis may no longer be ignored in scaled CMOS designs.

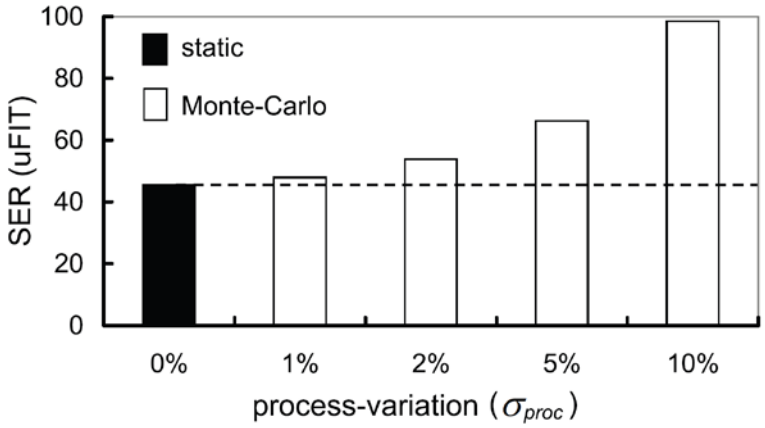


Figure 1.2: SER discrepancies between static and Monte-Carlo SPICE simulation w.r.t. process-variation

1.1 Research goal

In this project, we formulate the statistical soft error rate (SSER) problem and present three frameworks to cope with the aforementioned sophisticated issues. We first review statistical soft error rate analysis based on which a Monte-Carlo framework is built. We further employ the quasi-random sequences, which successfully speeds up the convergence of simulation error and shortens the runtime. Moreover, advanced sampling techniques are incorporated for variance reduction of SSERs. Then, SVR-learning framework captures the change of transient-fault distributions explicitly using statistical learning theory. Regardless of the methods used, current statistical SER (SSER) frameworks invariably involve a trade-off between accuracy and efficiency. Third framework presents accurate cell models in first-order closed-form to overcome this problem, thereby enabling the analysis of SSERs in a block-based fashion similar to statistical static timing analysis (SSTA).

1.2 Research method

1.2.1 First year

The first framework combines the current static approaches with the

Monte-Carlo (MC) method, a computational algorithm using repeated random samplings to portray complex statistical behaviors of physical or mathematical systems as depicted in Figure 1.3. This framework maps to the three masking mechanism using three loops: the outmost loop considers various levels of collection charge; the second loop accounts for all vulnerable nodes within a circuit; the innermost loop computes δ_{strike} and δ_{prop} implicitly. As the key component of the framework, the last loop can be further decomposed into two parts: (1) cell pre-characterization and (2) sampling and renewal of transient faults.

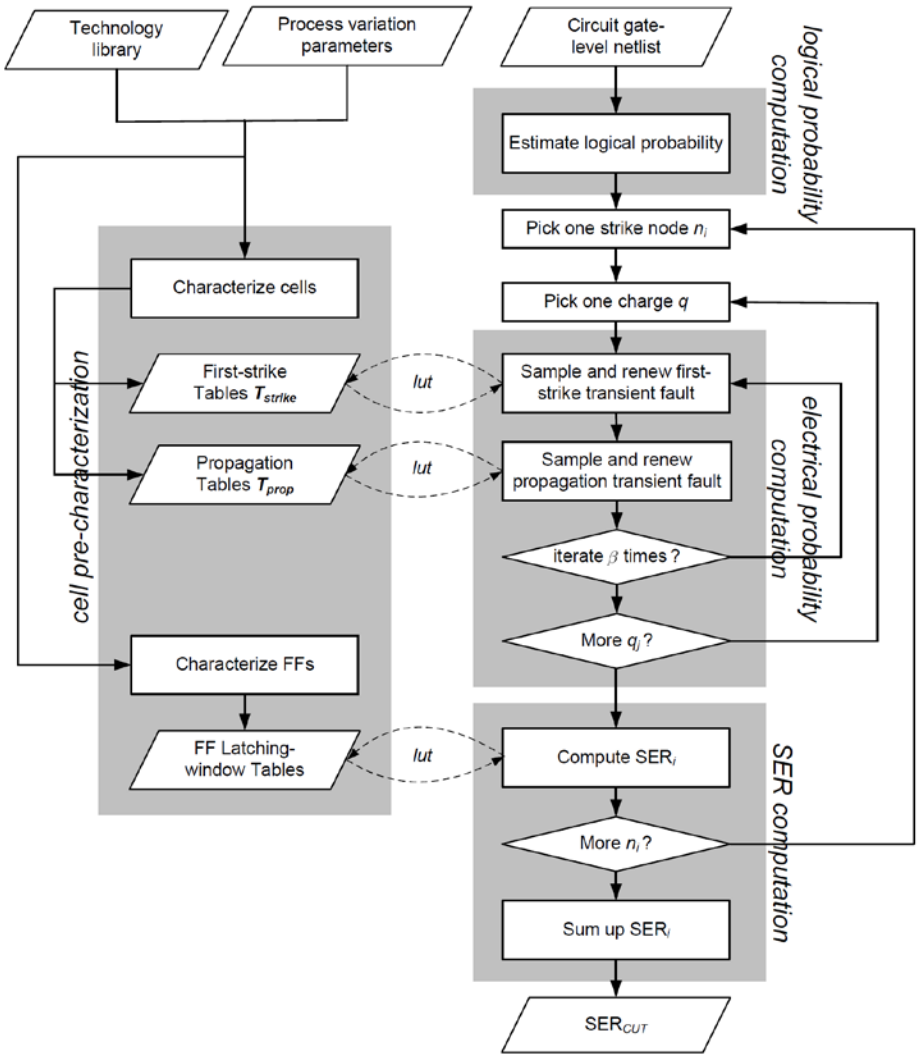


Figure 1.3: Proposed table-lookup framework

Furthermore, we customize the use of quasi-random sequences, which successfully speed up the convergence of simulation error and hence shorten runtime. However, there is still a problem about the uniformity of the quasi-sequence samples in multivariate distribution. To solve this problem, we use importance sampling to

reduce variance in quasi-sequence samples. From experimental results, the framework is capable of yielding more accurate SSER results compared to previous works and running much faster.

1.2.2 Second year

Integrating the impact of process variations, four models are traditionally built using lookup tables. However, lookup tables have two limitations on applicability: (1) inaccurate interpolation and (2) coarse model-size control. First, lookup tables can take only finite table indices and must use interpolation. However, interpolation functions are often not accurate enough or difficult to obtain, especially as the table dimensionality grows. Second, a lookup table stores data samples in a grid-like fashion, where the table will grow prohibitively large for fine resolution. Meanwhile, the information richness often differs across different parts of a table. For example, we observe that pulse widths generated by strong charges behave much simpler than weaker charges do. Naturally, simple behaviors can be encoded with fewer data points in the model, whereas complicated behaviors need to be encoded with more.

In this year, we proposed another learning-based framework to computes δ_{strike} and δ_{prop} directly with support of support vector regression (SVR) and is found to be both more efficient and more accurate than table look-up method. Note that our SVR-learning framework can be represented in the same flowchart as Figure 1.3 with the replacement of first-strike tables (T_{strike}) and propagation tables (T_{prop}) with respective learning models (δ_{strike} and δ_{prop}).

1.2.3 Third year

In this year, we proposed a novel approach, similar to that of block-based SSTA, for SSER in which a transient fault is decomposed into two transitions for analysis: a rising edge and a falling edge. Each edge is processed using an analytical approach and statistical static timing analysis, which is based on a first-order closed-form. Because the transient fault is analyzed using a mathematical method, the timing cost can be largely reduced and timing information can be preserved, which is helpful for describing the interactive behavior of transient faults. However, correlations are the main concern when applying a closed-form block-based approach to the estimation of SSER. Theoretically, all correlations between transition signals and corresponding gate delays must be considered; however, the correlation between transition signals can be overlooked because the difference in SER has been shown to be less than 1%

according to our experiments. Thus, we devised a parameterized SSTA framework that takes into account the timing correlation to derive more accurate SER. Experimental results demonstrate that our approach can provide reasonable results much more rapidly than all previous works.

Chapter 2
Fundamental of Statistical Soft Error Rate

2.1 Transient-fault behavior in very deep submicron era

Transient faults exhibit two characteristics in the very deep sub-micron era. One makes the faults more unpredictable whereas the other causes the discrepancy in Figure 1.2. In this section, the discrepancy are explained and associated with the electrical and timing masking mechanisms, respectively

2.1.1 To be electrically better or worse?

The first observation is conducted by running static SPICE simulation on a path consisting of various gates (including 2 AND, 2 OR and 4 NOT gates) in the 45nm PTM technology. As shown in Figure 2.1, the radiation particle first strikes the output of the first NOT gate with a collection charge of 32fC, and then propagates the transient fault along other gates with all side-inputs being set properly. The pulse widths (pw_i's) in voltage of the transient fault starting at the struck node and after passing gates along the path in order are 171ps, 183ps, 182ps, 177ps, 178ps, 169ps, 166ps and 173ps, respectively. Each pw_i and pw_{i+1} can be compared to show the changes of voltage pulse widths during propagation in Figure 2.1.

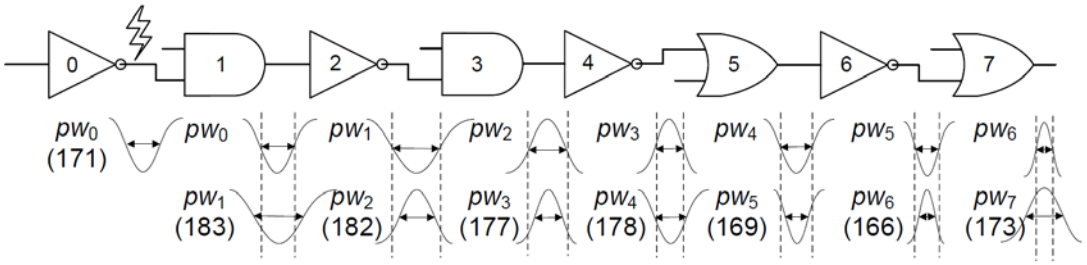


Figure 2.1: Static SPICE simulation of a path in the 45nm technology

As we can see, the voltage pulse widths of such transient fault grow larger through gate #1, #4, and #7 while gate #2, #3, #5 and #6 attenuate such transient fault. Furthermore, gates of the same type behave differently when receiving different voltage pulses. To take AND-type gates for example, the output pw_1 is larger than the input pw_0 on gate #1 while the contrary situation ($pw_3 < pw_2$) occurs on gate #3. This

result suggests that the voltage pulse width of a transient fault is not always diminishing, which contradicts some assumptions made in traditional static analysis [10]. A similar phenomenon called Propagation Induced Pulse Broadening (PIPB) is discovered in [25] and states that the voltage pulse width of a transient fault widens as it propagates along the long inverter chain.

2.1.2 When error-latching probability meets process variations

The second observation is dedicated to the timing-masking effect under process variations. In [9][18], the error-latching probability (PL) for one flip-flop is defined as

$$\mathrm{PL} = \frac{\mathrm{pw}-\mathrm{w}}{\mathrm{t_{clk}}} \tag{1}$$

where pw, w and t_{clk} denote the pulse width of the arrival transient fault, the latching window of the flip-flop, and the clock period, respectively. However, process variations make pw and w become random variables. Therefore, we need to redefine Equation (1) as following.

Definition ($P_{err-latch}$, **error-latching probability**)

Assume that the pulse width of one arrival transient fault and the latching window (t_{setup}+t_{hold}) of the flip-flop are random variables and denoted as pw and w, respectively. Let x = pw − w be another random variable and μ_x and σ_x be its mean and variance. The latch probability is defined as:

$$\mathrm{P_{err-latch}(pw, w)} = \frac{1}{\mathrm{t_{clk}}} \int_0^{\mathrm{u_x}+3\sigma_x} \mathrm{x} \cdot \mathrm{P(x > 0)} \cdot dx \tag{2}$$

With the above definition, we further illustrate the impact of process variations on SER analysis. Figure 4(a) shows three transient-fault distributions with the same pulse-width mean (95ps) under different σ_{proc}'s: 1%, 5% and 10%. A fixed latching window w = 100ps is assumed as indicated by the solid lines. According to Equation (1), static analysis result in zero SER under all σ_{proc}'s because 95 − 100 < 0.

From a statistical perspective, however, these transient faults all yield positive and different SER's. It is illustrated using two terms: P(x > 0) and x in Equation (2). First, in Figure 2.2(a), the cumulative probabilities for pw > w under three different σ_{proc}'s are 17%, 40%, and 49%, respectively. The largest σ_{proc} corresponds to the

largest P(x > 0) term. Second, in Figure 2.2(b), we compute the pulse-width averages for the portion x = pw − w > 0 and they are 1, 13 and 26, respectively. Again, the largest σ_{proc} corresponds to the largest x term.

These two effects jointly suggest that larger σ_{proc} leads to larger $P_{err-latch}$, which has been neglected in traditional static analysis, and also explain the increasing discrepancy shown in Figure 1.2. In summary, process variations make traditional static analysis no longer effective and should be considered in accurate SER estimation for scaled CMOS designs.

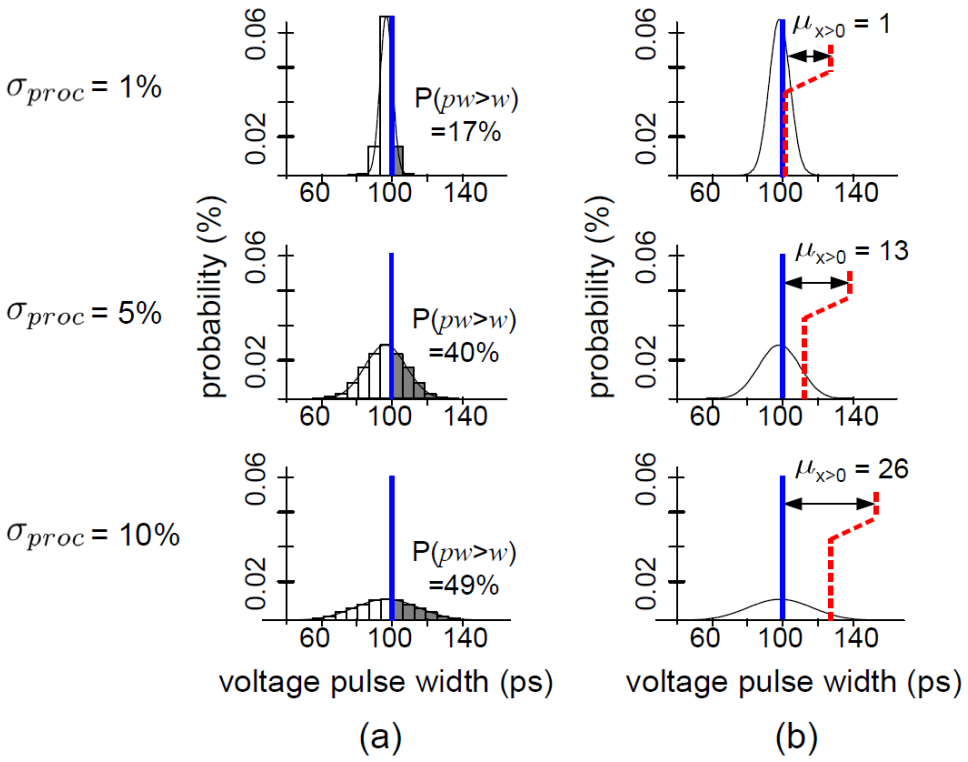


Figure 2.2: Process-variation vs. error-latching probabilities

2.2 Impact of spatial correlation

Variations have become important as technology scales further. High levels of device parameter variations are changing the design flows from deterministic to probabilistic as technology nodes beyond 90nm experience increasingly. Process variations can be classified into the two categories. One is the inter-die variations and the other is intra-die variations. Intra-die variations can significantly affect the variability of performance parameters on a chip due to the modern technologies are rapidly and steadily growing. Intra-die variations are locally layout-dependent, and

therefore it is spatially correlated.

Devices tend to have similar characteristics as it with similar layout patterns and proximity structures. In other words, it is globally location-dependent. Devices have the similar characteristics than placed far away as it located close to each other. With increased process scaling, intra-die variations are becoming a more dominant portion of the overall variability of device features, meaning that devices on the same die can no longer be treated as identical copies of the same device.

If we do not take into account the value of process variations, it will lead to underestimated/overoptimistic estimation on SSER. However, all previous works consider the impact of process variations but do not include spatial correlations in the statistical soft error rate, leading to incorrect SSERs. Therefore, we investigate the impact of spatial correlations in our project to comprehend the accuracy of SSERs as shown in Figure 2.3.

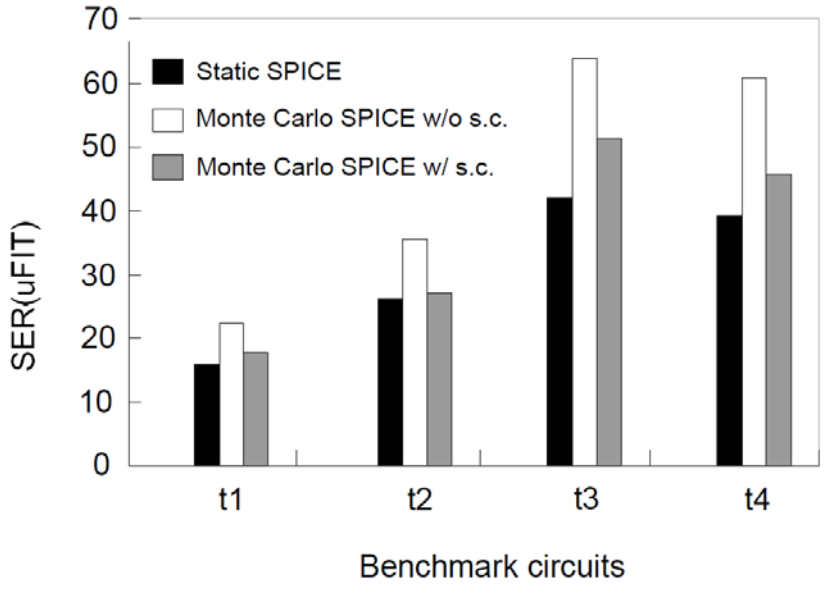


Figure 2.3: SSER comparison from static and Monte Carlo SPICE simulations, the proposed MC with spatial correlations and without spatial correlations frameworks

According to Figure 2.3, circuit SER is overestimated under the process variation 5% without considering spatial correlations. Circuit SER that considers spatial correlations under the process variation 5% is generally lower when comparing with the circuit SER under the process variation 5% without considering spatial correlations. Therefore, we propose an effective model considering spatial correlations of statistical soft error rate. The analysis is extended to include spatial

correlations. Then we explain the model used for process variations and spatial correlations of intra-die variations.

There are a few models in order to handle parameter correlations. First, we introduce the ***grid*** model. ***Grid*** model is a die area divided by a square grid. A group of fully correlated devices is assumed to correspond to each square of the grid. Each square is modeled as a random variable (RV) which correlates with the random variables corresponding to the rest of the squares. Another one model is called the ***quadtree*** model. This method is recursively dividing the die area into four squares until individual gates into the grid. The partitions are stacked on top of another level. We then assign each of them an independent random variable. By summing all areas that cover this particular device, the random variable corresponding to the gate is computed. Due to share common random variables on higher levels, the spatial correlations can be addressed properly.

Without losing the generality, in the beginning of our project, we used the grid model to apply spatial correlations to soft error. We partitioned the region of die into $n_{row}*n_{col} = n^2$ grids for modeling the intra-die spatial correlations of parameters. We assumed that perfect correlations among the devices are in the same grid. Low or zero correlations are between far-away grids, and high correlations between close grids. The devices are more likely to have more similar characteristics than those placed far away due to they are close to each other. For example, Figure 2.4 shows that gate *a* in grid (1, 1) and gate *e* in grid (3, 3). Since they are far away from each other, we assume that their parameters are uncorrelated. Gate *c* in grid (1, 2), gate *a* and gate *c* lie in neighboring grids, and due to their spatial proximity, their parameter variations are not identical but should be highly correlated. Since gate *a* and gate *b* are located in the same grid, we assume that the variations of their gate length are identical.

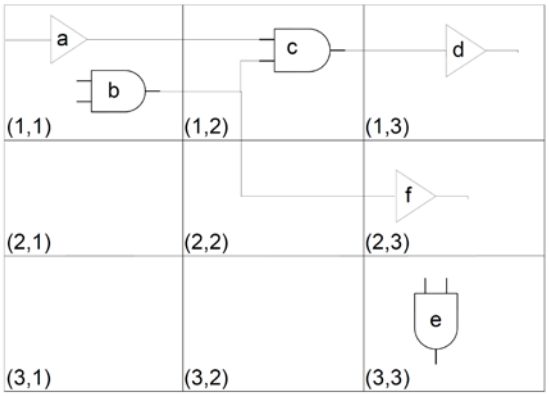


Figure 2.4: The gates in different grid with different process variations

Our algorithm makes a second assumption. Assume that there are no correlations between different types of process parameters, and nonzero correlations may exist only among the same type of process parameters in different grids. For instance, the L_g values for transistors in nearby grids are correlated, but the other parameters such as W_g or W_{int} in any grid are uncorrelated. In other words, we assume that interconnect parameters in different layers to be different types of parameters.

2.3 Full-spectrum analysis or not

Some previous works simplify the SER estimation by injecting only four levels of electrical charges. Therefore, our project poses a simple, yet important question, *"Are four levels of electrical charges enough to converge SER correctly and properly address the process-variation effect?"*

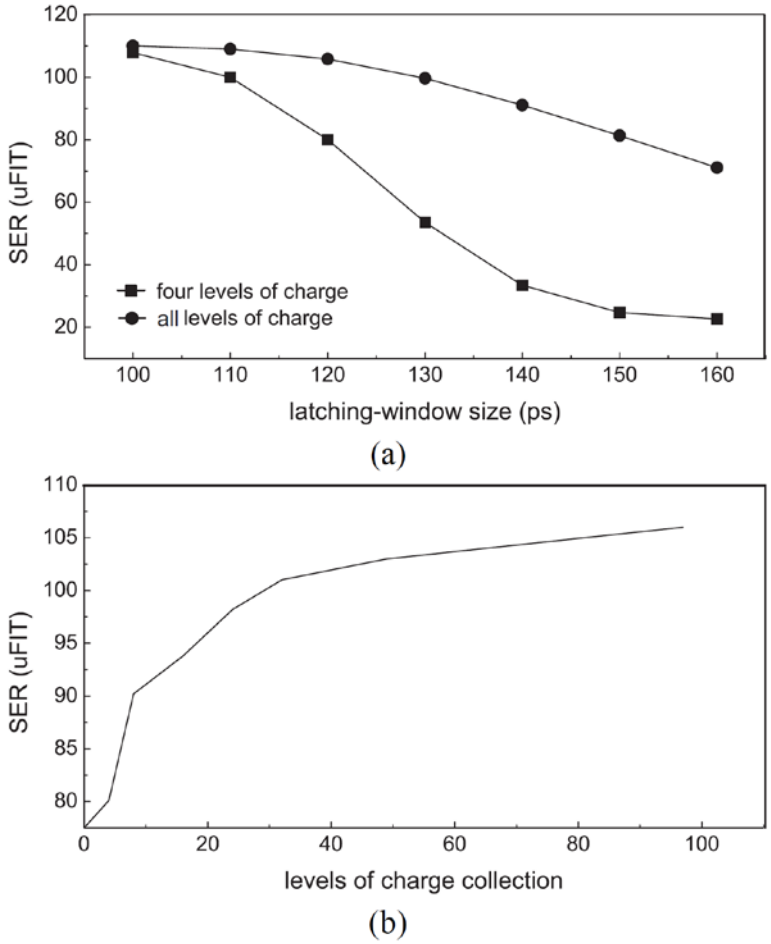


Figure 2.5: (a) SERs of four-level and full-spectrum charge collection w.r.t. different latching-window size (b) SERs w.r.t. different levels of charge collection

Figure 2.5(a) compares of SERs from Monte-Carlo SPICE simulations. These SERs had different levels of charges when collected onto a sample circuit (c17 from ISCAS'85) with different latching-window sizes. The line with square symbols and the line with circle symbols represent the SERs induced by four-level and full-spectrum charge collection, respectively. As the latching-window size was set to 100ps, the SERs obtained from four-level and full-spectrum analyses were the same. However, as the latching-window size grew to 150ps, the effective range of charge collection for SSER analysis increased from 35fC to 132fC. Therefore, the SER difference between four-level and full-spectrum analyses grew to 69%. Another question naturally arises, *"If four levels of charge collection are not sufficient to derive accurate SERs, how many levels are sufficient?"*

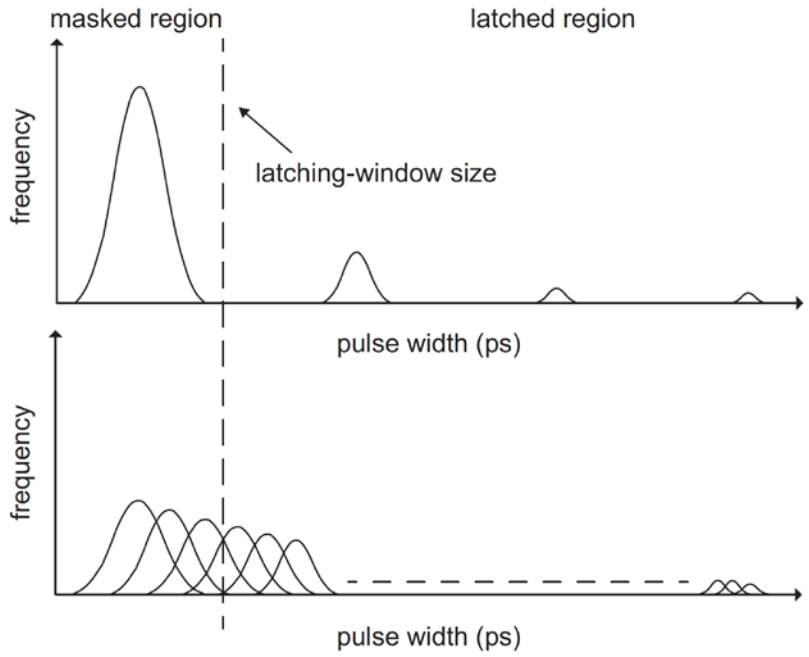


Figure 2.6: Transient-fault distributions induced by four-level and full-spectrum charge collection

Figure 2.5(b) suggests the answer. All levels of deposited charges should be considered because SERs increase with charge collections. SER difference using different levels of deposited charges is further illustrated (Fig. 2.6), where the upper and lower parts show SER estimation by only four levels of charges and by all levels of charges, respectively. The X-axis and Y-axis denote the pulse width of transient faults and the effective frequency for a particle strike of different levels of deposited charges. For the analysis using four-level deposited charges, only four transient-fault (TF) distributions were generated and could contribute to the final soft error rate. In other words, soft errors can only be generated from four concentrated distributions,

and therefore may result in mistakes on SER integration. As the latching-window size of one flip-flop was far from the first TF distribution, soft errors from such TF distributions were entirely masked due to the timing-masking effect. For example, the biggest pulse width distribution in the upper part of Figure 2.6 is excluded from SER estimation. But, only part of them (those smaller decomposed TF distributions) were masked during analysis using all levels of deposited charges (Figure 2.6, lower part). As a result, SER estimation was no longer valid with analysis using only four levels of charges and instead should comprehensively consider full-spectrum charge collection.

2.4 Problem formulation of statistical soft error rate (SSER)

In this section, we formulate the statistical soft error rate (SSER) problem for general cell-based circuit designs. Figure 2.7 illustrates a sample circuit subject to process variations, where the geometries of each cell vary [21]. Once high-energy particles strike the diffusion regions of these variable-size cells, according to Figure 1.2, 2.1 and 2.2, the electrical performances of the resulting transient faults also vary a lot. Accordingly, to accurately analyze the soft error rate (SER) of a circuit, we need to integrate both process-variation impacts and three masking affects discussed in Chapter 1 simultaneously, which brings up the statistical soft error rate (SSER) problem.

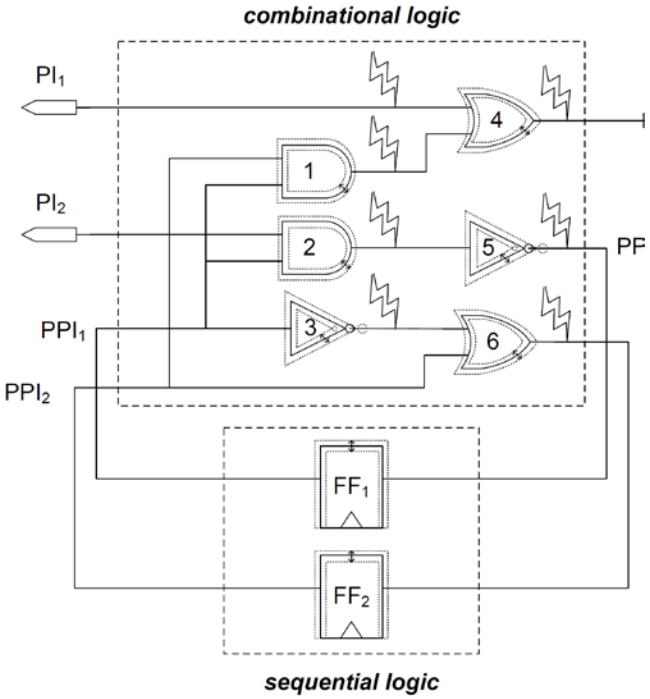


Figure 2.7: An example for illustrating the SSER problem

The SSER problem is composed of three elements: (1) electrical-probability computation, (2) propagation-probability computation and (3) overall SER estimation. A bottom-up mathematical explanation of the SSER problem will start reversely from overall SER estimation to electrical probability computation.

2.4.1 Overall SER estimation

The overall SER for the circuit under test (CUT) can be computed by summing up the SER's of each individual node in the circuit. That is,

$$SER_{CUT} = \sum_{i=0}^{N_{node}} SER_i \tag{3}$$

where N_{node} denotes the total number of possible nodes to be struck by radiation particles in the CUT and SER_i denotes the SER results from node i, respectively.

Each SER_i can be further formulated by integrating over the range q = 0 to Qmax (the maximum collection charge from the environment) the products of particle-hit rate and the total number of soft errors that q can induce at node i. Therefore,

$$SER_i = \int_{q=0}^{Q_{max}} (R_i(q) \times F_{soft-err}(i, q)) dq \tag{4}$$

In a circuit, $F_{soft-err}(i, q)$ represents the total number of expected soft errors from each flip-flop that a transient fault from node i can propagate to. $R_i(q)$ represents the effective frequency for a particle hit of charge q at node i in unit time according to [1][8]. That is,

$$R_i(q) = F \times K \times A_i \times \frac{1}{Q_s} e^{\frac{-q}{Q_s}} \tag{5}$$

where F, K, A_i and Q_s denote the neutron flux (> 10MeV), a technology-independent fitting parameter, the susceptible area of node i in cm^2, and the charge collection slope, respectively.

2.4.2 Logical probability computation

$F_{soft-err}(i, q)$ depends on all three masking effects and can be decomposed into

$$F_{soft-err}(i, q) = \sum_{j=0}^{N_{ff}} P_{logic}(i, j) \times P_{elec}(i, j, q) \quad (6)$$

where N_{ff} denotes the total number of flip-flops in the circuit under test. $P_{logic}(i, j)$ denotes the overall logical probability of successfully generating a transient fault and propagating it through all gates along the path from node i to flip-flop j. It can be computed by multiplying the signal probabilities for specific values on target gates as follows.

$$P_{logic}(i, j) = P_{sig}(i = 0) \times \prod_{k \in i \to j} P_{side}(k) \quad (7)$$

where k denotes one gate along the target path (i→j) starting from node i and ending at flip-flop j, P_{sig} denotes the signal probability for the designated logic value, and P_{side} denotes the signal probability for the non-controlling values (i.e. 1 for AND gates and 0 for OR gates) on all side inputs along the target path.

Figure 2.8 illustrates an example where a particle striking net a results in a transient fault that propagates through net c and net e. Suppose that the signal probability of being 1 and 0 on one arbitrary net i is P_i and $(1-P_i)$, respectively. In order to propagate the transient fault from a towards e successfully, net a needs to be 0 while net b, the side input of a, and net d, the side input of c, need to be non-controlling, simultaneously.

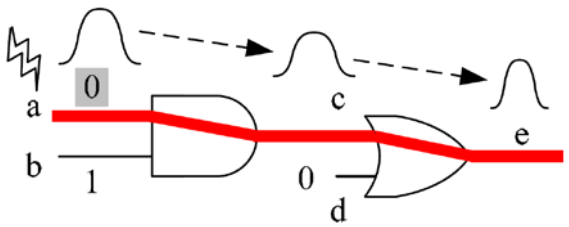


Figure 2.8: Logical probability computation for one sample path

Therefore, according to Equation (7),

$$\begin{aligned} P_{logic}(a, e) &= P_{sig}(a = 0) \times P_{side}(a) \times P_{side}(c) \\ &= P_{sig}(a = 0) \times P_{sig}(b = 1) \times P_{sig}(d = 0) \\ &= (1 - P_a) \times P_b \times (1 - P_d) \end{aligned}$$

2.4.3 Electrical probability computation

Electrical probability $P_{elec}(i, j, q)$ comprises the electrical and timing masking effects and can be further defined as

$$\begin{aligned} P_{elec}(\mathrm{i,j,q}) &= \mathrm{P_{err-latch}}\left(\mathrm{pw_j}, \mathrm{w_j}\right) \\ &= \mathrm{P_{err-latch}}\left(\lambda_{\mathrm{elec-mask}}(\mathrm{i,j,q}), \mathrm{w_j}\right) \end{aligned} \tag{8}$$

While $P_{err-latch}$ accounts for the timing making effect as defined in Equation (2), $\lambda_{elec-mask}$ accounts for the electrical masking effect with the following definition.

Definition ($\lambda_{elec-mask}$, **electrical masking function**)
Given the node i where the particle strikes to cause a transient fault and flip-flop j is the destination that the transient fault finally ends at, assume that the transient fault propagates along one path (i ; j) through v_0, v_1, ..., v_m, v_{m+1} where v_0 and v_{m+1} denote node i and flip-flop j, respectively. Then the electrical masking function is defined as

$$\lambda_{\mathrm{elec-mask}}(\mathrm{i,j,q}) = \delta_{\mathrm{prop}}\left(\cdots\left(\delta_{\mathrm{prop}}\left(\delta_{\mathrm{prop}}(\mathrm{pw_0}, 1), 2\right), \cdots\right), \mathrm{m},\right) \tag{9}$$

where $pw_0 = \delta_{strike}(q, i)$ and $pw_k = \delta_{prop}(pw_{k-1}, k)\ \forall k \in [1,m]$

In the above definition, two undefined functions, δ_{strike} and δ_{prop}, respectively, represent the first-strike function and the electrical propagation function of transient-fault distributions. $\delta_{strike}(q, i)$ is invoked once and maps the collection charge q at node i into a voltage pulse width pw0. $\delta_{prop}(pw_{k-1}, k)$ is invoked m times and iteratively computes the pulse width pw_k after the input pulse width pw_{k-1} propagates through the k-th cell from node i. These two types of functions are also the most critical components to the success of a statistical SER analysis framework due to the difficulty from integrating process-variation impacts.

The theoretical SSER in Equation (7) and Equation (9) is analyzed from a path perspective. However, in reality, since both the signal probabilities and transient-pulse changes through a cell are independent to each other, the computation of SSER only needs to proceed stage by stage and thus can be implemented in a block-based fashion. Chapter 3, Chapter 4 and Chapter 5 will present three different block-based SSER frameworks, a table-lookup framework, SVR learning framework, and SSTA-like framework, respectively. These frameworks consider process variations but differ

from the way they compute δ_{strike} and δ_{prop}.

Chapter 3
Table-lookup Monte-Carlo (MC) Framework

The first framework combines the current static approaches with the Monte-Carlo (MC) method, a computational algorithm using repeated random samplings to mimic complex statistical behaviors of physical or mathematical systems. As depicted in Figure 1.3, this framework maps to the formulation in Section 2.4 using three loops: the outmost loop considers various levels of collection charge q_i, which forms the discrete approximation of Equation (4); the second loop accounts for all vulnerable nodes within a circuit, which corresponds to Equation (6); the innermost loop maps to Equation (9) and computes δ_{strike} and δ_{prop} implicitly. As the key component of the framework, the last loop can be further decomposed into two parts: (1) cell pre-characterization and (2) sampling and renewal of transient faults.

3.1 Cell pre-characterization

To reflect the electrical masking effect of transient faults on one cell intertwined with process variations, an approach similar to [26] is employed to extract pre-characterized tables. The objective of such pre-characterized tables is to model the pulse width and voltage magnitude for each cell as random variables that can be sampled during the particle-strike process and transient-fault propagation of one cell.

Table contents are derived on the basis of data from Monte-Carlo SPICE simulation with targeted process-variation parameters (or direct silicon measurement on test structures if applicable). Considering the mapping relationship, two types of tables are built for each cell separately: one for the particle-strike process, T_{strike}, and the other for transient-fault propagation, T_{prop}

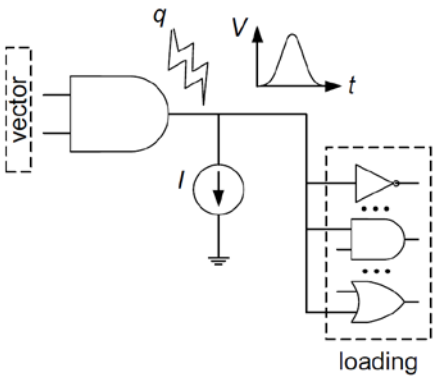
3.1.1 Particle-strike table T_{strike}

T_{strike} maps the collection charge q incurred by the particle strike to electrical properties of cells. Figure 3.1 illustrates the example to pre-characterize one AND gate by properly setting up SPICE simulation environment. Figure 3.1(a) is the circuit netlist where a charge q is injected at the output of the AND gate as an independent

current source according to [7]:

$$I(q,t) = \frac{q}{\tau_\alpha - \tau_\beta} \times (e^{-\frac{t}{\tau_\alpha}} - e^{-\frac{t}{\tau_\beta}}) \quad (10)$$

An arbitrary number of cells are also generated and connected as the output loading for the AND gate. Capacitance of each cell will be normalized in terms of the unit-size inverter (NOT). The final output loading is obtained from summing up each output cell and represented by a total number of equivalent NOTs.



(a)

vector	loading (equivalent NOTs) 1 2 3 4 ··· k
00 01 10	pulse-width mean M^{μ}_{pw}
00 01 10	pulse-width sigma M^{σ}_{pw}
00 01 10	voltage-magnitude mean M^{μ}_{vm}
00 01 10	voltage-magnitude sigma M^{σ}_{vm}

(b)

Figure 3.1: Pre-characterization of particle-strike table T_{strike} for an AND gate

Given a fixed q, a number of MC runs with different SPICE settings are repeated in Figure 1.3 to compute the means and variances of pulse width and voltage magnitude, respectively, for the resulting transient fault. Figure 3.1(b) shows the table for the AND gate including four matrices: pulse-width mean matrix (M^{μ}_{pw}), pulse-width variance matrix (M^{σ}_{pw}), voltage-magnitude mean matrix (M^{μ}_{vm}) and voltage-magnitude variance matrix (M^{σ}_{vm}) to store mean and sigma values for pulse widths and voltage magnitudes of transient-fault propagation. Note that since first-strike transient faults are sensitive to input vectors, the input vector also serves as an index in T_{strike}.

3.1.2 Transient-fault propagation table T_{prop}

The transient-fault propagation table T_{prop}, on the other hand, reflects the changes of electrical properties when propagating the transient fault through one cell. Figure 3.2(a) shows the sample SPICE simulation environment to pre-characterize the transient-fault propagation through one OR gate. The output loading is set up

similarly to the pre-characterization of T_{strike} for the AND gate mentioned above. Both input and output of the OR gate are described as glitches and pulse widths and voltage magnitudes are measured accordingly.

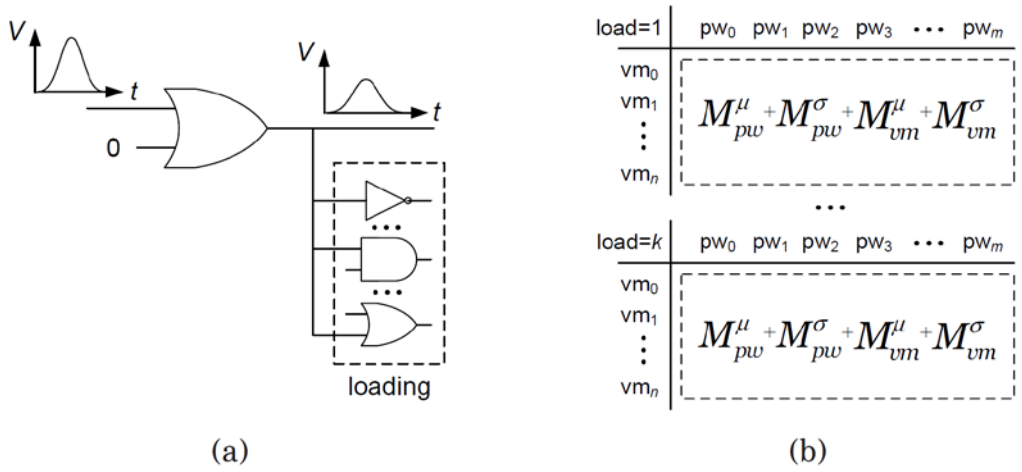


Figure 3.2: Pre-characterization of transient-fault-propagation table T_{prop} for OR gate

After performing statistical calculation, four matrices, pulse-width mean (M^{μ}_{pw}), pulse-width sigma (M^{σ}_{pw}), voltage-magnitude mean (M^{μ}_{vm}) and voltage-magnitude sigma (M^{σ}_{vm}) can be obtained for one output loading in the tables. Furthermore, each T_{prop} has three dimensions where the first one is the output loading (load = 1..k), the second one is the input pulse width (pw_0...pw_m), and the third one is the input voltage magnitude (vm_0...vm_n). Therefore, the above process iterates k times to derive one T_{prop} of size 4 × k × m× n.

3.2 Sampling and renewal of transient faults

Each Monte-Carlo (MC) run consists of two types of actions: sampling and renewal. A two-tuple transient fault f=(pw,vm) is first generated by randomly choosing pw and vm from pulse-width and voltage-magnitude distributions in T_{strike} according to the probability theory. Later, electrical properties of f after propagating through the next cell are renewed and new pulse-width and voltage-magnitude distributions can be looked up from T_{prop} of such cell. Then a sampling step repeats to pick next $f' = (pw', vm')$ followed by looking up the next $(\mu'_{pw}, \sigma'_{pw})$ and $(\mu'_{vm}, \sigma'_{vm})$ in the renewal step. The sampling and renewal steps alternate until the transient fault either reaches the input of any flip-flop or disappears during its propagation.

Transient-fault probability P(f) denotes the updated probability after f propagates through one gate and is also incorporated in the proposed table-lookup framework. Initially, all inputs are assumed to be a independent variable with equal probabilities of being 1 and 0. Probabilities for each node can be derived statically according to its input probabilities. Later, during computing the change of f on each cell, P(f) is updated simultaneously to reflect the logic masking effect mentioned in Section 2.4. Two different cases are discussed in detail as follows.

3.2.1 First-strike cases

For the first-strike cases, the struck node is required to remain 0 for a positive transient fault and 1 for a negative transient fault. Let's take one AND gate shown in Figure 3.3(a) for example. Given the collection charge q, transient fault $f_z = (pw_z, vm_z)$ can be looked up in T_{strike} and denoted as $f_z = lut_{P.S.}(q, z)$. Assume that the probabilities of being 1 for input x and y are denoted by P_x and P_y. For the particle strikes the output z to induce a positive transient fault (f_z^+), z is required to be 0 and thus, $P(f_z^+) = (1 - P_x) \times P_y$. Similarly, for a negative transient fault (f_z^-) striking output z, $P(f_z^-) = P_x \times P_y$.

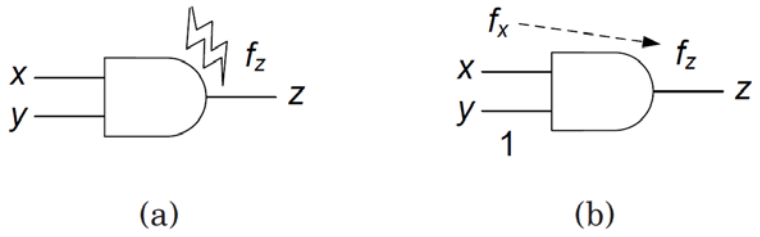


Figure 3.3: Logical probability update for an AND gate

3.2.2 Propagation cases

For the propagation cases, in order to propagate the positive (or negative) transient fault through one gate, all other side-inputs are required to be non-controlling values (n.c.v.). Besides, non-convergent and convergent conditions need to be considered separately. Figure 3.3(b) illustrates a non-convergent example of the AND gate. Similarly, given f_x, f_z can be looked up in T_{prop} by $f_z = lut_{prop.}(f_x, z) = (pw_z, vm_z$. As to transient-fault probability, since non-convergent condition assumes that only one positive (or negative) transient fault arrives one input of the AND gate, say x in this example, only y is required to be 1 (n.c.v. for the AND gate). Therefore, $P(f_z) = P(f_x) \times P_y$.

A transient fault going through multiple propagation paths may re-converge to one node, which is very expensive to handle using enumeration. Currently, the worst-case approximation is used since it is reported to have only minor estimation error. From the electrical perspective, the worst case denotes a re-convergent transient fault that has the maximum pulse-width and voltage magnitude among updated values from each input transient faults. An example for the AND gate is shown in Figure 3.4(a). Following this notion, a MAX operation is defined to facilitate such computation:

$$\begin{aligned} f_z &= \mathrm{MAX}\left(\mathrm{lut}_{\mathrm{prop}}(f_x), \mathrm{lut}_{\mathrm{prop}}(f_y)\right) \\ &= \mathrm{MAX}\left(\mathrm{lut}_{\mathrm{prop}}(pw_x, vm_x), \mathrm{lut}_{\mathrm{prop}}(pw_y, vm_y)\right) \\ &= \mathrm{MAX}\left((pw_x', vm_x'), (pw_y', vm_y')\right) \\ &= \mathrm{MAX}\left((pw_x', pw_y'), (vm_x', vm_y')\right) \\ &= pw_z, vm_z \end{aligned} \tag{11}$$

where lut() looks up values from T_{prop} in the renewal step.

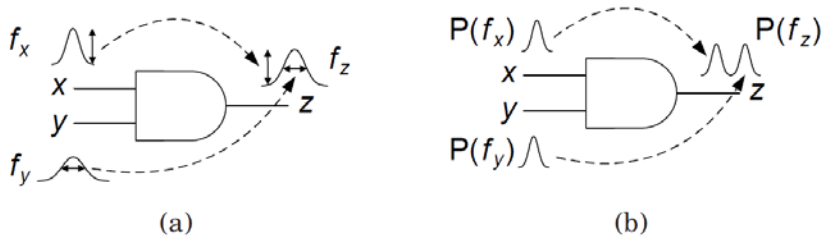


Figure 3.4: Re-convergent transient faults on an AND gate

From the logical perspective, the worst case happens when the arrival windows of two transient pulses are not overlapped and Figure 3.4(b) illustrates this concept. The corresponding transient-fault probability $P(f_z)$ can be computed by the summation of two transient-fault probabilities from input x and y. That is,

$$P(f_z) = P(f_x) + P(f_y) \tag{12}$$

3.3 Using qauasirandom sequences

Pseudorandom number generation plays a key role to the success of the Monte Carlo method. However, using rand() function for sampling points often suffers from the clustering problem in high dimensional spaces. Figure 3.5(a) illustrates this problem on an example of generating a (X, Y)-distribution by the Mont e Carlo method using the rand() function . The sampling points are observed not evenly scattered among the (X, Y) plate, which means that these sampling points from pseudorandom generation may not be representative enough for the entire space.

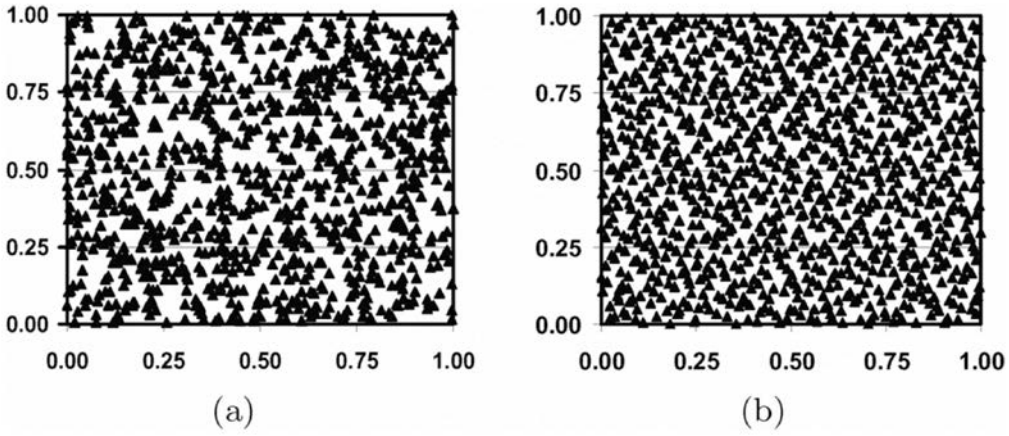


Figure 3.5: Distributions from the Monte Carlo methods with random number generation and quasirandom sequences

The clustering problem motivates research of finding a deterministic sequence such that well-chosen points are distributed in the high-dimensional spaces uniformly. Such sequences are named quasirandom sequences. Figure 3.5(b) shows the same number of sampling points using quasirandom sequences on the (X,Y) plate. Sobol algorithm is used to generate the corresponding sequences. From Figure 5(b), new sampling points are observed more uniformly distributed over the (X,Y) plate and thus have better representativeness.

Monte Carlo methods with quasirandom sequences are termed Quasi-Monte Carlo (QMC) methods. Given a sampling number N and a dimension d, Monte Carlo methods converge with $O(1/\sqrt{N})$ simulation errors whereas QMC methods converge with $O(1/\sqrt{N})$ for optimal cases. Previous research works have demonstrated better results for QMC than MC methods for t he problems with $\leq$360 dimensions in finance and physics.

Since each gate in the circuit becomes a free dimension (regardless of spatial correlations) , the total dimension in the corresponding SSER system can be very high . However, for a large d and moderate N, quasirandom sequences perform no better than the pseudorandom sequences. Besides, high dimensional quasirandom sequences tend to suffer from the clustering problem again. In the worst cases, QMC's convergence rate, $O((\ln N)^d/N)$, are even worse than MC's $O(1/\sqrt{N})$ as d goes larger . Therefore, we are motivated to apply dimension reduction to ensure the effectiveness of the proposed QMC framework for SSER analysis.

Effective dimensions of circuits can be observed through experiment s. Figure 3.6 shows the convergence rates for four sample circuit s where the vertical lines indicate the logic depths (a.k.a. levels) of each circuit. All convergence rates drop quickly as the dimension numbers increase. Such phenomenon implies their underlying SSER systems can be properly described using much lower dimensions. For example, the intuitive dimension number for the circuit c7552 is 2114, the total number of its nodes. From Figure 3.6(d), however, a dimension number of 60 is already good enough. Also, from Figure 3.6 states that the circuit level can suffice to represent the total dimension and thus converge SER faster.

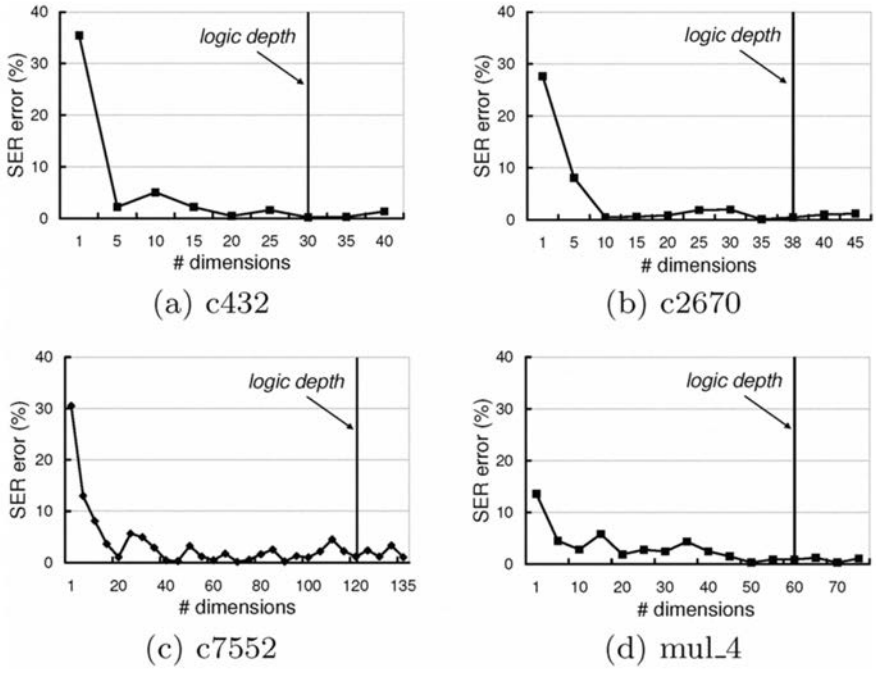


Figure 3.6: Convergence rate, dimension number, and logic depth of benchmark

3.4 Applying importance sampling on QMC

In this project, we also combine the QMC and **importance sampling** in order to efficiently calculate expectations with respect to multivariate distributions. This method can be used to circumvent the definition of non-uniform quasi-random varieties. Interpreted as a parameter transformation method, it can get rid of singularities of the integrand which increases the speed of convergence of QMC. In the case of complicated multivariate distributions the application of QMC techniques is much easier for importance sampling than for Markov chain Monte Carlo methods.

3.4.1 Importance sampling overview

In importance sampling, one attempts to avoid taking samples in regions where the value of the function is negligible, and to focus on regions where the value is large. It is important to allow for this bias in sampling by weighting the sample values appropriately. Importance sampling is based on the idea of using weights to correct for the fact that we sample from the instrumental distribution g(x) in place of the target distribution f(x). Importance sampling is based on the identity shown as follows:

$$P(X \in x)\int_x f(x)dx = \int_x g(x)\frac{f(x)}{g(x)}dx = \int_x g(x)w(x)dx$$

For all g(x), such that g(x) > 0 for (almost) all x with f(x) > 0. We can generalize this identity by considering the expectation Ef (h(X)) of a measurable function h:

$$E_f(h(X)) = \int f(x)h(x)dx = \int g(x)\frac{f(x)}{g(x)}h(x)dx = \int g(x)w(x)h(x)dx = E_g(w(X)\cdot h(X))$$

Importance sampling is a numerical method in order to approximate an integral. It can be implemented to estimate the mean response for a given sample under an alternate distribution. Importance sampling is based on the following identity. Let G and g be the distribution function and the density function of some distribution, called importance distribution in the sequel as following equation:

$$E_{f(q)} = \int_{R^d} q(x)f(x)dx = \int_{R^d} q(x)\frac{f(x)}{g(x)}g(x)dx = \int_{R^d} q(x)w(x)dG(x)$$

The importance distribution can be chosen such that it is not hard to generate a sample of points that follow the importance density. In the case of QMC this will be the inversion method. In dimension one (d = 1), we then have the estimator:

$$E_{f(q)} = \int_{R^d} q(x) f(x) dx = \int_{(0,1)} q(G^{-1}()) \cdot w(G^{-1}(u)) du$$

By a proper choice of the importance density g, the integrand has bounded variation. It is enough that g has higher tails than the product of q(x)f(x) to get rid of the singularity problem.

Algorithm 3-1 (importance sampling):

1. for i = 1 to ***n***
   generate X_i from $g(X)$;
   let $w(X_i) = \frac{f(X_i)}{g(X_i)}$;
2. return $\hat{u} = \frac{\sum_{i=1}^{n} w(X_i) \cdot h(X_i)}{\sum_{i=1}^{n} w(X_i)}$;

The following theorem, bias and variance of Importance Sampling, gives the bias and the variance of importance sampling.

(a) $E_g(\tilde{u}) = u$

(b) $\mathrm{var}_g(\tilde{u}) = \frac{\mathrm{var}_g(w(X) \cdot h(X))}{n}$

The theorem implies that contrary to $\tilde{\mu}$ the self-normalized estimator $\hat{\mu}$ is biased. The self-normalized estimator $\hat{\mu}$ however might have a lower variance. In addition, it has another advantage: we only need to know the density up to a multiplicative constant, as it is often the case in hierarchical Bayesian modeling.

3.4.2 Advantage of applying importance sampling on QMC

Two problems arise when the expectation of some function with respect to a non-uniform multivariate distribution has to be computed by (quasi-) Monte Carlo

integration: the integrand can have singularities when the domain of the distribution is unbounded and it can be very expensive or difficult to sample points from a general multivariate distribution.

$$E_{f(q)} = \int_{R^d} q(x) f(x) dx = \int_{R^d} q(x) dF(x)$$

For typical applications, we want to derive expectation, variance and some quantities of all marginal distributions together with all correlations between the variables. If we consider, for instance, the expectation, it is obvious that we have to use $q(x) = x_k$ to obtain the expectation of the marginal.

The convergence rate often can be increased when highly uniform point sets (HUPS, also called low discrepancy sequences or quasi-random numbers) are used instead of (pseudo-) random points. Such methods are called quasi-Monte Carlo methods (QMC). There exist HUPS where the star discrepancy (and thus the QMC estimator) converges with $O((\ln N)^d / N)$. When $E_f(q)$ has to be evaluated with respect to some non-uniform distribution F with bounded domain, similar results exist.

The QMC approach requires point sets with low F–discrepancy. Such point sets are also created by applying appropriate transformation methods on low discrepancy sequences. However, for general multivariate distributions such transformations are hard to find and/or numerically very expensive. Moreover, these may introduce singularities into our integration problem and thus convergence is not guaranteed by the Koksma-Hlawka inequality.

Thus, we need to transform low discrepancy point sets into sets of points with low F-discrepancy when we calculate the QMC estimator. However, the transformation methods that have been developed for non-uniform random variety generation cannot be applied for QMC, because these destroy the structure of the underlying point set. Moreover, the theory of non-uniform random numbers does not directly apply when quasi-random numbers are used.

The problem of generating non-uniform random points and that of generating non-uniform quasi-random points should be seen as different problems. For the first one, we need to transform uniform random numbers into random points. The correctness of the transformation is verified using probability theory. The structure of the used uniform pseudo-random point set is usually not taken into consideration. The

latter problem of generating quasi-random points should be interpreted as transforming the integration problem with respect to F over R_d into an equivalent one over (0, 1) with respect to the Lebesgue measure. This is required as HUPS are constructed to work for the integral over the unit cube. From this perspective, it is somewhat surprising that most papers dealing with QMC methods for evaluating expectations $E_f(q)$ do not concern about the problem of appropriate transformations.

There are some problems with this approach. First, the inverse CDF, F^{-1}, is often not given in closed form and thus numerical methods that only compute $F^{-1}(u)$ approximately have to be used. There exist fast methods for this task, but they either require the CDF or compute it by integrating the density function numerically. In the multivariate case the inversion method can be applied to the marginal distributions, if the components of the random vector X are stochastically independent. Otherwise, the conditional distribution method must be used which can be seen as the multivariate generalization of the inversion method. It needs the (inverse) CDF of conditional distributions of marginal distributions which is practically never available in practice. Moreover, the F-discrepancy is increased when the components are not independent.

A more serious problem in the framework of QMC is the fact that the inter-grand $q(F^{-1}(u))$ is often unbounded and thus has unbounded variation when the support of the distribution is unbounded. This is for instance the case when the m-th moment of the i-th variable has to be computed in Bayesian inference where $q(x) = x_i^m$ or in derivative pricing in financial engineering when $q(x)$ behaves like $\exp(\sum_{i=1}^{d} x_i)$. In this case the Koksma-Hlawka inequality does not apply and convergence of the QMC estimator is not guaranteed.

Chapter 4
Support-Vector-Regression (SVR) Learning Framework

The table-lookup Monte-Carlo framework is inherently limited in execution efficiency because it computes δ_{strike} and δ_{prop} indirectly using extensive samplings of Monte-Carlo runs. In this section, we propose another learning-based framework to do the task directly with support of support vector regression (SVR) and is found to be both more efficient and more accurate. Note that our SVR-learning framework can be represented in the same flowchart as Figure 1.3 with the replacement of first-strike tables (T_{strike}) and propagation tables (T_{prop}) with respective learning models (δ_{strike} and δ_{prop}) as shown in Figure 4.1.

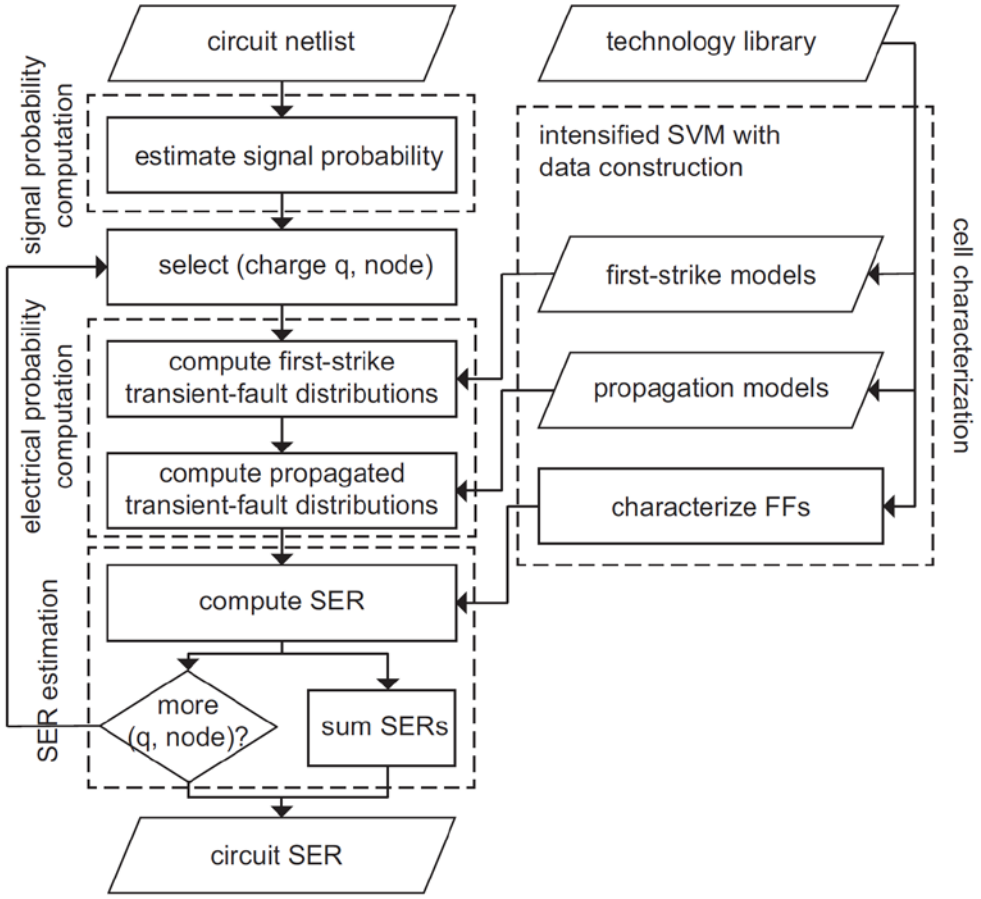


Figure 4.1: Proposed statistical SER framework using support-vector-regression models

By definition, δ_{strike} and δ_{prop} are functions of pw that is a random variable. From Figure 2.1 and Figure 2.2, we assume pw follows the normal distribution, which can be written as:

$$pw \sim N(\mu_{pw}, \sigma_{pw}) \tag{13}$$

Therefore, we can decompose δ_{strike} and δ_{prop} into four models: δ^{μ}_{strike}, δ^{σ}_{strike}, δ^{μ}_{prop}, and δ^{σ}_{prop} where each can be defined as:

$$\delta: \vec{x} \rightarrow y \tag{14}$$

where $\vec{x}$ denotes a vector of input variables and y is called the model's label or target value

Integrating the impact of process variations, four models are traditionally built using lookup tables. However, lookup tables have two limitations on applicability: (1) inaccurate interpolation and (2) coarse model size control. First, lookup tables can take only finite table indices and must use interpolation. However, interpolation functions are often not accurate enough or difficult to obtain, especially as the table dimensionality grows. Second, a lookup table stores data samples in a grid-like fashion, where the table will grow prohibitively large for fine resolution. Meanwhile, the information richness often differs across different parts of a table. For example, we observe that pulse widths generated by strong charges behave much simpler than weaker charges do. Naturally, simple behaviors can be encoded with fewer data points in the model, whereas complicated behaviors need to be encoded with more.

In statistical learning theory, such models are built using regression, which can be roughly divided into linear [27] and non-linear [28] methods. Among them, Support Vector Regression (SVR) [29] [30] combines linear methods' efficiency and non-linear methods' descriptive power. SVR has two advantages over lookup tables: (1) It gives an explicit function and need no interpolation. (2) It filters out unnecessary points and yields compact models. In the following, we propose a methodology to adapt the framework in Chapter 3 to a learning-based one based on SVR models, which comprises training sample preparation, SVR model training, and parameter selection. Also, the modification of the MAX operation in Equation (11) is addressed.

4.1 Training sample preparation

SVR models differ from lookup tables on the way we prepare training samples for them. For lookup tables, one starts from selecting a finite set of points along each table dimension. On one hand, they should be chosen economically; on the other hand, it is difficult to cover all corner cases with only a limited numbers of points. For SVR models, we do not need to select these points. Instead, we provide large sets of training samples, and let the SVR algorithm do the selection task.

A training sample set S of m samples is defined as:

$$S \in (\vec{X} \times Y)^m = \{(\vec{x}_1, y_1), \cdots, (\vec{x}_m, y_m)\} \tag{15}$$

where m pairs of input variables $\vec{x}_i$'s and target values y_i's are obtained from massive Monte-Carlo SPICE simulation. For δ^{μ}_{strike}, δ^{σ}_{strike}, we use input variables including charge strength, driving gate, input pattern, and output loading; for δ^{μ}_{prop}, δ^{σ}_{prop}, we use input variables including input pattern, pin index, driving gate, input pulse-width distribution (μ^{i-1}_{pw} and σ^{i-1}_{pw}), propagation depth, and output loading.

In our training samples, we implement output loading using combinations of arbitrary cell input pins. Doing so preserves additional information for the output loading status and saves the labor (and risk) of characterizing the capacity of each cell's input pin. Although the number of such combinations can easily explode, there are usually only a limited number of representatives, which are automatically identified by SVR. Furthermore, from a learning perspective, since both peak voltage and pulse width are the responses of charge injection current formulated in Equation (10), they are highly correlated. Empirically, using pulse-width information alone can yield satisfactory SSERs and thus in our framework, we do not need to incorporate models for peak voltage.

4.2 Support vector machine and its extension to regression

Support vector machine (SVM) is one of the most widely used algorithms for learning problems [29] and can be summarized with the following characteristics:

- SVM is an efficient algorithm and finds a global minimum (or maximum) for a convex optimization problem formulated from the learning problem.
- SVM avoids the curse of dimensionality by capacity control and works well

with high-dimensional data.

- SVM automatically finds the decision boundary for a collection of samples using a small subset where each sample is called a support vector.

The basic idea behind SVM is to find a function as the decision boundary with minimal errors and a maximal margin to separate data in multi-dimensional space. Given a training set S, with $\vec{x}_i \in R^n$, $y_i \in R$, the SVM learning problem is to find a function f (first assume $y = f(\vec{x}_i) = \langle \vec{w} \cdot \vec{x} \rangle + b$ that models S properly. Accordingly, the learning task is formulated into a constrained optimization problem as follows,

$$\begin{aligned} &\text{minimize } \|\vec{w}\|^2 + C(\textstyle\sum_{i=1}^{m} \xi_i)^k \\ &\text{subject to } \begin{cases} y_i(\langle \vec{w} \cdot \vec{x} \rangle + b) \geq 1 - \xi_i, i = 1, \dots, m, \\ \xi_i \geq 0, i = 1, \dots, m \end{cases} \end{aligned} \tag{16}$$

ξ_i is a slack variable providing an estimate of the error induced by the current decision boundary; C and k are user-specified parameters indicating the penalty of function errors in control. Later, the Lagrange multiplier method can efficiently solve such a constrained optimization problem [29] and finds $\vec{w}$ and b for $f(\vec{x}_i) = \langle \vec{w} \cdot \vec{x} \rangle + b$ with a maximal margin $2/|\vec{w}|$ between $\langle \vec{w} \cdot \vec{x} \rangle + b = +1$ and h $\langle \vec{w} \cdot \vec{x} \rangle + b = -1$. Figure 4.2 shows an example for a two-dimensional data set containing samples of two different classes. Figure 4.2(a) illustrates many possible decision boundaries to separate the data set whereas Figure 4.2(b) shows the one with the maximal margin and the minimal errors that the user can tolerate among all boundaries.

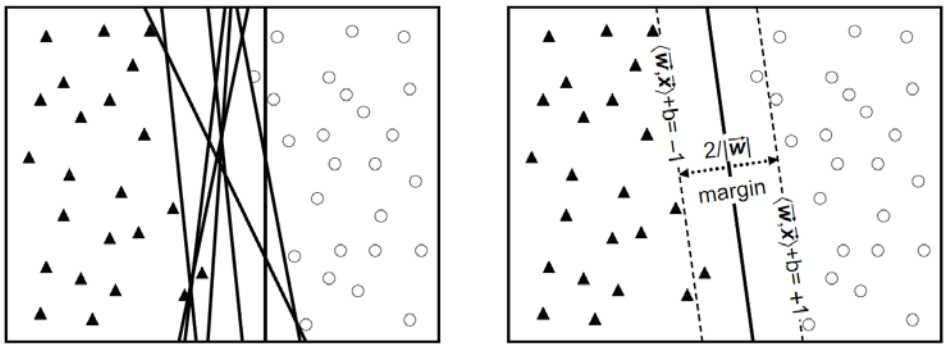


Figure 4.2: Linear decision boundaries for a two-class data set

One SVM algorithm can be applied to regression problems with three steps: (1) primal form optimization, (2) dual form expansion, and (3) kernel function

substitution. The primal form presents the nature of the regression whereas the dual form provides the key to the later non-linear extension using kernel functions. In our framework, ϵ-SVR [29] is implemented to realize a family of highly non-linear regression models $f(\vec{x}_i) : \vec{x} \rightarrow y$ for δ^{μ}_{strike}, δ^{σ}_{strike}, δ^{μ}_{prop}, and δ^{σ}_{prop} for pulse-width mean and sigma of first-strike functions and pulse-width mean and sigma of propagation functions, respectively.

4.2.1 Primal form optimization

The regression's goal is to derive a function that minimizes slacks and meanwhile to make f as smooth as possible. The corresponding constrained optimization problem for ϵ-SVR is modified as follows,

$$\begin{aligned} &\text{minimize } \|\vec{w}\|^2 + C\sum_{i=1}^{m}(\xi_i^{\,2} + \hat{\xi}_i^{\,2}) \\ &\text{subject to } \begin{cases} (\langle \vec{w} \cdot \vec{x}_i \rangle - y_i) \le \epsilon + \xi_i, i = 1, \dots, m, \\ y_i - (\langle \vec{w} \cdot \vec{x} \rangle + b) \le \epsilon + \hat{\xi}_i, i = 1, \dots, m, \\ \xi_i, \hat{\xi}_i \ge 0, i = 1, \dots, m \end{cases} \end{aligned} \tag{17}$$

where the two slack variables ξ_i and $\hat{\xi}_i$ represent variations of the error exceeding and below the target value by more than ϱ, respectively. The parameter C determines the trade-off between the smoothness of $f(\vec{x}_i)$ and the variation amount of errors (ξ_i and $\hat{\xi}_i$) to be tolerated. Equation (17) is termed the regression's primal form.

4.2.2 Dual form expansion

Instead of finding $\vec{w}$ directly, the Lagrange multiplier method transforms the optimization problem from the primal form to its dual form and derives f as,

$$f(\vec{x}_i) = \sum_{i=1}^{m}(\alpha_i - \alpha_i^*)\langle \vec{x} \cdot \vec{x}_i \rangle + b \tag{18}$$

where α_i, α_i^* are Lagrange multipliers and b is a function of ϵ, C, α's and α^*'s [30].

Several findings can be inferred from Equation (18). First, the only inner product $\langle \vec{x} \cdot \vec{x}_i \rangle$ implies that only an unseen sample $\vec{x}$ and a training sample $\vec{x}_i$, are sufficient to predict a new unseen target value y. Second, only training samples $\vec{x}_i$'s that correspond to nonzero $(\alpha_i - \alpha_i^*)$'s contribute to the prediction outcome. All other samples are unnecessary for the model and are filtered out during the training process.

Third, the inner product operation is a form of linear combination. As a result, the predicted target values of such a model are all linear combinations of training samples and thus f is a linear model. In practice, SVR often keeps only few samples (i.e., $\vec{x}_i$'s with nonzero coefficients) in its models and thus benefits from both smaller model size and faster prediction efficiency.

4.2.3 Kernel function substitution

According to the statistical learning theory [29], SVM remains valid if the inner product operation $\langle \vec{u} \cdot \vec{v} \rangle$ in Equation (18) is substituted by a kernel function $K(\vec{u} \cdot \vec{v})$ [31]. That is,

$$f(\vec{x}_i) = \sum_{i=1}^{m} (\alpha_i - \alpha_i^*) K(\vec{x} \cdot \vec{x}_i) + b \quad (19)$$

Radial Basis Function (RBF) is one kernel function used in our framework and can be formulated as $K(\vec{u} \cdot \vec{v}) = e^{-\gamma \cdot \|\vec{u}-\vec{v}\|^2}$ where γ is a controlling parameter. Unlike the inner product operation, the RBF kernel is highly non-linear. This enables the SVM algorithm to produce families of non-linear models that are suitable to capture complicated behaviors, like that of generation and propagation of pulse-width distributions of transient faults.

4.3 Parameter search

Now we return to the issue of selecting parameters (ϵ,C,γ) that have an unbounded number of combinations and is critical to achieving fine model quality. Figure 4.3 illustrates 200 models built from the same training sample set; each point represents one model using a distinct parameter combination. Their quality is measured along two coordinates: Y-axis denotes the error rate for prediction; X-axis denotes the sample compression ratio, the ratio between the number of samples kept by the model and the original size of S. Figure 4.3 shows that while it is possible to obtain an ideal model that is small and accurate (indicated by the circle), it is also possible to obtain a large and inaccurate model (indicated by the square). The differences are 20X in both axes, and there is so far no deterministic method to find the best combination.

Since exhaustive search is clearly impractical, we need an efficient searching process with an effective cost function, which is written as:

$$(\hat{\epsilon}, \hat{C}, \hat{\gamma}) = \arg\min(E^k R) \quad (20)$$

In Equation (20), E^kR denotes the cost function, where E and R respectively denote error rate and compression ratio, and k is a parameter controlling the trade-off between E and R. A larger k makes the cost function more sensitive to the error rate, and vice versa. Note that if a single k is used, the cost function may wrongly select a combination with one matrix being extremely low whereas the other being undesirably high, e.g. E = 0.01% and R = 0.99%, as indicated by the triangle in Figure 4.3.

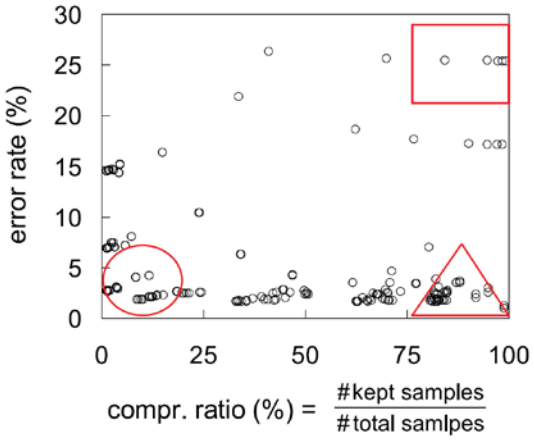


Figure 4.3: Quality comparison of 200 models using different parameter combinations

Therefore we applied a prioritized scheme according to predefined goals on both matrices as illustrated in Figure 4.4. Assuming the goal (E < 6%, R < 10%), we draw finite grids near these goals, and prioritize them accordingly. For example, G_0 is preferred over G_1, G_1 is preferred over G_2, and $G_0 \sim G_5$ are preferred over G'. The main idea is that in grids where E is small or R is large, the cost function is adjusted to be more insensitive to error. Therefore, k is assigned smaller in grids with lower error rate or larger compression ratio, as illustrated in Figure 4.4. In G', k = 3.5 generally works well.

After determining the cost function, exhaustive search may still take months. To speed up the searching process, we observe two helpful properties from samples of all our four types of models. First, a sufficiently large (> 500) sample subset shares similar behaviors as the complete sample set. Second, points forming a cluster in Figure 4.3 have similar parameter combinations. For example, the combination (ϵ, C, γ) of points within the circle has a range of $[2^{-4}, 2^{-6}]$ on ϵ, $[2^4, 2^8]$ on C, and $[2^{-2}, 2^{-6}]$ on γ. The first property enables the use of subset search; the second property allows for incremental search with granularity. Parameter search is critical for building SVR models. Using the prioritized cost function, we can systematically find a good

parameter combination

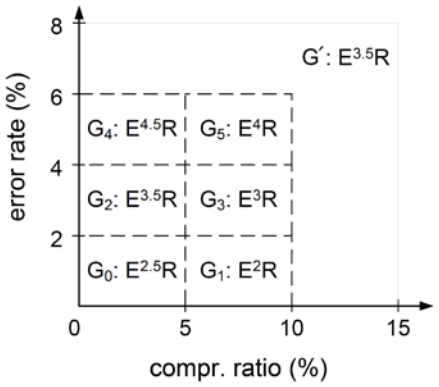


Figure 4.4: Prioritized scheme for parameter search

4.4 An intensified learning framework

This section uses an intensified learning with data construction method for statistical model extraction. The proposed algorithm also incorporates an automatic bounding-charge selection technique to remove unnecessary charges for facilitating SER estimation.

4.4.1 Intensified learning with data reconstruction

Although the SVM provides accurate and compact models estimate SER, two problems remain unsolved: (1) the training time for data preparation and (2) parameter search for high quality models. For these two problems, this framework incorporates a metaheurisitc, particle swarm optimization (PSO), to facilitate the search for the optimal setting within short training time.

PSO is one of the evolutionary computation techniques developed by Kennedy and Eberhart in 1995 [32]. PSO adopts a strategy to search for potential solutions based on the behavior of particle swarms which are inspired by swarm intelligence from insects, birds and fish. Initially, PSO generates a set of random particles in a multi-dimensional search space. The position and velocity are each represented by a particle. The position indicates a possible solution of the optimization problem and the velocity is used to determine the search direction. During each iteration, particles change their positions by tracking the best position of all particles (G_{best}) and their best positions (P_{best}). The velocity and position of particle *i* is updated according to the following equation:

$$V_i^{k+1} = wV_i^k + c_1 r_1 (Pbest - X_i^k) + c_2 r_2 (Gbest - X_i^k)$$

$$X_i^{k+1} = X_i^k + V_i^{k+1}$$

,where k is the iteration number, w is the inertia weight, c_1 and c_2 are the learning factor, and r_1 and r_2 are random numbers among range [0,1].

The advantages of PSO are easy implementation, it requires only a few setting parameters to be adjusted, and it is capable of avoiding being trapped in a local optimum solution when compared with other evolutionary algorithms, such as the genetic algorithm (GA).

Figure 4.5 illustrates the interaction between our intensified SVM-learning and PSO. First, PSO generates a set of training parameters required for SVM to build behavioral models. After building the training models, the SVM reports model's accuracy to PSO as its fitness value. Based on the model's accuracy, PSO will breed new generations and generate better parameters for training. This process iterates for a specific number of generations or until achieving a stopping criteria.

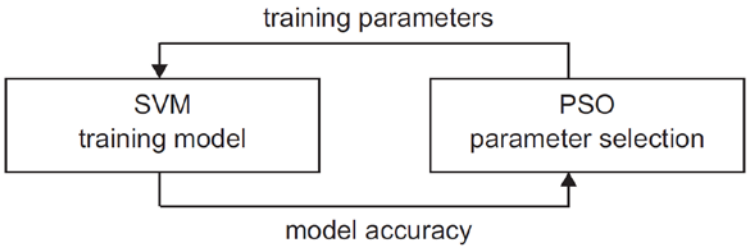


Figure 4.5: Intensified SVM learning with PSO

Besides PSO, this study uses a data reconstruction technique to reduce the size of the training data and greatly improve the training time and the compression ratio of models. This data reconstruction calculates the average value of training data in each block (Fig. 4.6). The red points represent the raw data from the extensive SPICE simulation. The green points illustrate the average values of each block. After reconstruction, the size of the training data is greatly reduced. Combining the intensified learning with data reconstruction, the framework can systematically find a set of high quality parameters to build accurate models. Furthermore, training time significantly reduces from the order of months to the order of hours.

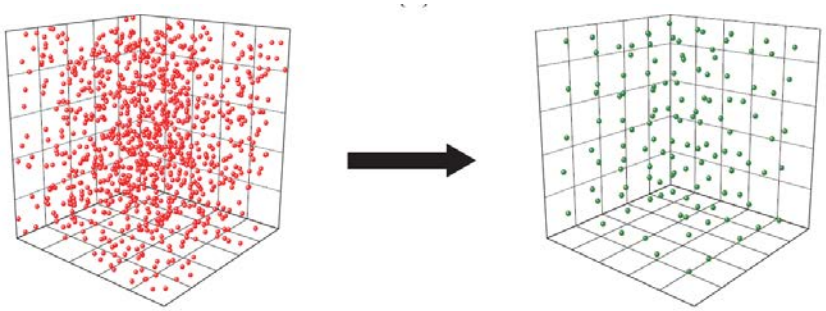


Figure 4.6: Example for data construction

4.4.2 Automatic bounding-charge selection

Computing SER with full-spectrum charge collection is still challenging, even using the new models. Therefore, to save time from too many rounds of statistical analysis, a technique of automatic bounding-charge selection is further proposed to discover charges that only need to be computed by traditional static analysis.

Figure 4.7 shows the mean, sigma, lower bound (mean-3*sigma), and upper bound (mean+3*sigma) of TF distributions, which are induced by different levels of deposited charges. Results show that the mean of pulse widths increases monotonically as the deposited charge increases. The larger deposited charge also leads to a smaller sigma of its pulse width. Hence, larger lower- and upper- bounds of the TF distribution can be observed when the level of charge collection increases.

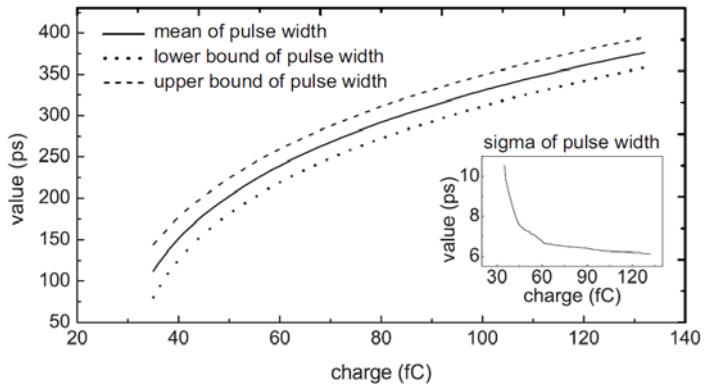


Figure 4.7: The mean, sigma, lower bound (mean-3*sigma) and upper bound (mean+3*sigma) of TF distribution which are induced by different electrical charges.

Based on this finding, a technique of automatic bounding-charge selection is proposed to accelerate the overall SER estimation. For computing overall SERs, this study only needs to consider the distribution of a pulse width, which overlaps the

latching-window (Fig. 4.8). The pulse-width distributions in dotted lines are entirely masked. The pulse-width distributions in solid lines undoubtedly results in soft errors. In other words, when the lower bound of a TF distribution exceeds than the latching-window size, the SER from such distribution can be replaced by the corresponding static results. On the contrary, the SER from a distribution in the dotted line induced by a weaker deposited charge (its upper bound is smaller than the latching-window size), will be masked completely and can be ignored. Only distributions in dash lines require statistical analysis.

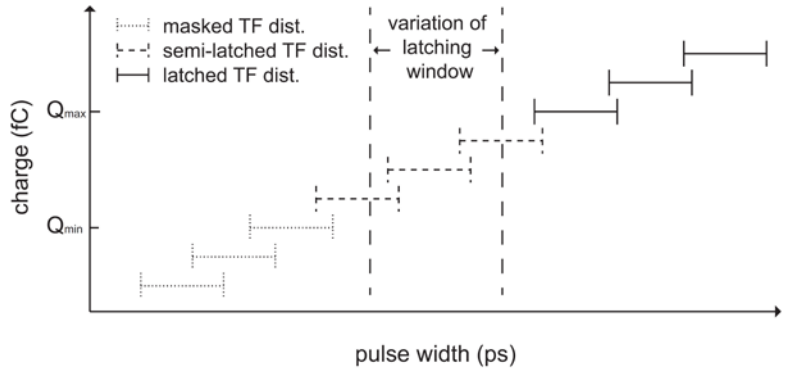


Figure 4.8: Different pulse-width distributions versus a latching-window size

Algorithm 4.1 shows the pseudocode for automatic bounding-charge selection. First, it chooses deposited charge q to strike a gate in the circuit and then it derives the upper and lower bounds of TF distributions from each Flip-Flop. After estimating the upper and lower bounds, the maximum upper bound and minimum lower bound can be found. If the maximum upper bound is smaller than the latching-window size, then the minimum charge (Q_{min}) is obtained. On the other hand, the maximum charge (Q_{max}) is decided when the minimum lower bound of TF distribution is greater than the latching-window size. As a result, the algorithm only considers deposited charges in the range of [Q_{min},Q_{max}] for SER estimation.

Algorithm 4.1: Automatic bounding charge selection

```
Automatic_Bounding_Charge_Selection()
1  while Q_min or Q_max are undecided
2      pick a charge q
3      compute each TF dist. latched by each FF
4      MaxUpperBound=max(upper bound of TF dist.)
5      MinLowerBound=min(lower bound of TF dist.)
6      if MaxUpperBound < latching-window size
7          Q_min=q
8      if MinLowerBound > latching-window size
9          Q_max=q
10 end
```

Chapter 5
Closed-form SSTA-like Framework

Regardless of the methods used, current statistical SER (SSER) frameworks (table-lookup or support-vector-regression) invariably involve a trade-off between accuracy and efficiency. This chapter presents accurate cell models in first-order closed-form to overcome this problem, thereby enabling the analysis of SSERs in a block-based fashion similar to statistical static timing analysis (SSTA). These cell models are derived as a closed form in the proposed framework and remain precise under the assumption of a normal distribution for the process parameters.

5.1 Statistical static timing analysis (SSTA)

Visweswariah et al. [33] proposed a canonical first-order delay model that considers both correlated and independent random sources as shown in Figure 5.1. By expressing timing quantities in closed form, the arrival time and required arrival time can be propagated through a timing graph using a linear-time block-based statistical timing algorithm. Moreover, the local and global criticality probabilities can be computed in a short time. In standard or first-order closed-form, a timing quantity t for a gate or wire delay can be expressed as follows:

$$t \triangleq a_0 + \sum_{i=1}^{n} a_i \Delta X_i + a_{n+1} \Delta V_a$$

where a_0 is the nominal value of the delay, X_i represents the variation of n global sources X_i from their nominal value, a_i is the sensitivity of each global source of variation, and $\forall i \in [1, n]$. V_a is the variation of an independent random variable V_a from its nominal value and a_{n+1} is the sensitivity of the timing quantity to V_a.

To apply the first-order closed-form statistical static timing analysis, two operations, sum and max, are required. The procedure of the sum operation of two jointly-distributed random variables is described as follows:

Let $t' = t + d$, where t' is the sum of two mutually-correlated and normally-distributed variables t and d where μ_t, μ_d, σ_t, and σ_d are their means and variations, respectively. The mean and variance of t' can be derived as:

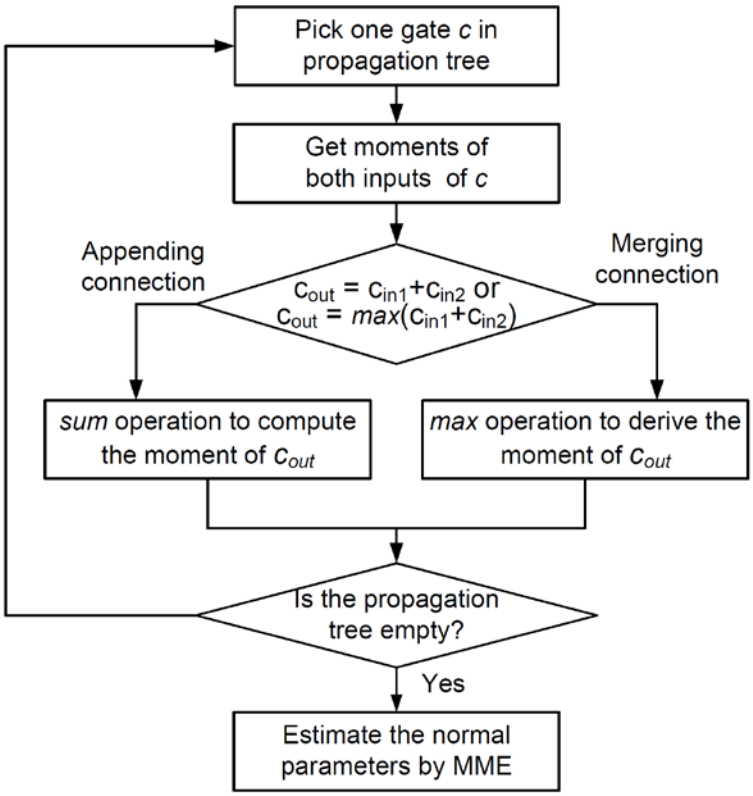


Figure 5.1: Flowchart of closed-form block-based SSTA

$$\begin{aligned}\mu_{t'} &= E(t') = E(t+d)\\ &= E(t) + E(d) = \mu_t + \mu_d \end{aligned} \tag{21}$$

$$\begin{aligned}\sigma_{t'}{}^2 &= E\left(\left(t' - E(t')\right)^2\right)\\ &= E\left(t'^2\right) - (E(t'))^2\\ &= E((t+d)^2) - (E(t+d))^2\\ &= E(t^2) + 2E(td) + E(d^2) - (E(t))^2 - \\ &\quad 2E(t)E(d) - (E(d))^2\\ &= E(t^2) - (E(t))^2 + E(d^2) - (E(d))^2 + 2E(td) - \\ &\quad 2E(t)E(d)\\ &= \sigma_t^2 + \sigma_d^2 + 2\rho_{td}\sigma_t\sigma_d \end{aligned} \tag{22}$$

where ρ_{td} denotes the correlation coefficient of t and d.

Visweswariah et al. [33] further used the concept of tightness probability to deduce the result of the max operation of two timing quantities in closed-form. The definition of the max operation is described as follows:

Let Z = max(X, Y), where Z is the responsive random variable derived by taking a max operation between random variables X and Y . The moment of Z can be derived as:

$$\begin{aligned}\mu_Z &= E(Z) = E(\max(X,Y)) \\ &= \mu_X T_x + \mu_Y(1-T_X) + \theta_\phi\left(\frac{\mu_X+\mu_Y}{\theta}\right) \qquad (23)\\ \sigma_Z^2 &= \mu_2(Z) = \mu_2(\max(X,Y)) \\ &= (\sigma_X^2+\sigma_{ZX}^2)T_X + (\sigma_Y^2+\sigma_Y^2)(1-T_X) \\ &\quad +\left(\mu_X+\mu_Y\right)\theta_\phi\left(\frac{\mu_X+\mu_Y}{\theta}\right) - \mu_Z^2 \qquad (24)\end{aligned}$$

The definition of tightness probability T_X is the probability of random variable X being larger than random variable Y. θ is the intermediate notation used to compute T_X. More details regarding (23) and (24) can be found in [34][35].

Similarly, in our SSER framework, a transient fault is split into two transition signals, which are both timing quantities and expressed in closed forms. Thus, they can also be efficiently analyzed in a parameterized block-based method like SSTA. The only difference is that SSER considers changes in the pulse-width of a transient fault, whereas SSTA emphasizes the timing signal with the maximum delay.

5.2 Algorithm of transient-fault propagation on SSTA framework

Because it is possible for a transient fault to occur at any gate on the circuit under test (CUT), all gates must be considered as candidates for hit gates. As soon as the hit gate c_i is determined, the transient fault induced by a particle hit at the output of c_i is generated and split into rising and falling transitions using the first-hit model hit, where upon the propagation model prop is employed to propagate both transitions. Transitions appearing at one primary output (PO) or pseudo primary output (PPO) are merged to reconstruct the transient faults, which are then used to compute SER. The pseudocode of the algorithm for electrical-pulse propagation is described below.

In the generation stage, the first-hit model Ψ_{hit} is used to deduce the distribution of the particle-induced transient fault on the output pin of the hit gate c_i. The initial transient fault is then split into a rising-transition signal and a falling-transition signal, denoted as t_r^0 and t_f^0 , respectively, and their moments can also be deduced by Ψ_{hit}.

Algorithm 5.1: Transient fault at (hitGate c_i)

1: Split transient fault at c_i into t_r^0 and t_f^0
2: Mark propagation tree (G_{prop}) rooted at hit gate c_i
3: Sort G_{prop} topologically
4: **repeat**
5: Gate Z = output of next gate c_j in G_{prop}
6: D = Get_Moment(c_j)
7: **if** Z is not a RFON **then**
8: X = on-path input of c_j
9: t_x = Get_moment(X)
10: t_z = sum(D,t_x)
11: **else**
12: (X,Y) = inputs of c_j
13: t_x = Get_moment(X)
14: t_y = Get_moment(Y)
15: t'_x = sum(D,t_x)
16: t'_y = sum(D,t_y)
17: t_z = ***mix***(t'_x,t'_y)
18: **end if**
19: **until** all gates in G_{prop} are VISITED
20: Merge transitions into transient faults
21: **return** transient-fault moments at one PO/PPO

The propagation stage starts after the generation stage and can be divided into three steps: in the first step, the breath-first search is employed to acquire the propagation tree G_{prop} of the transient fault starting from c_i and terminating at any PO or PPO. Once a gate is visited, it is added to G_{prop} and the flag is set as VISITED so that any gate on the reconvergent gates will not be added again. After G_{prop} is built, all gates in G_{prop} are ranked according to their topological orders.

In the second step, the initial transition signals t_r^0 and t_f^0 are propagated along G_{prop} using the propagation model Ψ_{prop} in a block-based fashion. During propagation, the two conditions are handled in different ways. For the case in which the output pin of the current gate c_j is a reconvergent fanout node (RFON), sum and mix (introduced in next section) operations are deployed to deal with the issue of convolution of transient faults. For the opposite case, only the sum operation is required.

In the final step, the transient faults arriving at one PPO or PO are reconstructed by merging t_r and t_f, and combined pulse-width distributions are used to compute SER, accordingly. Details regarding Ψ_{hit} and $\Psi_{prop}$are described in the following section.

5.3 First-order closed-forms for Ψ_{hit} and Ψ_{prop}

Traditional Monte-Carlo methods for SSER analysis are known to suffer from long simulation times when deriving the pulse-width distribution for particle hits and transient-fault propagation. Therefore, this paper employs a parameterized first-order closed-form for these two distributions. We simply divide a transient-fault into two transition signals (rising and falling), and each signal can be analyzed individually. Accordingly, rising and falling transitions are modeled as two normally distributed random variables, t_r and t_f. Moreover, the first-hit and propagation distribution functions, Ψ_{hit} and Ψ_{prop}, can be expressed in the form of

$$\Psi: \vec{x} \rightarrow \vec{y}$$

where $\vec{x}$ denotes a vector of input variables and $\vec{y}$ denotes a vector of target values. $\vec{x}$ provides guidance to find the target $\vec{y}$ in the models and includes several relationships of electrical and physical properties between gates and transient faults.

For example, the width of a transient pulse hitting the output of a gate decreases as the output load of the gate increases (because the charging/discharging time of capacitors increases). Another example is that a hitting charge with greater strength causes a wider transient pulse. Hence, for the first-hit model Ψ_{hit}, $\vec{x}$ includes charge strength, the type of driving gate and output loads; $\vec{y}$ contains the distribution of initial pulse width, correlation coefficients and slopes of the two transitions. Similarly, for Ψ_{prop}, $\vec{x}$ consists of the same components as $\vec{x}$ in Ψ_{hit} with an additional component – the slope of the transition signal; $\vec{y}$ contains the transition slope, the distribution of gate delay, the correlation between transition signal and the corresponding gate delay, and the correlation between transition signals.

From the proposed idea, a random variable pw, denoting the width of a particle-induced transient pulse can be decomposed into two normal jointly-distributed random variables, the rising transition t_r and the falling transition t_f , expressed as:

$$pw = \begin{cases} t_f - t_r & \text{if the pulse is positive} \\ t_r - t_f & \text{if the pulse is negative} \end{cases} \quad (25)$$

Based on Ψ_{hit} and Ψ_{prop}, both t_r and t_f are then using a parameterized SSTA-like method where the approximated distribution of pw can be derived by replacing the statistical variables μ_{pw} and σ_{pw} with the estimators $\hat{\mu}_{pw}$ and $\hat{\sigma}_{pw}$. The overall analysis is outlined as follows:

1) **Transient-fault generation and decomposition:** Initially, the first-hit model Ψ_{hit} is used to look up the distribution of the initial pulse width pw_0 from a pre-characterized table according to the output load of the hit gate and the strength of the hitting charge. Then, the estimated pulse width $\widehat{pw0}$ is decomposed into two initial transitions t_r^0 and t_f^0 according to the ratio of their slopes.
2) **Block-based propagation:** Two timing signals are updated by Ψ_{prop} whenever they are propagated through one gate, reflecting the gate delay. This step repeats until both the rising and falling signals arrive at one PO or PPO.
3) **Pulse-width reconstruction:** Once both signals reach PO or PPO, they are merged to reconstruct a new transient pulse to determine whether or not a soft error has occurred. The reconstruction step uses the idea proposed in (25).

Taking Figure 5.2 as an example, the original transient pulse generated by a particle hit at the output of G0 is split into two transition signals, which then individually begin their propagation. Finally, both signals end at G2 and are merged to reconstruct the transient pulse.

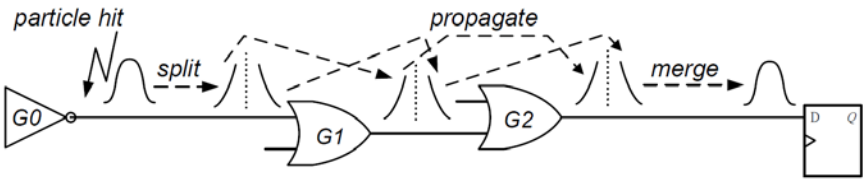


Figure 5.2: SSTA-based method w/o considering the correlation between transition signals

Details of each step are organized as follows. After introducing the first-hit model and propagation model in Section 5.3.1, the distributions of the width in a transient fault is estimated by the MME [35] in Section 5.3.2. The two issues related to correlation and reconvergence are discussed in Section 5.3.3 and 5.3.4, respectively.

5.3.1 Constructing linear timing models

In the first step, Ψ_{hit} is responsible for approximating the distribution of t_r^0 and t_f^0 and the corresponding computations can be enumerated as:

$$\mu_{t_r^0} = 0$$

$$\mu_{t_f^0} = \mu_{\widehat{pw_0}}$$

$$\sigma_{t_r^0}^2 = \sigma_{t_f^0}^2 \times \tau_{r/f}^0$$

$$\sigma_{t_f^0}^2 = \sigma_{\widehat{pw_0}}^2/(1 + (\tau_{r/f}^0)^2 - 2\tau_{r/f}^0 \times \rho_{t_r^0 t_f^0})$$

where the superscript is the corresponding topological order originating from hit gate G0, $\tau_{r/f}^0$ denotes the slope ratio defined as the slope of the rising signal to that of the falling signal, and $\rho_{t_r^0 t_f^0}$, pre-characterized into a table, is the correlation coefficient of t_r^0 and t_f^0.

After obtaining the distributions of the two initial transition signals, the linear timing model Ψ_{prop} is deployed to propagate both signals towards the primary outputs. The derivation of the linear timing model Ψ_{prop}, computed by typical statistical static timing analysis, is given as:

Transition signal t arrives at the input of a gate with delay d, where t and d can be expressed in linear closed-form as

$$t = t_0 + \sum_{i=1}^{n} a_i \Delta X_i + a_{n+1} \Delta V_a$$

and

$$d = d_0 + \sum_{i=1}^{n} b_i \Delta X_i + b_{n+1} \Delta V_b$$

Note that t_0 and d_0 are the nominal values of t and d, respectively.ΔX_i is the variation of n global sources from their nominal values; a_i and b_i represent the sensitivities of the transition signal and gate delay, respectively, of each ΔX_i. Both ΔV_a andΔV_b are variations of the independent random variables V_a and V_b from their mean values, and their timing sensitivities are denoted as a_{n+1} and b_{n+1}, respectively.

After the timing signal t passes through the gate, the output timing signal t' is updated as t+d, enabling us to deduce t' by a sum operation of two normal jointly-distributed random variables, as described in Section 5.1. Hence, a rising signal t_r^{in} and falling signal t_f^{in} at the gate input can be propagated to the gate output and modeled by Ψ_{prop}. Accordingly, the two output timing signals become

$$t_r^{out} = t_r^{in} + d_r \tag{26}$$
$$t_f^{out} = t_f^{in} + d_f \tag{27}$$

where subscripts r and f represent rising and falling, respectively, and the superscript (input or output) represent the pin locations.

Since we have deduced the first-hit model Ψ_{hit} and the propagation model Ψ_{prop}, the pulse width of a transient fault can be approximated using (25).

5.3.2 Estimating pulse-width parameters

Given the first-hit model Ψ_{hit} and the propagation model Ψ_{prop}, the final distribution of $\widehat{pw}$ in Fig. 6 can be further expanded according to (25). That is,

$$\begin{aligned}\widehat{pw} &= t_f^2 - t_r^2 \\ &= (t_f^1 - d_f^2) - (t_r^1 - d_r^2) \\ &= (t_f^0 - \textstyle\sum_{i=1}^{2} d_f^i) - (t_r^0 - \sum_{i=1}^{2} d_r^i)\end{aligned} \tag{28}$$

where the superscript is the corresponding topological order originating in the hit gate.

Thus, the distribution of $\widehat{pw}$ can be calculated by performing a series of sum operations over transition signals and corresponding gate delays. To derive the general form of a transient pulse, which is generated at one hit gate at the m-th level and propagated to one flip-flop at the n-th level where n > m, we can generalize (28) and rewrite it as:

$$\begin{aligned}\widehat{pw} &= t_f^{n-m} - t_r^{n-m} \\ &= (t_f^0 - \textstyle\sum_{i=1}^{n-m} d_f^i) - (t_r^0 - \sum_{i=1}^{n-m} d_r^i)\end{aligned} \tag{29}$$

5.3.3 Determining whether to consider transition correlation

Correlation is a major concern when using a first-order closed-form method to

approximate the behavior of transient pulses. This is because the pair of transition signals t_r and t_f are mutually dependent rather than completely uncorrelated. Intuitively, the solution to this issue is to iteratively split and merge the transient faults during propagation. As illustrated in Figure 5.3, a transient pulse is reconstructed by merging t_r and t_f after both transitions pass through a gate, and then splitting them again before they are propagated towards the succeeding gates.

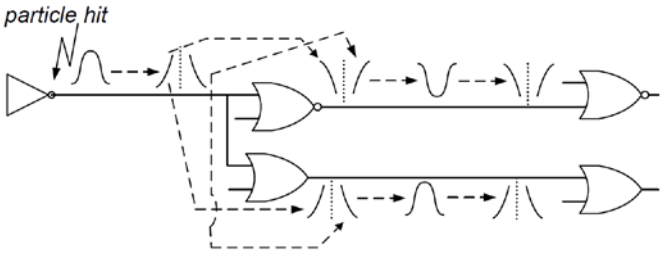


Figure 5.3: Process of iterative split and merge

Experimental results show that this process can be skipped because the impact of the correlation between transition signals on SSER is small. In Table 5.1, the name of each circuit is listed in column 1; the remaining two columns show the results derived by the closed-form block-based SSER framework with independent transition signals (a) and with correlated transition signals (b), respectively. The last column computes the difference of the SSER results derived using these two methods. According to Table 5.1, it is clear that the discrepancy between the SER results derived by the two methods is negligible on four ISCAS'85 benchmark circuits (from small to large), demonstrating that the correlation between transition signals can be overlooked.

Table 5.1: Comparison of SER w/o and w/ considering the correlation between transition signals

Circuit	(a) $SSER_{indep.}$ (μFIT)	(b) $SSER_{corr.}$ (μFIT)	Difference (%) $\frac{(b)-(a)}{(a)} \times 100$
c17	56.27	56.28	1.78×10^{-2}
c432	2.28×10^{5}	2.28×10^{5}	-1.82×10^{-3}
c2670	8.00×10^{4}	8.01×10^{4}	6.62×10^{-4}
c6288	8.10×10^{7}	8.10×10^{7}	-9.88×10^{-8}

5.3.4 Handling the re-convergence of transient-faults

The number of transient faults doubles if there is a reconvergent structure along the propagation path in the circuit, resulting in an exponential increase in the complexity of the SSER analysis. As shown in Figure 5.4, a particle hits the output of

G0 and induces a transient pulse. The transient faults then propagate along the paths in a block-based fashion, finally reconverging at the inputs of U0 and U1. Consequently, two positive transient faults appear on the output of U0, and two transient faults with different directions appear on the output of U1.

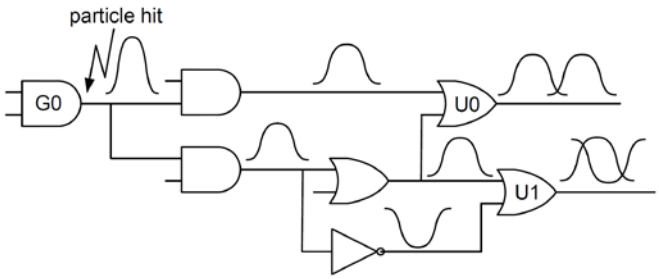


Figure 5.4: Reconvergent Structure

To resolve this problem of reconvergence, we propose a two-stage approach. In the first stage, transient faults are classified into two groups according to their directions. The outcomes of the pulse width and the logic probability of these convoluted transient faults are then derived in the second stage. The pulse-width distribution of convoluted transient faults is derived using a newly-defined mix operation in which the logic probability is updated as the union of the logic probabilities associated with these transient faults.

1) Computing re-convergent transient faults: The reason for defining a new mix operation for the two timing signals is that the pulse-width result of transient faults is underestimated and incorrect if the traditional max operation is used to deduce the result of these convoluted timing signals. The process for handling multiple positive transient faults can be expressed as

$$\mathrm{mix}(\mathrm{pw}_1, \mathrm{pw}_2, \dots, \mathrm{pw}_n) = \mathrm{mix}(\mathrm{t}_{f1}, \dots, \mathrm{t}_{fn}) + \mathrm{mix}(\mathrm{t}_{r1}, \dots, \mathrm{t}_{rn}) \quad (30)$$

The mix operation with multiple (>2) operands such as in (30) is computed by iteratively taking the 2-operand mix. Let $\mathrm{t}' = \mathrm{mix}(\mathrm{t}_1, \mathrm{t}_2)$, t_1 and t_2 follow normal distributions, and so as t'.

$$\mathrm{mix}(\mathrm{t}_1, \dots, \mathrm{t}_k) = \mathrm{mix}(\mathrm{mix}(\mathrm{t}_1, \mathrm{t}_2), \dots, \mathrm{mix}(\mathrm{t}_k, \mathrm{t}_{k+1}))$$
$$= \mathrm{mix}(\mathrm{t}_{1,\lfloor \frac{k}{2} \rfloor}, \mathrm{t}_{\lfloor \frac{k}{2} \rfloor, k})$$

$$= t_{1,k} \quad (31)$$

The two-operand mix can be further classified into two types to deduce convoluted pulses in the same directions and those in opposite directions.

To derive the pulse width of reconvergent transient faults in the same direction, we define the same-direction mix operation as a worst-case operation in which the new pulse comprises the latest transition signal and the earliest transition signal among these reconvergent transient faults. Before performing same-direction mix operations over two reconvergent transient faults, the existence of overlapping is checked. As shown in Figure 5.5(a), in the event of overlapping, the earliest transition and the latest transition are selected to form a new pulse; otherwise, the width of the new transient fault is the sum of the widths of the two convoluted transient faults, as displayed in Figure 5.5(b).

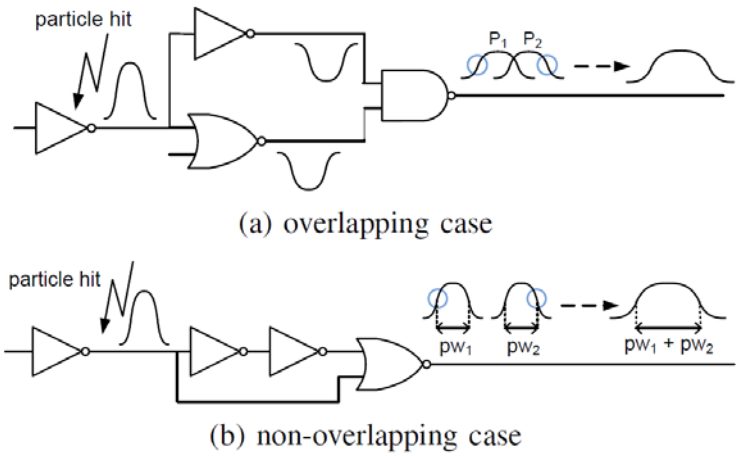


Figure 5.5: Illustration of mix operation in the same direction

The results derived using the traditional max operation in SSTA may lead to an underestimation of the pulse-width associated with reconvergent transient faults. Taking Figure 5.5(a) as an example, we denote the latter transient fault and former transient fault as P_1 and P_2, respectively. The result deduced by the same-direction mix operation performed on P_1 and P_2 should be the latest transition and the earliest transition among them, respectively denoted as t_{r1} and t_{f1}. However, the result derived using the traditional max operation performed on P_1 and P_2 are t_{r1} and t_{f2}. Similarly, in Figure 5.5(b), the pulse-width result deduced by SSTA's max operation is pw_2 rather than $pw_1 + pw_2$.

For reconvergent transient faults in opposite directions, the pulse width is determined according to interactive behavior. In Fig. 5.6, if the positive transient fault

appearing at one input of an AND gate does not overlap with the negative transient fault appearing at the other input of the AND gate, the pulse-width result is the width of the positive transient fault pw, because the negative transient fault is completely masked by the controlling value on the side input. In the event of overlapping, the result is computed as the width of positive transient fault pw subtracted by the overlapping period (d) between the positive and negative transient faults due to the negative transient fault masking part of the positive transient fault. Other gate types can be derived in a similar manner.

It is worth noting that because the timing information of transition signals is preserved, the issue of reconvergence can be analyzed in a manner that would be impossible in traditional SSER methods.

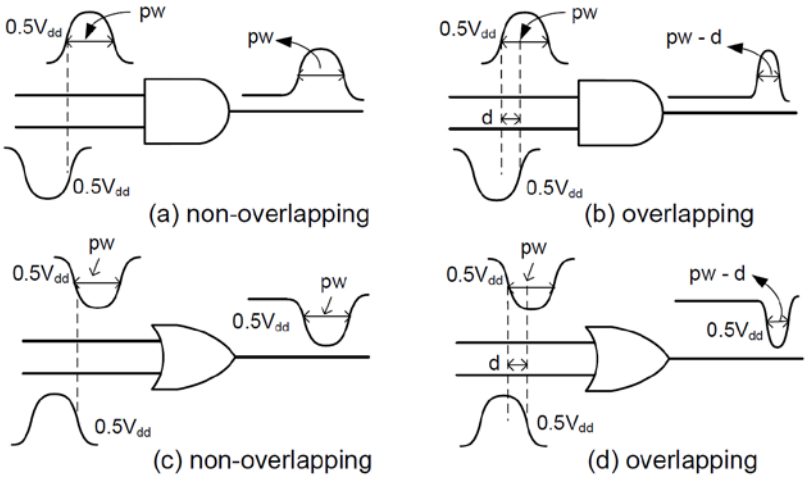


Figure 5.6: The mix operation in opposite directions for AND and OR gates

2) Updating logic probability: The logic probability at reconvergence fanout nodes should be updated to reflect the phenomenon of reconvergence. For convoluted transient faults, the result of logic probability is the union of the logic probabilities of input transient faults, because this condition is equivalent to all of these transient faults being able to pass through the reconvergent node.

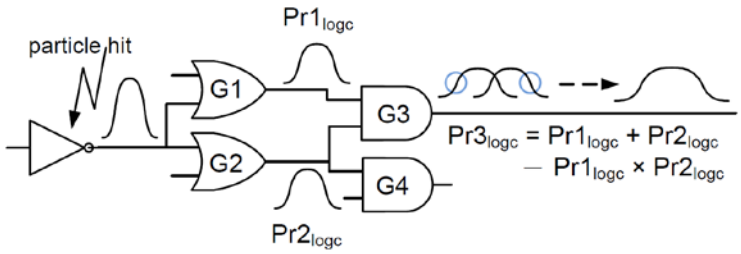


Figure 5.7: Illustration of updating logic probability at a RFON

Taking Figure 5.7 as an example, the logic probabilities of transient faults at the output pins of gate G1 and gate G2 are denoted as Pr1logc and Pr2logc, respectively. The logic probability of a transient fault at the output pin of gate G3, denoted as Pr3logc, as illustrated in Figure. 5.7.

Chapter 6
Experimental Results

In this section, all experiments are divided into two parts. The first part is to examine the accuracy of the pre-characterized lookup tables, learned models and SSTA-like method. In the second part, they are then integrated into their respective statistical SER analysis frameworks and are compared in their SSER analysis accuracy and runtime. We use a unified framework to generate test samples for the pre-characterized tables, learning models, and SSTA-like method considering process-variation impacts. For simplicity, we only consider the with-in die geometric process variation and other types of variation are not included in our work. The perturbed gate widths and channel lengths of each transistor in geometry are used to model with-in die variation since they are the dominant factors for gate delay. Note that, the other important random variation, threshold-voltage (Vth) fluctuation, can also be reflected indirectly by considering the process variation. However, more variation sources can be considered as long as their impacts can be reflected onto SPICE simulation results. As illustrated in Figure 6.1, the framework first generates a path consisting of a random number of cells, which are connected to additional random cells as loadings. Using Monte-Carlo spice simulation, the transient-fault distributions are recorded along the path, which are later collected as test samples.

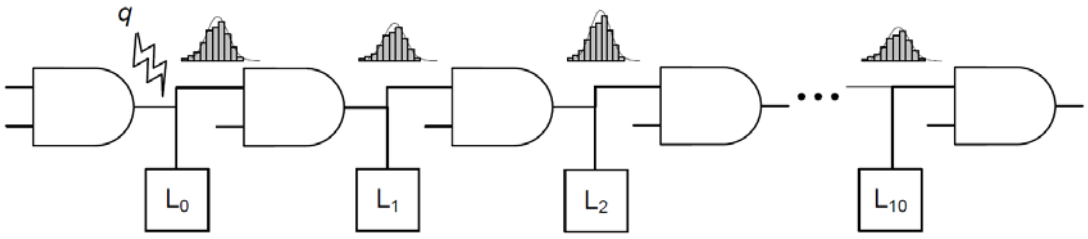


Figure 6.1: The framework for test sample generation

6.1 The table-lookup Monte-Carlo framework

6.1.1 Model accuracy

We build a series of pre-characterized tables for pulse width pw and voltage magnitude V_m with a total size of 9.5MB using about 1 month for data preparation and < 1 second for table construction according to Chapter 4. Used with samplings

and renewals, the tables are later verified with 10K test samples, where the results are presented and categorized according to cell and table types in Table 6.1. For pw tables, the results are better: the error rates for T^{μ}_{strike} and T^{σ}_{strike} are within 0.5%, whereas the error rates for T^{μ}_{prop} and T^{σ}_{prop} are up to 7.4%. For V_m tables, however, the error rates for T^{μ}_{strike} and T^{σ}_{strike} are around 3.0%, whereas the error rates for T^{μ}_{prop} and T^{σ}_{prop} are up to 23.7%. Note that in the table-lookup framework, V_m is also one of the indexing variables of pw tables. Therefore, when used in this framework, V_m tables' higher error rates will also affect the lookup of pw tables.

Table 6.1: Summary of table error rate

(a) V_m table error rate

	error rate (%)			
Cell	T^{μ}_{strike}	T^{σ}_{strike}	T^{μ}_{prop}	T^{σ}_{prop}
NOT	3.0	2.2	10.7	22.8
AND	2.8	1.6	11.2	22.6
OR	2.9	1.6	11.6	23.7

(b) pw table error rate

	error rate (%)			
Cell	T^{μ}_{strike}	T^{σ}_{strike}	T^{μ}_{prop}	T^{σ}_{prop}
NOT	0.4	0.2	4.4	5.3
AND	0.3	0.2	4.2	6.2
OR	0.4	0.2	4.3	7.4

6.1.2 SSER computation

Both circuit SER and SSER are measured and compared. For SER, we use static SPICE simulation; for SSER, we use Monte Carlo SPICE simulation as well as t he proposed framework with (QMC) and without (MC) quasirandom sequences. Considering t he extremely long runtime of Monte Carlo SPI CE simulation (w/ 100 runs), we can only afford to perform tests on small circuits (i4, i6, i18 and c17), with the largest containing 7 gates, 12 strike nodes and 5 inputs. The runtime of the Monte-Carlo SP ICE simulation ranges from 8 hours to slightly more than one day. The runtime of our framework requires less than 1 second with an average of 10^6 speed-up.

Figure 6.2 compares the results from SPICE simulation and our table-lookup framework. The three facts are observed: (1) Considering 5% process variations, the SSER obtained by Monte Carlo SPICE simulation are 35% ~ 52% above the SER obtained by static SPICE analysis (indicated by the black bars). Since the process variation worsens the stability of circuits beyond the deep submicron era, statistical effect should be considered to avoid increasingly underestimated circuit SER. (2) The proposed MC and QMC frameworks yield very similar SSERs with each other where the mismatches are within 0.4%. This means that we can use t he faster QMC without serious accuracy degradation. (3) Compared to the results of Monte Carlo SPICE simulation, the proposed QMC framework has error rates of 2.5%, 0.8%, 2.9%, and 2.8%, respectively.

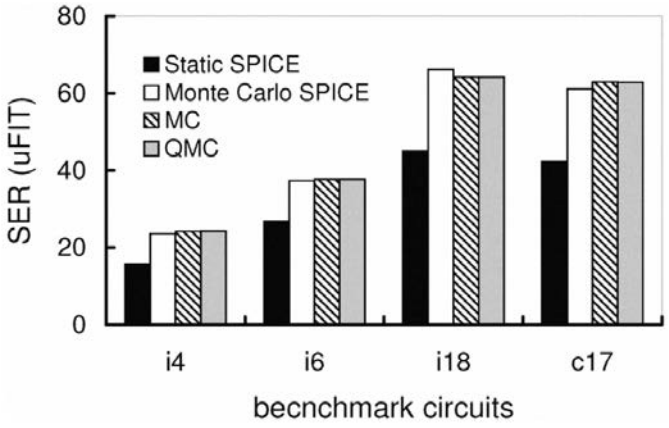


Figure 6.2: SSER comparison from static and Monte Carlo SPICE simulations, the proposed MC and QMC frameworks

Using the proposed MC/QMC frameworks, we conduct SSER analysis on a variety of circuits including the ones in Figure 6.2, the ISCAS'85 benchmark circuits, and a series of multipliers. Table 6.2 first lists the name, the total number of nodes, and the total number of outputs for each circuit. The following four columns report the SSER values and the runtime required by the MC and QMC frameworks, respectively. The last two columns compute the SER difference and speedup, respectively, by comparing results from the MC and QMC frameworks.

Table 6.2: Benchmark circuits, SER and runtime from the baseline MC and QMC frameworks

			MC		QMC		MC/QMC Comparison	
circuit	N_{node}	N_{po}	SSER (FIT)	T_{MC} (sec)	SSER (FIT)	T_{QMC} (sec)	SSER diff. (%)	speedup (X)
i4	4	1	24.22E-05	< 1	24.31E-05	< 1	0.37	-
i6	6	2	37.66E-05	< 1	37.65E-05	< 1	0.03	-
i18	12	3	64.26E-05	< 1	64.24E-05	< 1	0.02	-
c17	12	3	63.00E-05	< 1	62.89E-05	< 1	0.17	-
c432	233	7	1047.12E-05	114.37	1045.23E-05	30.43	0.18	3.76
c499	638	32	1150.61E-05	870.61	1161.77E-05	269.71	0.97	3.23
c880	443	26	1519.24E-05	173.23	1516.46E-05	36.90	0.18	4.69
c1355	629	32	1188.16E-05	891.80	1169.25E-05	273.20	1.59	3.26
c1908	425	25	1124.75E-05	365.07	1148.27E-05	109.25	2.09	3.34
c2670	841	157	3479.23E-05	401.02	3463.73E-05	120.23	0.45	3.34
c3540	901	22	2411.57E-05	1070.61	2395.72E-05	309.53	0.66	3.46
c5315	1806	123	9764.66E-05	818.22	9983.29E-05	403.17	2.2	2.03
c6288	2788	32	3860.03E-05	15703.05	3769.48E-05	4710.04	2.35	3.33
c7552	2114	126	6074.19E-05	1406.70	6098.10E-05	658.37	0.4	2.14
mul_4	158	8	883.38E-05	98.82	890.33E-05	34.85	0.79	2.84
mul_8	728	16	2127.35E-05	710.21	2094.05E-05	271.03	1.57	2.62
mul_16	3156	32	4775.07E-05	9565.03	4845.29E-05	5010.40	1.47	1.91
mul_24	7234	48	7636.46E-05	39628.50	7478.02E-05	29930.01	2.07	1.35
						Average	0.88	2.95

From Table 6.2, SSER is clearly related to the number of nodes and primary outputs of a circuit , which correspond to the possibility of the circuit struck by

radiation particles and the possibility of the transient faults observed at primary outputs, respectively. The runtime, however, depend on not only the number of strike nodes, but also the number of convolutions between nodes. SER difference is computed by $|SSER_{MC} - SSER_{QMC}|/SSER_{MC}$ and the average of 0.88% difference implies that the QMC and MC frameworks are of the same quality. For all benchmark circuits, the overall speedup brought by QMC is 2.95X in average.

Table 6.3: Benchmark circuits, SER from the baseline MC, QMC, and QMC-IS frameworks considering spatial correlations

	MC	QMC		QMC-IS	
circuit	SSER (FIT)	SSER (FIT)	SSER diff. (%)	SSER (FIT)	SSER diff. (%)
c432	897.37E-05	908.53E-05	1.24	905.01E-05	0.85
c499	1102.24E-05	1161.77E-05	0.97	1082.18E-05	1.82
c880	1199.94E-05	1193.65E-05	0.52	1191.71E-05	0.69
c1355	1111.32E-05	1127.01E-05	1.41	1087.1E-05	2.18
c1908	907.23E-05	917.83E-05	1.17	866.17E-05	4.53
c2670	2988.66E-05	2992.9E-05	0.14	2992.7E-05	0.14
c3540	2113.85E-05	2090.39E-05	1.11	2122.44E-05	0.41
c5315	7845.95E-05	7862.43E-05	0.21	7848.76E-05	0.04
c6288	3733.71E-05	3661.51E-05	2.35	3656.12E-05	2.08
c7552	5929.5E-05	6263.61E-05	5.63	5905.00E-05	0.41
m4	828.2E-05	829.74E-05	0.19	786.3E-05	5.06
m8	1973.04E-05	1988.19E-05	0.77	1977.49E-05	0.23
m16	4409.17E-05	4550.25E-05	3.20	4459.3E-05	1.14
m24	6927.18E-05	7109.2E-05	2.09	7036.49E-05	2.56
Average			1.59		1.68

Table 6.4: Benchmark circuits, runtime from the baseline MC, QMC, and QMC-IS frameworks considering spatial correlations

	MC	QMC		QMC-IS	
circuit	T_{MC} (sec)	T_{QMC} (sec)	speedup (X)	T_{QMC-IS} (sec)	speedup (X)
c432	145.20	44.76	3.24	31.04	4.68
c499	870.61	269.71	2.75	153.09	5.71
c880	174.43	49.62	3.51	31.93	5.46
c1355	913.07	280.46	3.26	198.36	4.60
c1908	341.71	139.59	2.45	103.46	3.30
c2670	463.91	142.52	3.26	96.11	4.83
c3540	1176.2	383.92	3.06	348.14	3.38
c5315	881.85	595.41	1.48	482.31	1.83
c6288	16111.8	4183.31	1.93	3671.84	4.39
c7552	1533.25	400.74	3.83	316.45	4.85
m4	114.23	47.65	2.4	37.159	3.07
m8	676.65	342.43	1.97	277.89	2.43
m16	9925.51	5636.89	1.76	2422.43	4.09
m24	37894.21	26687.6	1.42	10670.5	3.55
Average			2.55		3.72

Table 6.3 reports the SSER values required by the MC, QMC and QMC-IS (QMC + importance sampling) frameworks considering spatial correlation, respectively. The last column compute the SSER difference, by comparing results from the MC frameworks considering spatial correlation. Moreover, Table 6.4 reports

the runtime required by the MC, QMC and QMC-IS (QMC + importance sampling) frameworks considering spatial correlation, respectively. The last column computes the speedup, by comparing results from the MC frameworks considering spatial correlation. The average difference between MC and QMC-IS is 1.68%. That indicates that the QMC-IS and MC frameworks are of the same quality. And From Table 6.4, for all benchmark circuits, the overall speedup brought by QMC is 2.55X in average. For all benchmark circuits, the overall speedup brought by QMC-IS is 3.72X in average.

6.2 The support-vector-regression framework

6.2.1 Model accuracy

We also build the SVR models for three cells with four charge strength levels. Assuming a 5% process-variation, each model is trained with 10K training samples. Then, we examine these models' accuracy and compression ratio using another 10K test samples.

The mean error rates and compression ratios are first categorized according to model and cell types in Table 6.5. Three messages are observed. (1) All mean error rates and compression ratios of $\delta^{\mu}_{\text{strike}}$, $\delta^{\mu}_{\text{prop}}$, and $\delta^{\sigma}_{\text{prop}}$ models are below 4% and 4.5%, respectively. Hence, we found these models accurate and compact. (2) $\delta^{\sigma}_{\text{strike}}$ models have error rates and compression ratios around 13% and 0.4%, respectively. This type of model is less accurate and smaller, which means the behavior of $\delta^{\sigma}_{\text{strike}}$ may not be fully explained by its current input variables. (3) Among different cells, NOT has the largest mean compression ratio whereas OR has the smallest. It means that NOT models generally have a more complex behavior than OR models.

Table 6.5: Model quality w.r.t. model type

error rate (%)				
Cell	δ^{μ}_{strike}	δ^{σ}_{strike}	δ^{μ}_{prop}	δ^{σ}_{prop}
NOT	2.0	12.9	3.7	3.8
AND	2.8	12.0	2.4	3.9
OR	2.6	11.9	3.3	3.7
compression ratio (%)				
Cell	δ^{μ}_{strike}	δ^{σ}_{strike}	δ^{μ}_{prop}	δ^{σ}_{prop}
NOT	2.7	0.4	4.4	1.2
AND	2.4	0.3	1.1	0.9
OR	1.4	0.3	0.4	1.2
training time (sec.)				
Cell	δ^{μ}_{strike}	δ^{σ}_{strike}	δ^{μ}_{prop}	δ^{σ}_{prop}
NOT	273.0	1293.3	706.5	310.5
AND	1329.7	1373.3	1057.4	314.3
OR	1478.5	1341.3	1149.6	286.3

Table 6.6 shows the accuracy of the built models, including three types. The error rates of all proposed models are less than those from (Table 6.5). The error rates of sigma values for the generated models reduced significantly from 12% to 4%. Such result states that the effectiveness of the intensified SVM learning and data reconstruction collectively provide better quality models for further SER estimation.

Table 6.6: Model quality w.r.t. model type constructed by intensified SVM learning

Error Rate (%)				
Cell	μ_{first}	σ_{first}	μ_{prop}	σ_{prop}
INV	0.38%	4.45%	1.66%	2.42%
AND	0.39%	3.91%	1.09%	2.27%
OR	0.44%	3.95%	1.51%	2.05%

6.2.2 SSER computation

Figure 6.3 compares the SER analysis results where three facts are observed: (1) under 5% process-variation, the SER obtained by Monte-Carlo SPICE simulation are 35% to 52% above that obtained by static SPICE analysis. Since the process variations worsen the stability of circuits beyond deep sub-micron regime, statistical analysis methods should be used to avoid increasingly underestimated circuit SER. (2) The table-lookup framework underestimates t4, t18 and c17 but overestimates t6 meanwhile with the maximum error difference being 26.27%. (3) The SVR-learning framework yields SER's slightly above the result using Monte-Carlo SPICE simulation and the maximum difference is < 9.0%.

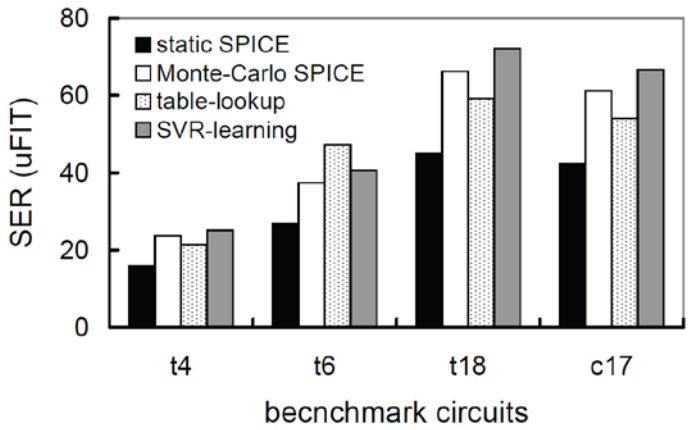


Figure 6.3: Soft error rate comparison between static SPICE simulation, Monte-Carlo SPICE simulation and the proposed frameworks

To more closely investigate the SER difference between static and statistical analysis, we breakdown the results in Figure 6.3 by charge strength levels, and present the results in Figure 6.4. Comparing the results between static and Monte-Carlo SPICE simulations across all test circuits, it is observed that the results of the two SPICE simulations and the two proposed frameworks are very similar for Q1 ~ Q3 parts (difference < 5%). For the Q0 part indicated by the white bars, however, the static SPICE simulation constantly underestimates the SER. The table-lookup framework performs better than the static SPICE simulation but worse than the SVR-learning framework. Overall, the SVR-learning framework can give slightly larger but closer (and more stable) results as Monte-Carlo SPICE simulation.

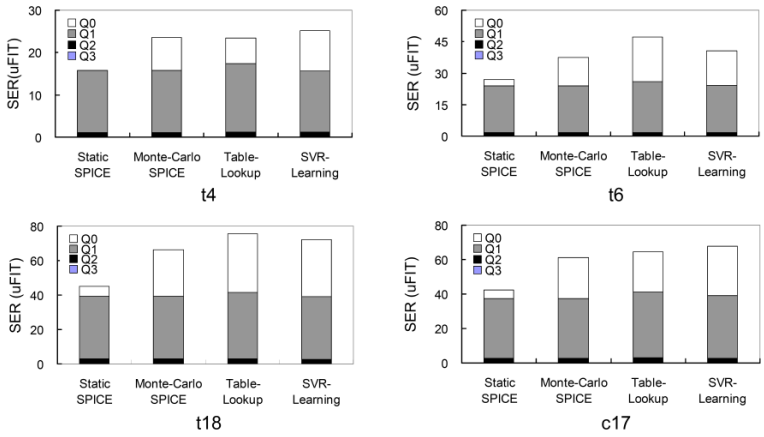


Figure 6.4: SER breakdown by charge strength

To further investigate the 9% SER over-estimation of the SVR learning framework, one transient fault along a path is particularly identified in Figure 6.5. The X-axis and Y-axis denote the propagation level and the standard deviation of the pulse width (σ_{pw}) of this transient fault, respectively. After two propagations, the σ_{pw} drops sharply and has not yet been fully captured by the current learning model. This behavior does not seem to correlate to any of our existing input variables, and caused larger SER estimations according to Equation (2) and Figure 2.2. Such an issue will be another topic worth exploration.

Since running Monte-Carlo SPICE simulation with process variations for large circuits will be prohibitively time-consuming, we can only run both frameworks on large benchmark circuits. However, the entire set of circuits ISCAS'85 benchmark circuits, and a series of multipliers. Table 6.7 first lists the name, the total number of nodes, the total number of outputs, and the total number of predictions for each circuits. The latter columns in the table report the SER and runtime from both the

table-based and the SVR-learning frameworks. Accordingly, SER is clearly proportional to the number of nodes and primary outputs of a circuit, which correspond to the possibility of the circuit struck by radiation particles and the possibility of the resulting transient faults observed in primary outputs, respectively. The runtime, however, does not only depend on the number of strike nodes, but also depend on the number of convolutions between these nodes. For example, c3540 (an ALU with control) has fewer nodes than c5315 (another ALU), whereas its runtime is larger. This property is also observed from the large runtime of multiplier circuits, in which every primary output depends on each primary input. Finally, the SVR-learning framework runs faster than the table-based framework by 11.8X-70.0X, with an average of 28.8X.

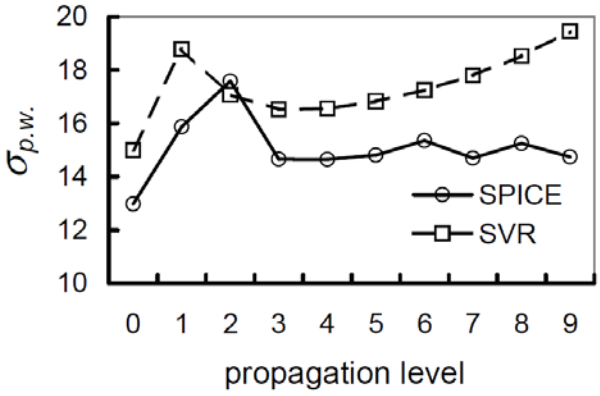


Figure 6.5: σ_{pw} propagation along a path

Table 6.7: Benchmark circuits, SER and runtime from the baseline MC and SVR frameworks

circuit	N_{node}	N_{po}	N_{pred}(k)	table-lookup (tbl) SER(FIT)	table-lookup (tbl) time(s)	SVR-learning (svr) SER(FIT)	SVR-learning (svr) time(s)	tbl/svr spdup(X)
t4	4	1	0.1	2.18E-05	0.2	2.52E-05	< 0.01	>20.0
t6	6	2	0.2	4.73E-05	0.3	4.06E-05	< 0.01	>30.0
t18	12	3	0.4	6.05E-05	0.7	7.21E-05	< 0.01	>70.0
c17	12	3	0.5	5.31E-05	0.7	6.66E-05	< 0.01	>70.0
c432	233	7	362.5	1.25E-04	114.4	1.48E-04	5.9	19.4
c499	638	32	2939.3	1.15E-04	870.6	1.59E-04	42.9	20.3
c880	443	26	402.5	1.52E-04	173.2	2.18E-04	6.1	28.4
c1355	629	32	3013.2	1.19E-04	891.8	1.36E-04	43.5	20.5
c1908	425	25	1240.3	2.12E-04	365.1	2.27E-04	18.4	19.8
c2670	841	157	570.8	3.48E-04	401.0	3.40E-04	9.6	41.8
c3540	901	22	3142.4	7.41E-04	1070.6	6.67E-04	39.8	26.9
c5315	1806	123	2272.2	1.15E-03	818.2	1.09E-03	35.1	23.3
c6288	2788	32	43776.4	6.86E-04	15703.1	8.45E-04	501.5	31.3
c7552	2114	126	3704.8	1.04E-03	1406.7	8.89E-04	97.4	14.4
mul_4	158	8	145.4	1.58E-04	98.8	1.79E-04	2.4	60.6
mul_8	728	16	2960.3	4.14E-04	710.2	6.06E-04	45.1	15.7
mul_16	3156	32	52348.1	1.48E-03	9565.0	1.47E-03	784.7	12.2
mul_24	7234	48	273008.7	2.63E-03	39628.5	2.35E-03	3553.2	11.2
mul_32	13017	64	890360.5	2.82E-03	131535.6	3.21E-03	11142.1	11.8
							Average	28.8

6.3 The closed-form analysis framework

6.3.1 Model accuracy

Figures 6.6 and 6.7 compare the results from the probability density function (PDF) of transient faults induced by four particles of different charge strength in the proposed models and those of Monte-Carlo SPICE simulation for one AND gate and one OR gate, respectively. The solid line represents the PDF results of the Monte-Carlo simulation while the PDF results from our models are denoted by a dotted line. The means by which PDF results are derived using our models are very close to those derived using Monte-Carlo SPICE simulation, while the variances of PDF results derived by our models are slightly smaller (6.76% on average).

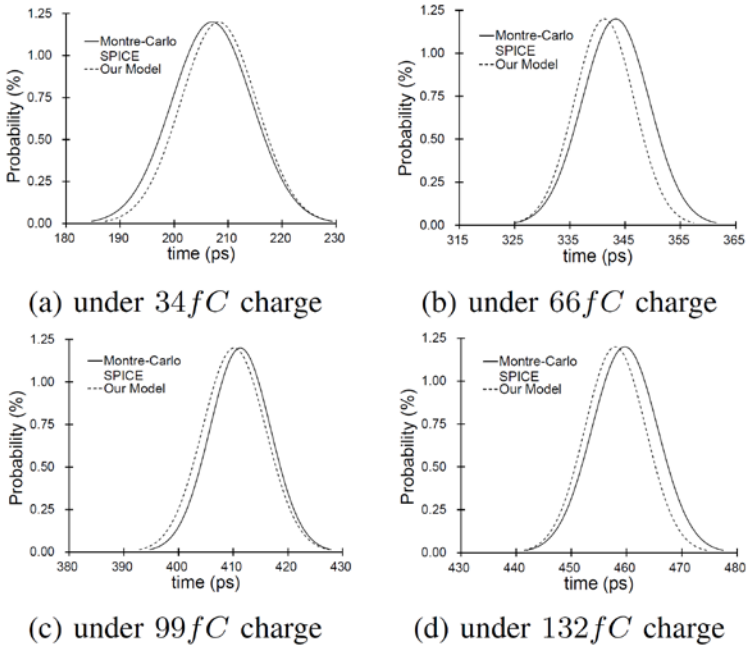
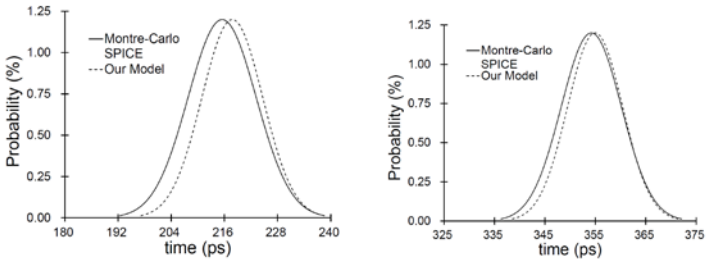


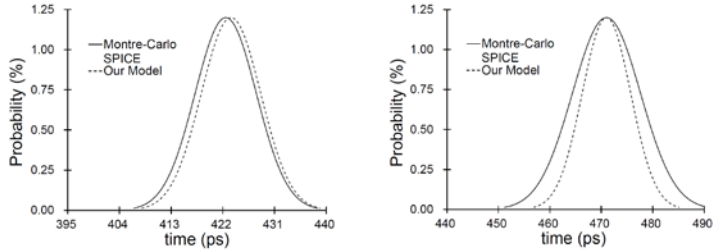
Figure 6.6: Model accuracy of AND gates

Table 6.8 summarizes the accuracy of the first-hit models and propagation models. The first column lists the name of the cell libraries, and the following four columns denote the mean and variance errors of first-hit models and those of the propagation models, respectively. The average mean and variance errors of our first-hit model are all less than 2%, as is the average mean error of the propagation models. The reason that the variance error associated with the propagation models is worse is that the shape of the hitting pulse becomes irregular during propagation. As shown in Figure 6.8, because the sinusoidal shape of a hitting pulse is transformed into a trapezoid, the variance of the flat part (like f_1 and f_2) of the trapezoid is hardly

considered in the proposed framework, leading to an underestimation of variance.



(a) under $34fC$ charge (b) under $66fC$ charge



(c) under $99fC$ charge (d) under $132fC$ charge

Figure 6.7: Model accuracy of OR gates

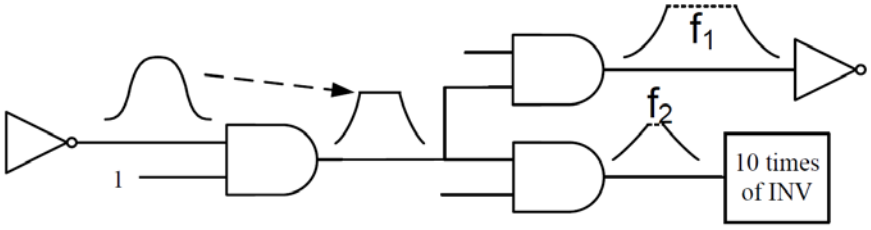


Figure 6.8: Explanation for variance errors

Table 6.8: Summary of model error

error (%)				
cell	ψ^{μ}_{hit}	ψ^{σ}_{hit}	ψ^{μ}_{prop}	ψ^{σ}_{prop}
INV	-0.42	-1.29	0.15	-4.76
AND	-0.37	-0.96	1.96	-6.98
OR	-0.52	-3.46	1.85	-8.55
Average	-0.43	-1.90	1.32	-6.76

6.3.2 SSER computation

Figure 6.9 compares the SER analysis results of five circuits (t1, t2, t3, c17, and Adder_{2bit}). Our findings lead to two conclusions: (1) The SVR-learning framework does not typically yield results of satisfactory accuracy for SER compared to those using Monte-Carlo SPICE simulation due to a lack of quality models. Moreover, the 16% difference in the result of two-bit adder (Adder_{2bit}) is due to reconvergence,

which was not considered in that framework. (2) The proposed closed-form SSTA-based framework yields more accurate SERs with differences of less than 3%, demonstrating that the proposed idea is capable of achieving superior accuracy. In addition, the results of $Adder_{2bit}$ were quite accurate, despite the inclusion of many reconvergence fanout nodes, demonstrating the effectiveness of our reconvergence handling strategy.

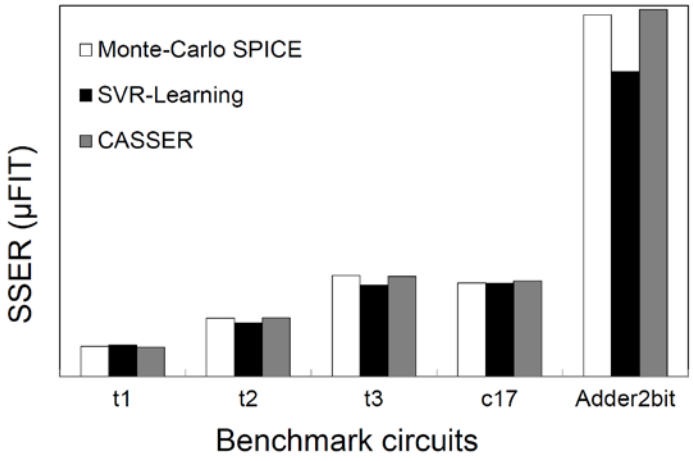


Figure 6.9: Soft error rate comparison between Monte-Carlo SPICE simulation and this framework (CASSER)

Information related to other benchmark circuits and their SSER results as well as runtimes derived using the two methods are listed in Table 6.9. Columns 1 to 5 denote the name of each circuit, the number of gates, the number of primary inputs (PI), the number of primary outputs, and the max topological level, respectively. The remaining four columns show more SSER results and runtimes derived by SVR-learning framework and the proposed framework on a variety of circuits, respectively. The last column computes the improvement in timing cost. The last six test cases were aborted because the runtime exceeded one day. The runtime of each test case using this framework was less than ten minutes except for bench7 and approximately half of the test cases were completed in one second. In addition, the timing cost grows slowly even if the circuit size grows rapidly, while that of the SVR-learning method increases rapidly as the circuit size increases. The runtime of this framework was approximately 286 times faster than that of the SVR-learning method. Moreover, because the proposed idea is built upon a closed-form SSTA-like analysis, the longer logic depth will induce a longer runtime. For this reason, c6288 and some multipliers (mul_16 to mul_32)) required a slightly longer runtime.

Table 6.9: SSER measurement of various benchmark circuits

					SVR-learning		this framework		
Circuit	$\#_{gate}$	$\#_{PI}$	$\#_{PO}$	Lv_{max}	SSER (μFIT)	time (sec)	SSER (μFIT)	time (sec)	speedup (X)
c432	233	36	7	30	5.85×10^3	24.00	1.27×10^4	0.08	300
c499	638	41	32	28	5.77×10^3	164.01	6.14×10^3	0.61	268
c880	433	60	26	33	7.26×10^3	24.05	1.22×10^4	0.11	218
c1355	629	41	33	30	6.19×10^3	164.11	9.35×10^3	0.60	273
c1908	425	33	25	39	9.18×10^3	68.00	1.60×10^4	0.34	200
c2670	872	157	64	38	1.22×10^4	40.12	1.64×10^4	0.17	235
c3540	901	50	22	52	2.58×10^4	180.02	3.28×10^4	0.68	265
c5315	1833	178	123	41	3.51×10^4	208.41	5.03×10^4	0.60	347
c6288	2788	32	32	122	3.74×10^4	3108.52	1.80×10^5	8.92	348
c7552	2171	207	108	60	3.33×10^4	308.31	7.38×10^4	0.64	481
mul_4	158	8	8	23	5.75×10^3	12.00	6.10×10^3	0.04	300
mul_8	728	16	16	50	2.48×10^4	164.93	6.73×10^4	0.56	293
mul_16	3156	32	32	105	7.79×10^4	3208.38	5.11×10^5	13.49	238
mul_24	7234	48	48	155	1.58×10^5	16132.57	1.45×10^6	70.59	228
mul_32	13017	64	64	194	-	-	2.74×10^6	304.37	-
bench2	110539	3975	3935	15	-	-	3.32×10^5	144.93	-
bench3	242347	5705	5661	20	-	-	8.84×10^5	449.12	-
bench4	49858	2429	2409	13	-	-	1.51×10^5	36.00	-
bench7	899618	17871	17823	22	-	-	4.38×10^6	7798.82	-
bench8	105334	4738	4718	19	-	-	3.04×10^5	162.61	-
								average	286

Chapter 7
Conclusion

Traditional SER analysis techniques try to mimic the results of static SPICE simulation. However, static analysis tends to increasingly underestimate true SER's in the presence of process variations, especially for nanometer CMOS designs. Therefore, we first examined the soft-error effect beyond deep sub-micron technologies considering process variations. From the statistical point of view, we found that transient faults are not always diminishing in pulse width after propagation and may even become larger when reaching flip-flops. We also showed that soft errors originated from particle strikes with small charges can easily escape from the traditional static analysis.

To cope with these sophisticated issues, a table-lookup Monte-Carlo framework, a SVR-learning framework, and SSTA-like framework are proposed, respectively. The first framework captures the change of transient-fault distributions implicitly using the Monte-Carlo method, whereas the second does the same task explicitly using Support Vector Regression. And the third framework considers both efficiency and accuracy simultaneously, this framework includes a novel idea for SSER analysis, in which a transient pulse is partitioned into two transition signals (one is rising transition and the other is falling transition). Because the two signals are expressed as timing quantities in closed-form, they can be analyzed using a block-based SSTA-like method, which considers the correlation of timing.

Experimental results show that all our frameworks are capable of more accurately estimating SERs when comparing to the static SPICE simulation. Moreover, the SVR learning framework outperforms the table-lookup framework in terms of both SER accuracy and runtime. The runtime of SSTA-like framework is about 286 times faster than that of a SVR-learning framework.

Statistical soft error rate (SSER) is an emerging topic. As the IC technology keeps evolving beyond deep sub-micron, we envision SSER analysis to become increasing critical for reliable scaled designs. As more and more circuit design projects are dedicated to automotive and biomedical applications, the circuit reliability issue are more and more important. Soft error has also been put into the specification

of car manufacturing process. Zero-defect is not only an expectation but becomes the standard in the near future. As a result, more directions of SSER research need to be investigated soon, including: (1) deriving more accurate learning models for σ_{pw}, (2) developing a faster Monte-Carlo framework with high accuracy and (3) applying to statistical circuit optimization.

References

[1] P. Shivakumar, M. Kistler, S. W. Keckler, D. Burger, and L. Alvisi, “Modeling the effect of technology trends on the soft error rate of combinational logic,” In Proc. Int’l Conf. Dependable Systems and Networks. 389–398, 2002.

[2] P. E. Dodd, and L. W. Massengill, “Basic mechanisms and modeling of single-event upset in digital microelectronics,” IEEE Tran. Nuclear Science 50, 3, 583–602, 2003.

[3] O. A. Amusan , L. W. Massengill , B. L. Bhuva, S. Dasgupta, A. F. Witulski , and J.R. Ahlbin, “ Design techniques to reduce set pulse widths in deep-submicron combinational logic,” IEEE Tran. Nuclear Science 54, 6, 2060–2064, 2007.

[4] H. Cha and J. H. Patel, “A logic-level model for α particle hits in cmos circuits,” In Proc. Int’l Conf. Circuit Design, pages 538–542, Aug 1993.

[5] Y. Tosaka, H. Hanata, T. Itakura, and S. Satoh, “Simulation technologies for cosmic ray neutron-induced soft errors: models and simulation systems,” IEEE Tran. Nuclear Science, 46(3), 774–780, Jun 1999.

[6] M. Omana, G. Papasso, D. Rossi, and C. Metra, “A model for transient fault propagation in combinational logic,” In Proc. Int’l On-Line Testing Symp., pages 111–115, 2003.

[7] R. Garg, C. Nagpal, and S. P. Khatri, “A fast, analytical estimator for the seu-induced pulse width in combinational designs.” In Proc. Design Automation Conf., pages 918–923, Jul 2008.

[8] M. Zhang and N. Shanbhag, “A soft error rate analysis (sera) methodology,” In Proc. Int’l Conf. Computer Aided Design, pages 111–118, Nov 2004.

[9] B. Zhang, W.-S. Wang, and M. Orshansky, “Faser: fast analysis of soft error susceptibility for cell-based designs,” In Proc. Int’l Smyp. Quality Electronic Design, pages 755–760, Mar 2006.

[10] R. Rajaraman, J. S. Kim, N. Vijaykrishnan, Y. Xie, and M. J. Irwin, “Seat-la: a soft error analysis tool for combinational logic,” In Proc. Int’l Conf. VLSI Design, pages 499–502, Jan 2006.

[11] R. Rao, K. Chopra, D. Blaauw, and D. Sylvester, “An efficient static algorithm for computing the soft error rates of combinational circuits,” In Proc. Design Automation and Test in Europe Conf., pages 164–169, March 2006.

[12] S. Mukherjee, M. Kontz, and S. Reihardt, “Detailed design and evaluation of redundant multi-threading alternatives,” In Proc. Int’l Symp. Computer Architecture, pages 99–110, May 2002.

[13] W. Bartlett and L. Spainhower, “Commercial fault tolerance: a tale of two

systems," IEEE Tran. Dependable and Secure Computing, 1(1):87–96, Jan-Mar 2004.

[14] S. Mitra, N. Seifert, M. Zhang, Q. Shi, and K. S. Kim, "Robust system design with built-in soft error resilience," IEEE Tran. Computer, 38(2):43–52, Feb 2005.

[15] M. Zhang, T. Mak, J. Tschanz, K. Kim, N. Seifert, and D. Lu, "Design for resilience to soft errors and variations," In Proc. Int'l On-Line Test Symp., pages 23–28, Jul 2007.

[16] K. Mohanram, "Closed-form simulation and robustness models for seu-tolerant design," In Proc. VLSI Test Symp., pages 327–333, May 2005.

[17] S. Krishnaswamy, I. Markov, and J. P. Hayes, "On the role of timing masking in reliable logic circuit design," In Proc. Design Automation Conf., pages 924–929, Jul 2008

[18] N. Miskov-Zivanov and D. Marculescu, "Mars-c: modeling and reduction of soft errors in combinational circuits," In Proc. Design Automation Conf., pages 767–772, Jul 2006.

[19] K. Bowman, S. Duvall, and J. Meindl, "Impact of die-to-die and within-die parameter fluctuations on the maximum clock frequency distribution for gigascale integration," IEEE Jour. Solid-State Circuits, 37(2):183–190, Feb 2002

[20] S. Borkar, T. Karnik, S. Narendra, J. Tschanz, A. Keshavarzi, and V. De, "Parameter variations and impact on circuits and microarchitecture," In Proc. Design Automation Conf., pages 338–342, Jul 2003.

[21] S. Natarajan, M. Breuer, and S. Gupta, "Process variations and their impact on circuit operation," In Proc. Int'l Symp. Defect and Fault Tolerance in VLSI Systems, pages 73–81, Nov 1998.

[22] K. Ramakrishnan, R. Rajaraman, S. Suresh, N. Vijaykrishnan, Y. Xie, and M. J. Irwin, "Variation impact on ser of combinational circuits," In Proc. Int'l Smyp. Quality Electronic Design, pages 911–916, 2007.

[23] N. Miskov-Zivanov, K.-C. Wu, and D. Marculescu, "Process variability-aware transient fault modeling and analysis," In Proc. Int'l Conf. Computer Aided Design, pages 685–690, Nov 2008.

[24] Nanoscale Integration and Modeling Group 2008. Predictive Technology Model. Nanoscale Integration and Modeling Group. Available at http://www.eas.asu.edu/ ptm/.

[25] V. Ferlet-Cavrois, P. Paillet, D. McMorrow, N. Fel, J. Baggio, S. Girard, O. Duhamel, J.S. Melinger, M. Gaillardin, J.R. Schwank, P.E. Dodd, M.R. Shaneyfelt, and J.A. Felix, "New insights into single event transient propagation

in chains of inverters-evidence for propagation-induced pulse broadening," IEEE Tran. Nuclear Science 54, 6, 2338–2346, 2007.

[26] H. Edamatsu, K. Homma, M. Kakimoto, Y. Koike, and K. Tabuchi, "Pre-layout delay calculation specification for cmos asic libraries," In Proc. Asian South Pacific Design Automation Conf. (ASP-DAC). 241–248, 1998.

[27] S. Weisberg. Applied Linear Regression, 3rd Edition. John Wiley and Sons, 2005.

[28] D. M. Bates and D. G. Watts. Nonlinear Regression Analysis and Its Applications. John Wiley and Sons, 1988.

[29] V. N. Vapnik. The nature of statistical learning theory. Springer-Verlag New York, Inc., New York, NY, USA, 1995.

[30] A. J. Smola, B. Scholkopf, and B. S. Olkopf. A tutorial on support vector regression. Technical report, Statistics and Computing, 2003.

[31] N. Cristianini and J. Shawe-Taylor. An Introduction to Support Vector Machines and Other Kernel-based Learning Methods. Cambridge University Press, 2002.

[32] J. Kennedy, and R. Eberhart, "Particle swarm optimization," Proc. Intl Conf. Neural Network, pp. 1942-1948, 1995.

[33] C. Visweswariah et al., "First-Order Incremental Block-Based Statistical Timing Analysis," in Proc. Design Automation Conf. (DAC), pp. 331 -336, 2004.

[34] C. E. Clark, "The greatest of finite set of random variables," in Operation Research, pp. 145-162, March-April 1961.

[35] M. Cain, "The moment-generating function of the minimum of bivariate normal random variables," in The American Statistician, vol. 48, pp. 124-125, May 1994.

國科會補助專題研究計畫成果報告自評表

請就研究內容與原計畫相符程度、達成預期目標情況、研究成果之學術或應用價值（簡要敘述成果所代表之意義、價值、影響或進一步發展之可能性）、是否適合在學術期刊發表或申請專利、主要發現或其他有關價值等，作一綜合評估。

1. 請就研究內容與原計畫相符程度、達成預期目標情況作一綜合評估
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3. 請依學術成就、技術創新、社會影響等方面，評估研究成果之學術或應用價值（簡要敘述成果所代表之意義、價值、影響或進一步發展之可能性）

   由於近年來在先進的電路設計上軟性錯誤被發現的頻率越來越高，商業電子產品的可靠度有了新的挑戰。而製程變異使得軟性電子錯誤變得難以分析，本計畫成功地研究了在深次微米時代下，軟性電子錯誤率的行為。不僅發現了在製程變異下，軟性電子錯誤率的行為與以往傳統上的分析不同，且於本計畫也建立了三種架構來分析在製程變異下軟性電子錯誤率的複雜行為。此三種架構分別為 1)蒙地卡羅分析(Monte-Carlo)架構 2)機器學習(machine learning)分析架構 3)閉合模式(closed-form)分析架構。此三種架構各有其優缺點，在蒙地卡羅分析架構中，提供了相當高的準確率來預測軟性電子錯誤率之行為，但其缺點為所需計算時間也較長。而閉合模式分析架構中，提供了相當快的計算，但其精準度就稍微差了一點。而機器學習分析架構中，其運算速度及精準度都介於蒙地卡羅分析架構及閉合模式分析架構之間。

未來，將可以透過此三種分析架構進行軟性電子錯誤率設計最佳化，設計工程師可依其所需選取適合之分析架構，並經由這些分析架構中獲得一些容錯設計的建議，藉此強化原先電路設計中的弱點或者架構中需要修正的特性以期達成相容的功能性。功率及效能因素也將會在這個階段一併被考量以其達成系統穩健性的最佳化。

是故，過去三年的研究成果中，由於過去的研究只針對電路對輻射干擾的抵抗性配合製程變異做分析，無法計算其全晶片錯誤率。於是在本實驗室成功地運用物理模型結果與計算智能模型化技術，在高品質國際期刊(TODAES)發表了全世界第一篇針對於製程變異對積體電路地軟性電子錯誤率估計的論文，並提出統計性軟性電子錯誤率(Statistical Soft Error Rate, SSER)的概念，希冀能誘發更多研究能量的投入。目前更進一步地準備分析空間關係性(spatial correlation)與全電量分布(full-spectrum charge collection)對電路設計的影響。

尤其當越來越多的積體電路要使用於車載或生醫相關零件時，可靠度的要求就更高。在圖 4.3 中，SIA (Semiconductor Industry Association) 對可靠度的預估的里程碑對 IC 長期故障率(Long Term Failure Rate) 從過去的幾十個 FIT(Failure in Time, Failure unit, or Failure instance/Time)降到目前只有數個 FIT(甚至希望零瑕疵)。國際車用電子協會(Automotive Electronics Council)也因此把軟性錯誤率的分析納入其最新的設計規範(AEC-Q100-Rev-G)當中。而更如圖 4.4 所示，日本車廠在追求汽車的可靠度上普遍優於歐美國家的車商。而以國內大廠 TSMC 而言，到 2010 年也才有了符合車用電子的半導體製程技術，可見其積體電路可靠度的困難度。本主持人未來將以車載專用的 CAN 控制設計為基礎，發展以零瑕疵為目標的軟性電子錯誤率最佳化方法，並融合其他設計可靠度/可製造性/可測性等對車載與生醫電路影響做全面分析。

行政院國家科學委員會補助國內專家學者出席國際學術會議報告

民國 100 年 10 月 01 日

附件三

報告人姓名	溫宏斌	服務機構及職稱	交通大學電機工程學系 助理教授
會議時間 會議地點	September 16-24, 2011 Anaheim, CA, U.S.A.	本會核定補助文號	計畫編號 NSC99-2220-E-009-011-
會議名稱	(中文) 2011 國際測試研討會 (英文) 2011 International Test Confernce		
發表論文題目	(中文) 以測試向量產生方法診斷導線開放缺陷 (英文) Diagnosing Interconnect Open Defects with Test-Pattern Generation		

報告內容應包括下列各項：

一、參加會議經過

國際測試研討會(ITC) 一向都是積體電路設計領域最頂尖的國際研討會之一。今年 2011 ITC 選在美國加州的 Disneyland Hotel 舉辦，為其總共四天。其中共收錄五十餘篇論文與二十九篇海報論文，主要來自國際上知名的積體電路設計大廠，如 Intel、AMD、IBM 與 Freescale。除了全程參與所有的 technical session，包含 Defect-oriented and Power-aware ATPG、Small-Delay Faults、Self-testing and Test Compression Techniques、Defects in advanced technology、Timing-and Power-aware DFT、Microprocessor testing、以及 Learning from data: diagnosis and data-mining。許多的論文報告都與我目前所從事的研究領域 ATPG 與 defect diagnosis 密切相關，而且與會的過程中聆聽到現在業界在驗證與測試上問題深入的討論，受益匪淺。並且，在我自己這次論文報告過程中，能與 Ken Bulter、Krishnendu Chakrabarty、Michael S. Hsiao 與 Magdy Abadir 等美加等地他校與業界 Verification & Test 先進教授學者直接討論，也獲得 Mentor Graphics 與 Synopsys 等公司的興趣。其中，由於我今年第一次參與海報論文報告，與會討論狀況更是熱烈。大會議程主席 Shawn Blanton 在我們的海報成果前與我們交換意見達半個小時之久。另外更有 nvidia 與 Mentor Graphics 與 Synopsys 等公司 ATPG 研究人員對於我們提出的技術表達興趣，深入想了解如何把我們提出的方法可以應用在該公司商用環境上，也啟發我們下一階段研究方想，實屬難得。

二、與會心得

ITC 涵概研究領域創新，邀請的講者也夠具知名度。今年本會參與人數與參業界代表還較歷年上升約 800 人，technical session 中參與人數，討論比往常熱烈許多。其中，Defects in advanced technology 場次更是坐無虛席，最後我是站著聽完整場論文報告。另外，在我報告的 poster 討論中，聽眾族群以其不同的背景，提出了對我們 Diagnostic ATPG 許多建設性的建議(包含如何修正問題設定使其更貼近真實面等)，也讓我們的研究方法更能拓廣其可實用性(包含如何與現有 Fastscan/Flextest 或是 TetraMax ATPG 做整合)。整體而言收穫許多，也推薦其他國內研發人員可以多透過海論論文形式與國際學者業界先進多做交流。

以下附上海報展示實照：

三、建議

此次大會附帶舉辦的多場 Embedded Tutorials，其中 Testing Low-Power Integrated Circuits: Challenges, Solutions, and Industry Practices 討論了先進製程上的積體電路功率的測試問題,提供想要進入該領域的研究人員一個很好的綜觀瞭解。以後只要經費許可，應多國內鼓勵老師學生積極參與，拓展我們的研究視野。此外，讓從事 EDA/Testing 的學生在全英文的學術環境與產學界專業人士共同討論可以激勵其對研究工作的嚮往與動力，並擴展國際之間交流。

四、攜回資料名稱及內容

會議論文集光碟片

溫宏斌 <opwen@g2.nctu.edu.tw>

Your ITC Poster has been Accepted

Bill Eklow (beklow) <beklow@cisco.com> **2011年6月28日上午12:34**
收件者: opwen@g2.nctu.edu.tw

Hi Charles,

Congratulations! Your poster has been accepted for presentation at this year's ITC Poster Session. Your poster number is: 17. This year's selection process was very competitive with many submissions and much higher quality than in previous years. The selection of your poster into this year's session is a significant achievement. The Poster Session will be held this year on Wednesday, September 21 from noon to 2 PM in the Exhibits Hall. This year we will be including accepted posters in the presentation CD (Power Point or PDF format). Abstracts and posters will also be posted on the ITC web site after the conference has concluded.

You will be getting a formal letter and instructions for submitting and presenting your final poster shortly. In the mean time, please confirm via reply to this email that you are willing and able to present at the poster session on September 21.

Congratulations again and best regards,

Bill Eklow.

ITC General Chair

Diagnosing Interconnect Open Defects With Test-Pattern Generation

Yen-Hou (Ian) Chen, Chia-Ling (Lynn) Chang, Jerry C.-Y. Ku and Charles H.-P. Wen
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***Abstract*—As an open occurs on a wire segment as a defect in the circuit, the Byzantine effect originated from the coupling wires of the physical layout and the cell library result in complicated faulty behaviors. Many previous researches focus on developing the test and diagnosis methods for open defects while the issue of pattern quality has not been well-addressed. Therefore, in this paper, a high-resolution diagnostic framework is proposed and combines (1) a diagnostic test pattern generation (DTPG) and (2) a diagnosis flow. A precise diagnosis flow generates the list of defect candidates in a dictionary-based fashion followed by an inject-and-evaluate analysis with physical information to greatly reduce the candidate size for future silicon inspection. Experimental results show that the proposed framework runs efficiently and deduces nearly one candidate for each open-segment defect on ISCAS85 benchmark circuits.**

I. BACKGROUND

Open defects - the unintended breaks or electrical discontinuities in IC interconnect lines - are common defects frequently discussed in VLSI testing beyond deep submicron era. Along with the scaling of the manufacturing process, the distance between interconnects becomes narrower and thus induces more neighboring wires. As a result, when an open defect occurs in one wire segment, its coupling condition is more complicated. To properly model the defect behaviors, the Byzantine effect [1][2] needs to be considered and states that the voltages of driven gates connecting an open segment are determined by comparing their threshold voltages and the floating voltage determined by its coupling condition. Figure 1 shows the Byzantine effect of interconnect opens.

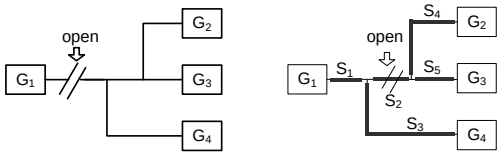

Fig. 1: The Byzantine effect of an interconnect open

II. A HIGH-RESOLUTION DIAGNOSTIC FRAMEWORK

A high-resolution diagnostic framework is proposed on the basis of open-segment fault model. Two stages are included: (1) diagnostic test pattern generation (DTPG) which applies a modified branch-and-bound search from [3] with a SAT solver to generate unique patterns for each single open-segment in the given circuit and (2) a dictionary-based diagnosis which is built upon the inject-and-evaluate analysis and can reduce the number of fault candidates greatly.

In our DTPG, we *indirectly* target each driven gate of the open segment instead of the segment itself *directly* to avoid ambiguities of repeated output syndromes. For Figure 1(b), our DTPG generates only three exclusive patterns targeting G_2, G_3 and G_4, respectively. If $\{G_2, G_3\}$ is the set of gates that capture faulty values, S_2 is the only open segment. If $\{G_2, G_3, G_4\}$ is the faulty-gate set, S_1 is the only open segment. The idea behind is not only to reduce the fault number but also to improve the diagnosis resolution. After DTPG, the information about patterns and their output syndromes are collected. Under the single defect assumption, we can diagnose the faulty circuit by a diagnosis flow proposed to achieve high resolution. This flow mainly consists of two stages: (1) a ***dictionary***-based matching and (2) an ***inject-and-evaluate*** pruning.

III. EXPERIMENTAL RESULTS

Our experiments are conducted on the ISCAS85 benchmark circuits. After generating diagnostic patterns and collecting the corresponding output syndromes, the diagnosis stage proceeds and Table 1 shows the experimental result. For all ISCAS85 circuits, near one candidate that exactly matches the injected defect can be reported on each defective sample to explain the effectiveness of the proposed algorithm.

Table 1: Diagnosis results of our diagnostic patterns

circuit	Diagnosis time (s)	#candidate/ #detected	resolution	#patterns
c432	11.6	91/91	**1.00**	292
c499	16.0	74/73	**1.01**	303
c880	41.5	83/84	**1.01**	615
c1355	145.8	70/70	**1.00**	729
c1908	91.9	68/68	**1.00**	1000
c2670	259.8	73/70	**1.04**	1801
c3540	445.2	79/79	**1.00**	2170
c6288	1045.9	79/80	**1.01**	3444
c7552	2424.8	84/84	**1.00**	4344

IV. REFERENCES

[1] S. Y. Huang, "Diagnosis of Byzantine Open-Segment Faults," in Proc. VLSI Test Symp. (VTS), pp. 248-253, 2002.

[2] W. Zou., W. T. Cheng and S. M. Reddy. "Interconnect Open Defect Diagnosis with Physical Information," in Proc. Asian Test Symp. (ATS), pp. 203-209, 2006.

[3] X. Lin and J. Rajski, "Test Generation for Interconnect Opens," in Proc. Int'l Test Conf. (ITC), pp. 1-7, 2008.

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Phone - +886-35131273
Fax - +886-35710116
Email - opwen@g2.nctu.edu.tw

Registration Information

Registration Category Program Participant Full Conference - $600

Total Fees - $600
Fees applied to Credit Card - MasterCardXXXXXXXXXX7803

CANCELLATION/SUBSTITUTIONS POLICY

Cancellations must be submitted in writing. All cancellations received in writing on or before August 22, 2011 are entitled to a refund, minus a $75 processing fee. No refunds will be given to registrants who cancel their registration after August 22, 2011 or who fail to attend the event. Substitutions for paid registrants may be made at any time without penalty. All requests for substitutions must be submitted in writing to itc2011@badgeguys.com.

DISCOUNT TICKETS

Discount theme park tickets are available online until September 12, 2011.
See ITC Advance Program page 32 or click here.

International Test Conference

Advance Program

Test Week
September 18–23, 2011

Conference and Exhibition
September 20–22, 2011

Disneyland Hotel,
Anaheim, California, USA

Welcome Message

On behalf of the International Test Conference (ITC) Steering Committee, Program Committee and all of the volunteers who were instrumental in putting this year's conference together, we would like to invite you to our 42nd conference which will be held at the Disneyland Hotel in Anaheim, California. We're very pleased to be back on the West Coast again and are especially excited about our partnership with Disney. Not only do we have a great venue, but we're also integrating Disney into the technical program as well. We have a fascinating invited talk presented by a Disney Imagineer, and will be offering a Disney Institute training session in conjunction with our tutorials.

Test Week is comprised of six days packed full of learning opportunities for engineers, managers, professors and students in design and test related fields. We start with 12 tutorials over two days (Sunday and Monday). We will also be repeating our very successful Test Clinic this year and presenting the Disney Institute training session.

Our conference will feature opening and closing keynotes. Bill Dally, Bell Professor of Engineering, Stanford University, Chief Scientist, NVIDIA Corporation, will provide an interesting look into the future of computing. Jyuo-Min Shyu, President, Industrial Technology Research Institute (ITRI), Taiwan, will look at the process of translating scientific discoveries into processes and tools which provide significant business value. Both will be very thought-provoking for design and test researchers, and professionals. The fascinating invited talk by Chuck Davis from Disney will discuss the creation of the spectacular show *World of Color*.

Our program will have 76 presentations covering 10 different topic areas, daily panel sessions from Monday evening through Thursday afternoon and a two-hour lunch-time poster session. There will be several "open" technical activities meetings including many test standards working group meetings throughout the week.

We have a broad, diverse and growing exhibitor floor comprised of EDA, hardware and test solutions providers covering almost any test need. The exhibits area will also be the site of corporate presentations that highlight new and exciting developments in test equipment, services, tools and methodologies. Once again this year, we will be holding our Exhibit Hall Passport Adventure. Stamped passports can be turned in for an opportunity to win a daily drawing on the exhibits floor.

ITC is a great opportunity to make connections with colleagues and test professionals. Our venue this year provides ample opportunities for networking before, during and after the conference. This year our Welcome Reception will be held at A Bug's Land (how appropriate is that?) in the California Adventure Park. Following the reception, we will be treated to an exclusive showing of Disney's World of Color, a spectacular light-on-water display highlighting the Disney animation characters over the years. With Downtown Disney just steps away from the conference, there will be plenty of opportunities for corporate outings and late-night networking. Of course, there are plenty of opportunities for networking during the conference as well. There will be complimentary lunch on the exhibits floor every day as well as extended breaks between sessions and several areas onsite for meetings and quiet conversations.

We invite you to take a look at the Advance Program and hope to see you in September.

Bill Eklow
General Chair

Shawn Blanton
Program Chair

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Test Week Highlights

	Sunday	Monday	Tuesday	Wednesday	Thursday	Friday
Twelve Full-Day TTTC Tutorials A great way to prepare for the ITC Technical program	●	●				
Test Clinic Learn how to test logic and memories in SOCs.		●				
Disney Institute		●				
Four Panels		●	●	●		
Plenary Session – Keynote Address			●			
Disney Imagineer				●		
Closing Keynote Address					●	
55 Technical Papers			●	●	●	
Poster Session				●		
Lecture Series and Advanced Industrial Practices Special sessions containing introductory and broadening material			●	●	●	
World-Class Exhibits Free exhibits-only admission on Wednesday afternoon and all day on Thursday			●	●	●	
Exhibits Passport Program Visit booths and be eligible for daily prize drawings			●	●	●	
Corporate Presentations The latest technical innovations from our exhibitors and corporate supporters			●			
Workshops Finish your Test Week experience with a choice of three					●	●
ITC Welcome Reception			●			
Fringe Technical Meetings	●	●	●	●	●	●

Become an ITC corporate supporter or utilize marketing opportunities

http://www.itctestweek.org

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Test Week At-a-Glance

SUNDAY, SEPTEMBER 18 – FULL-DAY TUTORIALS					
8:30 a.m. – 4:30 p.m.	Tutorial 1 Mixed-Signal DFT and BIST: Trends, Principles and Solutions	Tutorial 2 High-Quality and Low-Cost Delay Testing for VDSM Designs: Challenges and Solutions	Tutorial 3 IEEE Standards Provide Access to Debug, Validation and Test of Ever More Complex ICs—On ATE, on Board, in System	Tutorial 4 Power-aware Testing and Test Strategies for Low-Power Devices	Tutorial 5 The Convergence and Inter-relationship of Yield, Design-for-Manufacturability and Test

MONDAY, SEPTEMBER 19 – FULL-DAY TUTORIALS							
8:30 a.m. – 4:30 p.m.	Tutorial 6 Practices in Analog, Mixed-Signal and RF Testing	Tutorial 7 Delay Test: Concepts, Theory and Recent Trends	Tutorial 8 Demystifying Board-Level Test and Diagnosis	Tutorial 9 Testing Low-Power Integrated Circuits: Challenges, Solutions and Industry Practices	Tutorial 10 Statistical Adaptive Test Methods Targeting "Zero Defect" IC Quality and Reliability	Tutorial 11 The Economics of Test and Testability	Tutorial 12 Testing Memories in the Nano-Era: Fault Models, Test Algorithms, Industrial Results, BIST and BISR

MONDAY, SEPTEMBER 19 – DISNEY INSTITUTE	
1:00 p.m. –5:00 p.m.	Disney Institute Disney's Approach to Inspiring Creativity

MONDAY, SEPTEMBER 19 – TEST CLINIC	
8:30 a.m. –4:30 p.m.	Test Clinic Logic and Memory Testing for SOCs

MONDAY, SEPTEMBER 19 – SPECIAL PANEL	
4:30 p.m. –6:00 p.m.	Panel 1 Industry Leaders Panel – How Will Testing Change in the Next 10 Years?

TUESDAY, SEPTEMBER 20 – TECHNICAL SESSIONS				
9:00 a.m. – 10:30 a.m.	Plenary – Keynote Address: *Power, Programmability and Granularity: The Challenges of ExaScale Computing*			
10:30 a.m. – 5:30 p.m.	Exhibits			
11:00 a.m. – 5:00 p.m.	Corporate Presentations			
12:00 p.m. – 2:00 p.m.	Lunch			
2:00 p.m. – 3:30 p.m.	Session 1 New DFT for General Analog	Session 2 Defect-oriented and Power-aware DFT	Advanced Industrial Practices 1 New Developments in Boundary-Scan Standards	Lecture 1 Partner Conference Showcase 1
4:00 p.m. – 5:30 p.m.	Session 3 ATE Feature Set Expansions and Test Cost Reduction	Panel 2 Challenges and Best Practices in Advanced Silicon Debug	Lecture 2 Small-Delay Faults	Session 4 Ph.D Thesis Competition Forum: Final Round

TUESDAY, SEPTEMBER 20 – ITC WELCOME RECEPTION	
6:00 p.m. –9:30 p.m.	ITC Welcome Reception - California Adventure Park

Test Week At-a-Glance

WEDNESDAY, SEPTEMBER 21 – TECHNICAL SESSIONS				
8:30 a.m.–10:00 a.m.	Session 5 Board Diagnosis and Safe Boundary-Scan Testing	Session 6 RF DFT and Test Cost Reduction	Session 7 Self-Testing and Test Compression Techniques	Lecture 3 Elevator Talks
9:30 a.m.–4:30 p.m.	Exhibits			
10:30a.m.–12:00 p.m.	Panel 3 In-Circuit Test (ICT): The King Is Dead; Long Live the King!	Session 8 BIST and Fault Tolerance for SRAM	Session 9 Defects in Advanced Technologies	Lecture 4 Partner Conference Showcase 2 Highlights from ISSCC
12:00 p.m.–2:00p.m.	Poster Session - Lunch			
2:00 p.m.–4:00 p.m.	Session 10 Pre- and Post-Silicon Validation for µPs and NOCs	Session 11 Taming High-Speed Digital Interfaces > 10 Gbs	Session 12 Timing- and Power-aware DFT	Session 13 Microprocessor Testing
4:30 p.m.–5:30 p.m.	Disney Imagineer *Manufacturing a Disney Spectacular*			

THURSDAY, SEPTEMBER 22 – TECHNICAL SESSIONS			
8:30 a.m.–10:00 a.m.	Session 14 DFT for Complex SOCs	Session 15 Learning from Data: Diagnosis and Data Mining	Advanced Industrial Practices 2 Electrical Validation from First Chip to Product
9:30 a.m. – 1:00 p.m.	Exhibits		
10:30 a.m.–12:00 p.m.	Session 16 Advancing Mixed-Signal Test	Session 17 Stacked Device Test	Advanced Industrial Practices 3 Adaptive Test in Production
12:00 p.m.– 1:00 p.m.	Lunch		
1:00 p.m.– 2:00 p.m.	Keynote *A Systems Perspective on the R&D of Industrial Technology*		
2:00 p.m. – 3:30 p.m.	Panel 4 The Gap: Test Challenges from the Asia Manufacturing Field and Today's Tools		

THURSDAY, SEPTEMBER 22 – WORKSHOPS			
4:00 p.m. – 6:30 p.m.	Testing Three-Dimensional Stacked ICs	Silicon Debug and Diagnosis	Defect and Adaptive Test Analysis
7:00 p.m. – 9:00 p.m.	Workshop Reception		

FRIDAY,SEPTEMBER 23 – WORKSHOPS			
8:00 a.m. – 4:00 p.m.	Testing Three-Dimensional Stacked ICs	Silicon Debug and Diagnosis	Defect and Adaptive Test Analysis

TTTC TEST TECHNOLOGY EDUCATION PROGRAM (TTEP) 2011

The Tutorials & Education Group of the IEEE Computer Society Test Technology Technical Council (TTTC) organizes a comprehensive set of Test Technology Tutorials to be held in conjunction with several TTTC-sponsored technical meetings worldwide. The mission of the Test Technology Educational Program (TTEP) is to serve test and design professionals by offering fundamental education and expert knowledge in state-of-the-art test technology topics. TTEP offers tutorial participants the opportunity to earn official certification from IEEE Computer Society TTTC. Each full-day tutorial corresponds to four TTEP units. Upon completion of 16 TTEP units, official recognition in the form of an IEEE TTTC Test Technology Certificate will be presented to the participant. For further information regarding TTEP, please visit *http://tab.computer.org/tttc/teg/ttep/*

At ITC 2011, TTTC/TTEP is pleased to present twelve **full-day tutorials** on topics of current interest to test professionals and researchers and a **test clinic** geared toward students and newcomers to test. All tutorials qualify for credit towards IEEE TTTC certification under the TTEP program. Five tutorials are held on Sunday, September 18. Seven tutorials will be held on Monday, September 19. *Each tutorial requires a separate registration fee* (see ITC registration form or *www.itctestweek.org* for further information). *Admission for onsite registrants is subject to availability.*
Tutorial attendees receive study material, breakfast, lunch, and coffee breaks. The study material includes a hardcopy of the presentation and bibliographical material. Tutorial registration, coffee and pastry are available at 7:00 a.m. on Sunday and Monday.

Sunday 8:30 a.m. – 4:30 p.m.

more Sunday tutorials >

TUTORIAL 1

Mixed-Signal DFT and BIST: Trends, Principles and Solutions

Presenter *S. Sunter*

Description We analyze trends in IC processes and design, and implications for test, and then look at trends in testing, such as multisite and the dominance of MS in test time/effort for SOCs. Next, we discuss trends in standardized DFT, including IEEE 1149.1, .4, .6, .8, and 1687. The trend analysis concludes with a review of DFT techniques, including fault simulation and BIST. Addressed circuits include PLL/DLL, ADC/DAC, SerDes/DDR, general I/Os, random analog, and RF. Next, seven essential principles of practical analog BIST are presented. Lastly, we search for the most-practical DFT and BIST techniques, ranging from the basic but limited analog bus, to oversampling and undersampling methods that greatly extend range. Examples and case studies are included. Attendees will gain a clear picture of where they are keeping up with industry, why analog BIST always seems to be a future solution, and how to make parametric DFT, diagnosis and testing systematic.

TUTORIAL 2

High-Quality and Low-Cost Delay Testing for VDSM Designs: Challenges and Solutions

Presenters *M. Tehranipoor, K. Chakrabarty, J. Rearick*

Description As technology scales to 32 nm and functional frequency and density continue to rise, many factors and parameters have shown significant impact on design and test of chips. Test engineers must now deal with many new challenges such as IR-drop and power-supply noise (PSN) effects on chip performance, signal integrity and crosstalk effects on path delay, high test pattern volume, low fault/defect coverage, small-delay defect test pattern generation and fault simulation, process variation effects, high cost of test implementation and application, and unmodeled faults. This tutorial provides practice-oriented solutions to the above challenges. The tutorial is designed to provide design and test engineers with in-depth knowledge on high-quality delay test generation for reduced escape and increased in-field reliability.

TUTORIAL 3

Bridge to Moore—IEEE Standards Provide Access to Debug, Validation and Test of Ever More Complex ICs—On ATE, on Board, in System

Presenters *A. Ley, A. Crouch*

Description Modern chips have a wealth of embedded content and are becoming more complex in architecture with SOCs being made up of multiple cores and with multiple-TAP configurations; and known-good-die being stacked into SIPs and POPs. The need for access to embedded instruments for debug, validation, test and yield analysis on various occasions during a chip's life-cycle are driving the industry toward "standard" solutions instead of collections of ad hoc access mechanisms. These solutions include IEEE 1149.1, 1500, 1149.7 and P1687, which provide for, respectively, the original standard test access port (TAP), embedded-core test, the new reduced-pin and enhanced-functionality TAP, and access and control of instrumentation. This tutorial will familiarize the student with these IEEE standards and draft standards, will present the drivers for adoption and use of the standards, will show examples of architectures and usage, and will evaluate pros and cons associated with implementation and use.

< previous Sunday tutorials

Sunday 8:30 a.m.– 4:30 p.m.

TUTORIAL 4

Power-aware Testing and Test Strategies for Low-Power Devices

Presenters *P. Girard, N. Nicolici, X. Wen*

Description Managing the power consumption of circuits and systems is now considered as one of the most important challenges for the semiconductor industry. Elaborate power management strategies, such as voltage scaling, clock gating or power gating techniques, are used today to control the power dissipation during functional operation. The usage of these strategies has various implications on manufacturing test, and power-aware test is therefore increasingly becoming a major consideration during design-for-test and test preparation for low power devices. This tutorial provides knowledge in this area. It is organized into three main parts. The first one gives necessary background and discusses issues arising from excessive power dissipation during test application. The second part provides comprehensive knowledge of structural and algorithmic solutions that can be used to alleviate such problems. The last part surveys low-power design techniques and shows how these low power devices can be tested safely without affecting yield and reliability. EDA solutions for considering power during test and design-for-test are also discussed in the last part of the tutorial.

TUTORIAL 5

The Convergence and Inter-relationship of Yield, Design-for-Manufacturability and Test

Presenters *S. Venkataraman, R. Aitken*

Description The tutorial goal is to show how design-for-yield (DFY) and design-for-manufacturability (DFM) are tightly coupled into what we conventionally think of as test. As process geometries shrink, the line between defects and process variation blurs to the point where it is essentially non-existent. As feature sizes reduced to 90 nm and below, systematic mechanism-limited yield loss began to appear as a substantial component in yield loss due to the interaction between design and manufacturing. The basics of yield and what fabs do to improve defectivity and manage yield are described. DFM techniques to analyze the design content, flag areas of design that could limit yield, and make changes to improve yield are discussed. In DFM/DFY circles, it is common to speak of defect-limited yield, but it is less common to think of test-limited yield, yet this concept is common in DFT (e.g. IDDQ testing, delay testing). Test techniques to close the loop by crafting test patterns to expose the defect-prone feature and circuit marginality through ATPG, and by analyzing silicon failures through diagnosis to determine the features that are actually causing yield loss and their relative impact are covered. This tutorial will provide background needed for DFT practitioners to understand DFM and DFY, and see how their work relates to it. The ultimate goal is to spur attendees to conducting their own research in the area, and to apply these concepts in their jobs.

Monday 8:30 a.m. – 4:30 p.m.

more Monday tutorials >

TUTORIAL 6

Practices in Analog, Mixed-Signal and RF Testing

Presenters *S. Abdennadher, S. Shaikh*

Description The objective of this course is to present existing industry ATE solutions and the alternative solutions to ATE testing for mixed-signal and RF SOCs. These techniques greatly rely upon DFT and BIST structures. Tutorial presents the basic concepts in analog and RF measurements (eye diagram, jitter, gain, power compression, harmonics, noise figure, phase noise, BER, EVM, etc.). Several industrial examples of production testing of mixed-signal and RF devices, such as, SERDES transceivers, PHYs, PMDs, and RF transceivers are also presented. The block-DFT solutions are presented for PLLs, delta-sigma converters, equalizers, filters, mixers, AGC, LNAs, DACs and ADCs. The testing of high-speed IO interfaces, such as, PCI-Express, and XAUI, etc, and the new design trends in RF systems such as MIMO and SIP based systems and their testability are also presented in this tutorial.

TUTORIAL 7

Delay Test: Concepts, Theory and Recent Trends

Presenters *S. Natarajan, A. Sinha*

Description This is an advanced tutorial on validating and testing integrated circuits for speed failures. It covers fundamental concepts, research ideas and industry practices in delay defect and performance testing of nanometer designs. The intended audience is a combination of semiconductor industry practitioners, EDA technologists, and researchers in digital test. The tutorial starts with a discussion on defects and design marginalities that induce circuits to fail at its rated speed while passing at lower speeds, followed by fault models and fault sensitization conditions. It next discusses test generation, fault simulation and diagnosis algorithms. Design-for-test techniques to apply delay tests, metrics to measure delay test quality, and techniques to improve delay test quality and reduce yield loss are then addressed. Application of delay test techniques in post-silicon validation, defect screening, speed binning and field aging are discussed using industry case studies.

TUTORIAL 8

Demystifying Board-level Test and Diagnosis

Presenters *K. Chakrabarty, Z. Conroy, W. Eklow*

Description The gap between working silicon and a working board/system is becoming more significant and problematic as technology scales and complexity grows. The result of this increasing gap is failures at the board and system level that cannot be duplicated at the component level. These failures are most often referred to as "NTFs" (No Trouble Founds). The result of these NTFs can range from higher manufacturing costs and inventories to failure to get the product out of the door. The problem will only get worse as technology scales and will be compounded as new packaging techniques (SIP, SOC, 3-D) extend and expand Moore's law. This is a problem that must be solved, yet, little effort has been applied up to this point. This tutorial will provide a detailed background on the nature of this problem and will provide DFT and test solutions at both the component and board/system level.

TUTORIAL 9

Testing Low-Power Integrated Circuits: Challenges, Solutions and Industry Practices

Presenter *S. Ravi, R. Kapur, M. Tehranipoor*

Description The push for portable, battery-operated, and "cool-and-green" electronics has elevated power consumption as the defining metric of integrated circuit (IC) design. Testing ICs built for such applications requires judicious consideration of test power implications on various aspects of the design cycle (e.g., packaging and power grid design), test engineering (multisite ATE power supply limitations and board design), power-aware test planning (DFT and ATPG), and developing the enabling EDA tool infrastructure (SW for estimation, reduction and low-power test generation). Furthermore, with power optimization and power management techniques becoming "de-facto" in almost all emerging 45-nm and lower chips, systematic testing of these structures and the device in the presence of these structures becomes mandatory. This tutorial is intended to provide an in-depth and up-to-date understanding of low-power IC testing covering (a) dimensions of power-aware testing, (b) techniques for estimation and reduction of test power consumption and (c) test of power-managed designs. Case studies illustrating industrial design deployment practices and existing EDA vendor support will be outlined to illustrate capabilities and gaps in the state-of-the-art.

Monday 8:30 a.m. – 4:30 p.m.

< previous Monday tutorials

TUTORIAL 10

Statistical Adaptive Test Methods Targeting "Zero Defect" IC Quality and Reliability

Presenters *A. Singh*

Description Integrated circuits have traditionally all been tested identically in the manufacturing flow with little sharing of test results between the different test insertions. However, as the detection of subtle manufacturing flaws becomes ever more challenging and expensive in aggressively scaled nanometer technologies, innovative new statistical screening methods are being developed that attempt to improve test effectiveness and optimize test costs by subjecting "suspect" parts to more extensive testing, and also adaptively bring in additional tests that target the suspected failure mode. The idea is analogous to selective security screening approaches applied at airports. Such statistical methods fall into two broad categories: those that exploit the statistics of defect distribution on wafers, and those that exploit the correlation in the variation of process and performance parameters on wafers. This tutorial presents test methodologies that span both these categories, and illustrates their effectiveness with results from a number of recently published experimental studies on production digital and analog circuits from IBM, Intel and LSI, Analog Devices and NXP Semiconductor. Commercial tools offered by a number of new companies that have emerged in the "Adaptive Test" space will also be discussed. Broadly, these aim to provide support for the sharing and leveraging of results from the different tests in the test flow for effective test adaptation and optimization.

TUTORIAL 11

The Economics of Test and Testability

Presenters *S. Davidson, H. Colby, L. Ungar*

Description Test economics provides a way of quantifying the costs and benefits of test, and helps a test engineer choose an effective test strategy. Classical microeconomics is far more sophisticated than what is found in test economics papers. Recent work in behavioral economics, known to the public through bestsellers such as *Freakonomics* and *Predictably Irrational*, has shown that classical assumptions about the behavior of economic actors are wrong. This tutorial will summarize existing work in test economics, provide background on microeconomic and behavioral economics concepts that are of interest to test and DFT engineers, and will show their applicability to test. The student will emerge with the ability to do traditional cost and benefit modeling, and with a deeper understanding of the economic principles that affect the cost and benefits of test. The researcher will emerge with the tools to make a much better case for the benefits of proposed research.

TUTORIAL 12

Testing Memories in the Nano-Era: Fault Models, Test Algorithms, Industrial Results, BIST and BISR

Presenter *S. Hamdioui, A.J. Van de Goor, S. Gregor*

Description The objective is to provide attendees with an overview of fault modeling, test design, BIST and BISR for memory devices in the nano-era. Traditional fault modeling and recent development in fault models for current and future technologies are covered. Systematic methods are presented for designing and optimizing tests, supported by industrial results from different companies (e.g., Intel, ST) and for different technology nodes (e.g., 0.13 um, 65 nm). Impact of algorithmic (e.g., data-background) and non-algorithmic (e.g., voltage) stresses is explored in order to get better insight in the test effectiveness. Novel BIST architectures are covered; special attention is given to the optimization of address generator designs as they typically consume considerable BIST area overhead. BISR and redundancy analysis are also discussed. Moreover, CPU based memory test—which is in some applications the only resource to perform at least the Power-on test is addressed. Finally, future challenges in memory testing are highlighted.

TTTC/TTEP Test Clinic

Monday 8:30 a.m. – 4:30 p.m.

In addition to the regular tutorials, TTTC/TTEP is offering at ITC 2011 a Test Clinic, particularly geared towards newcomers to the area of test, such as new test engineers and students pursuing graduate studies in test. Its key objective is to offer a broad yet comprehensive review of basic test topics in an accessible way to the lay audience. This year's topic will be Logic and Memory Testing for SOCs.

The Test Clinic will be a full-day event, which will be held on Monday, September 19th. Upon its completion, an official recognition in the form of an IEEE TTTC Test Technology Certificate will be presented to each participant.

For further information regarding TTEP, please visit *http://tab.computer.org/tttc/teg/ttep/ The Test Clinic requires a separate registration fee* (see ITC registration form or *www.itctestweek.org* for further information). *Admission for on-site registrants is subject to availability.*

Test Clinic attendees receive study material, breakfast, lunch, and coffee breaks. The study material includes a hardcopy of the presentation and bibliographical material. Test Clinic registration, coffee and pastry are available at 7:00 a.m. on Monday.

TEST CLINIC—Logic and Memory Testing for SOCs

Presenters *A. Cron, Y. Zorian*

Testability is a fundamental requirement for today's systems-on-chip. These integrated circuits are typically designed based on intellectual property (IP) block integration to make the best use of millions of gates available. Logic and memory IP blocks require adequate fault detection, silicon debug and yield optimization. All of which are based on testability infrastructure build into the systems-on-chip. This tutorial presents the fundamental knowledge base that any designer or testability engineer must have in order to fulfill the current industrial best practices for design-for-testability. The tutorial discusses the requirements for block-level test architecting, at-speed design practices, scan compression, memory self-test, debug and repair, test interface standardization efforts such as IEEE Std 1149.1 (JTAG) and IEEE Std. 1500, and integration for system-on-chip level and beyond. Actual industrial experiences will be shared with the audience whenever possible.

Disney Institute

Monday 1:00 p.m. – 5:00 p.m.

DISNEY INSTITUTE—Program Description

See registration information on page 28.

Disney's Approach to Inspiring Creativity

In today's workplace, change is occurring at an ever-increasing rate. In order to be successful in a climate of change, organizations must be able to foster an environment where collaboration and new ideas are not only safe, but expected.

Disney's founder, Walt Disney, knew that Disney's success as a company relied on its ability to encourage innovative ideas and then support their development. At the *Disneyland*® Resort, Disney not only encourages the creative process, Disney manages it to produce the maximum return on its investment.

This Program is designed to show you the business case for creativity. Disney facilitators will present the viability of a corporate culture where the creative process thrives and produces profitable products and services.

They will help you discover how organizational creativity can give you the competitive edge in today's changing business world.

- Foster a collaborative environment that draws on the creative resources of your entire organization
- Establish systems that help your leaders make decisions about new ideas
- Focus your employees' creativity on the goals of your organization
- Improve productivity by implementing new ideas generated in the creative process

Additional Program Notes

- Participants must be at least 16 years of age. Generally, no one under 16 years of age is permitted to participate in any Disney Institute program.
- Each Program participant must carry a valid driver's license and/or passport for access to any backstage areas, if required.
- Please notify the ITC office (see page 33) if you have any special needs.
- Theme park admission is not included in the price of this program, nor is it required. However, if any program participant wishes to stay in the theme park after this program, admission must be purchased.
- Attire should be suitable for current weather conditions. The program might involve walking in the theme parks or resort. Comfortable shoes are recommended. For all backstage tours, all program participants must wear closed toe and closed heel footwear.

Exhibits

Exhibits hours: Tuesday 10:30 a.m. – 5:30 p.m.
Wednesday 9:30 a.m. – 4:30 p.m., Thursday 9:30 a.m. – 1:00 p.m.

FREE EXHIBITS-ONLY ADMISSION

ITC is offering free exhibits-only registration to visit the exhibit hall during all exhibit hours. Onsite registration for this special opportunity begins on Tuesday at the ITC registration area in the Disneyland Hotel Conference Center. Lunch is not included with free admission.

Fill in your Exhibit Hall Passport for Prizes.

All registered ITC attendee will receive a passport with their conference totes. Get your passport stamped while visiting exhibitor booths, drop your completed passport into the box on the exhibit floor, and be eligible for daily drawings for an iPod and an iPod Shuffle. Winners may choose instead a Disney store gift certificate of equal value.

Participating Exhibitors*

Aehr Test Systems
Altanova Corporation
Ardent Concepts, Inc.
ASSET InterTech, Inc.
Atrenta, Inc.
Chroma ATE, Inc.
CMR Summit Technologies
Corelis, Inc.
DCG Systems
DeFacTo Technologies
Evaluation Engineering
Evans Analytical Group (EAG)
Everett Charles Technologies
Exatron
Finley Design Services, Inc.
GOEPEL Electronics, LLC
Gorilla Circuits
Integra Technologies LLC
Integrated Test Corporation
JD Instruments
Johnstech International
Mentor Graphics Corporation
Micro Control Company
Multitest
OpenATE
OptimalTest
PWB America
Q-Star Test
R&D Circuits
Roos Instruments, Inc.
Salland Engineering
SiliconAid Solutions
SPEA America
Synopsys, Inc.
SynTest Technologies, Inc.
TDK-Lamda Americas
TekniProbe Int'l, LLC
Teladyne Relays
Teradyne Global Services
Tessolve DTS
Test Insight
TSSI
Unisem
Vermont MIcrodrilling
Yamaichi Electronics USA, Inc.
ZTEC Instruments

* As of publication date.

Plenary & Keynote Address

Tuesday 9:00 a.m. – 10:30 a.m.

Opening Remarks

William Eklow, *ITC General Chair*

ITC 2010 Best Paper Awards Presentation

Erik Volkerink, *ITC 2010 Program Chair*

Keynote Address

Power, Programmability and Granularity: The Challenges of ExaScale Computing

Bill Dally, *Bell Professor of Engineering, Stanford University, Chief Scientist, NVIDIA Corporation*

Reaching an ExaScale computer by the end of the decade, and enabling the continued performance scaling of smaller systems requires significant research breakthroughs in three key areas: power efficiency, programmability, and execution granularity. To build an ExaScale machine in a power budget of 20 MW requires a 200-fold improvement in energy per instruction: from 2 nJ to 10 pJ. Only 4X is expected from improved technology. The remaining 50X must come from improvements in architecture and circuits. To program a machine of this scale requires more productive parallel programming environments—that make parallel programming as easy as sequential programming is today. Finally, problem size and memory size constraints prevent the continued use of weak scaling, requiring these machines to extract parallelism at very fine granularity—down to the level of a few instructions. This talk will discuss these challenges and current approaches to address them.

About the speaker: Dr. Dally is the Willard R. and Inez Kerr Bell Professor of Engineering at Stanford University and Chief Scientist at NVIDIA Corporation. Bill and his group have developed system architecture, network architecture, signaling, routing and synchronization technology that can be found in most large parallel computers today. While at Bell Labs, Bill contributed to the BELLMAC32 microprocessor and designed the MARS hardware accelerator. At Caltech he designed the MOSSIM Simulation Engine and the Torus Routing Chip which pioneered wormhole routing and virtual-channel flow control. While a Professor of EECS at the Massachusetts Institute of Technology, his group built the J-Machine and the M-Machine, experimental parallel computer systems that pioneered the separation of mechanisms from programming models and demonstrated very low overhead synchronization and communication mechanisms. At Stanford University his group has developed the Imagine processor, which introduced the concepts of stream processing and partitioned register organizations. Bill has worked with Cray Research and Intel to incorporate many of these innovations in commercial parallel computers, with Avici Systems to incorporate this technology into Internet routers, co-founded Velio Communications to commercialize high-speed signaling technology, and co-founded Stream Processors, Inc. to commercialize stream processor technology. He is a Member of the National Academy of Engineering, a Fellow of the IEEE, a Fellow of the ACM, and a Fellow of the American Academy of Arts and Sciences. He has received numerous honors including the ACM Eckert-Mauchly Award, the IEEE Seymour Cray Award, and the ACM Maurice Wilkes award. He currently leads projects on computer architecture, network architecture, and programming systems. He has published over 200 papers in these areas, holds over 75 issued patents, and is an author of the textbooks, *Digital Systems Engineering* and *Principles and Practices of Interconnection Networks.*

Keynote Address

Thursday 1:00 p.m. – 2:00 p.m.

A Systems Perspective on the R&D of Industrial Technology

Jyuo-Min Shyu, *President, Industrial Technology Research Institute (ITRI), Taiwan*

Scientific discoveries open up new horizons, and technologies based on them can create or transform markets. However, the process of translating scientific discoveries into technologies involves a series of risk steps, resulting in low success rates. In industrial technology research institutes such as ITRI, the planning of such projects typically starts with conceptualizing innovative applications that meet certain needs of consumers or society. Once initiated, the process is forced to be in constant touch with both ends of its range: scientific discovery and market needs; the utmost consideration is the large impact it will have on industries, economy and the society at large. In this talk, examples of industrial technology research from a semiconductor application perspective, along with the collaboration model with the industry and academia, are presented. Crucial factors leading to successful deployment of new technologies such as cost, quality, and reliability are also addressed.

About the speaker: Jyuo-Min Shyu is President of Industrial Technology Research Institute (ITRI), the largest applied research institute in Taiwan. He joined ITRI in 1988, starting his research career in the field of semiconductor design technology. He initiated many high-impact R&D programs in ITRI and took the lead in exploring new technologies, contributing to the development and advancement of semiconductor and flat-panel display industries in Taiwan. He was founding chairs of *Chinese Fuzzy Systems Association* (1994), *Taiwan SoC Consortium* (2000), and *Taiwan Nanotechnology Industry Development Association* (2004), and was Executive Director of Taiwan's *National Nanotechnology Science and Technology Program* (2004-2006), chair of *Taiwan Nanotechnology and Microsystems Association* (2006-2008), and Dean of the College of Electrical Engineering and Computer Science, National Tsing Hua University (2007-2009). Dr. Shyu received his BS and MS degrees both from the Dept. of Electrical Engineering of National Taiwan University, and his PhD degree from the Dept. of Electrical Engineering and Computer Science, University of California at Berkeley. He is a fellow of the IEEE and the Chinese Society for Management of Technology (CSMOT).

Disney Imagineer

Wednesday 4:30 p.m. – 5:30 p.m.

Manufacturing a Disney Spectacular

Chuck Davis, *Disney Creative Entertainment Senior Technical Director*

Chuck discusses the creation of the technical aspects of the spectacular show *World of Color*, which is performed nightly on Paradise Bay at Disney California Adventure. This 60-minute lecture will take participants on a little-seen journey through the design, fabrication, installation and mounting process of *World of Color*. We will discover how the teams use normal manufacturing principles and process to insure the eventual outcome is safe, reliable, maintainable, and financially viable, while still delivering on the highest of creativity. Participants will see how the show starts from a creative idea, imagined to provide an "only at Disney" emotional experience. They will understand how this creative experience is the touchstone to which all project decision-making is derived, and how principles of high-reliability, self-diagnostics, redundancy, self-healing, safety and leveraging cutting edge technology are spun together to support the show's creation. We will also see how these systems are used to maintain the show, as well as keep the creative vision fresh and up-to-date.

Please join us for a rarely seen backstage view of this truly unique nighttime spectacular.

About the speaker: Chuck began his Disney career in 1996 after successful stints in the worlds of professional ballet and education. He currently serves as Sr. Technical Director for creative entertainment and is responsible for spectaculars, atmosphere and blue-sky projects. He has been a key player in the creation of many of the most technically sophisticated nighttime spectaculars Walt Disney Parks and Resorts has to offer worldwide. Chuck leads the automation and advanced technologies teams for DLR entertainment. Past projects include *Remember Dreams Come True, Believe there is Magic in the Stars, Believe in Christmas Magic, Fantasmic, Innoventions* and *Disney in the Stars.*

2:00 p.m. – 3:30 p.m.

SESSION 1
New DFT for General Analog
F. Muradali, National Semiconductor (Chair)

1.1 Defect-oriented Testing for Analog/Mixed-Signal Devices
B. Kruseman, B. Tasić, C. Hora, J. Dohmen, H. Hashempour, M. van Beurden, Y. Xing, NXP Semiconductors

1.2 DFT for Extremely Low Cost Test of Mixed-Signal SOCs with Integrated RF and Power Management
R. Mittal, L. Balasubramanian, A. Sontakke, H. Parthasarathy, P. Narayanan, P. Sabbarwal, R. Parekhji, Texas Instruments (India)

1.3 Test Cost Reduction Through Performance Prediction Using Virtual Probe
H-M. Chang, K-T. Cheng, University of California, Santa Barbara;W. Zhang, X. Li, Carnegie Mellon University; K. Butler, Texas Instruments

SESSION 2
Defect-oriented and Power-aware ATPG
A. Gunda, LSI (Chair)

2.1 P-PET: Partial Pseudo-Exhaustive Test for High Defect Coverage
A. Mumtaz, M. Imhof, HJ. Wunderlich, University of Stuttgart

2.2 Faster-Than-At-Speed Test for Increased Test Quality and In-Field Reliability
T. Yoneda, K. Hori, M. Inoue, H. Fujiwara, Nara Institute of Science and Technology

2.3 Clock-Gating-aware Low-Launch WSA Test Pattern Generation for At-Speed Scan Testing
Y. Lin, J. Huang, National Taiwan University; *X. Wen, Kyushu Institute of Technology*

4:00 p.m. – 5:30 p.m.

SESSION 3
ATE Feature Set Expansions and Test Cost Reduction
C. Kuntzsch, Texas Instruments (Chair)

3.1 Architecture and Implementation of a Truly Parallel ATE Capable of Measuring Picoampere-level Current
D. Acharyya, K. Miyao, D. Ting, D. Lam, R. Smith, P. Fitzpatrick, B. Buras, Advantest Verigy Group; *J. Williamson*, White Eagle Consulting

3.2 Development of an ATE Test Cell for At-Speed Characterization and Production Testing
J. Moreira, Advantest Verigy Group

3.3 Actual Implementation of Multidomain Test: Further Reduction of Cost-of-Test
M. Ogura, A. Maeda, Y. Takahashi, Advantest Verigy Group

SESSION 4
Ph.D Thesis Competition Forum: Final Round
I. Polian, University of Passau (Chair)

4.1 Online Timing Variation Detection and Tolerance for Digital Integrated Circuits
G. Yan, X. Li, Chinese Academy of Sciences, Beijing

4.2 Physically-aware Analysis of Systematic Defects in Integrated Circuits
W. Tam, S. Blanton, Carnegie Mellon University

4.3 Investigation into Voltage- and Process-Variation-aware Manufacturing Test
U. Ingelsson, B. Al-Hashimi, University of Southampton

The award winner will be announced immediately before the keynote address on Thursday at 1:00 p.m.

Read the paper's summary by placing your cursor over the paper number.

1.1 Paper Title

Wednesday A.M.

8:30 a.m. – 10:00 a.m.

SESSION 5
Board Diagnosis and Safe Boundary Scan Testing
T. Chakraborty, Qualcomm (Chair)

5.1 Smart Diagnosis: Efficient Board-level Diagnosis and Repair Using Artificial Neural Networks
Z. Zhang, K. Chakrabarty, Duke University;
Z. Wang, Z. Wang, X. Gu, Huawei

5.2 Surviving State Disruptions Caused by Test: A Case Study
K. Parker, Agilent Technologies;
S. Kameyama, Fujitsu and Ehime University;
D. Dubberke, Intel

5.3 IEEE Std. 1581—A Standardized Test Access Methodology for Memory Devices
H. Ehrenberg, GOEPEL Electronics;
B. Russell, Technical Consultant

SESSION 6
RF DFT and Test Cost Reduction
P. O'Brien, Analog Devices (Chair)

6.1 Multisite Test of RF Transceivers on Low-Cost Digital ATE
I. Koren, B. Schuffenhauer, F. Demmerle, F. Neugebauer, G. Pfahl, Intel;
D. Rautmann, Infineon Technologies

6.2 Wafer Probe Test Cost Reduction of an RF/A Device by Automatic Testset Minimization—A Case Study
D. Drmanac, L. Wang, University of California, Santa Barbara;
M. Laisne, Qualcomm

6.3 Accurate Signature-driven Power-conscious Tuning of RF Systems Using Hierarchical Performance Models
A. Banerjee, S. Sen, S. Devarakond A. Chatterjee, Georgia Institute of Technology

SESSION 7
Self-Testing and Test Compression Techniques

R. Parekhji, Texas Instruments (India), (Chair)

7.1 Low-Power Compression Utilizing Clock Gating
E.K. Moghaddam, S.M. Reddy University of Iowa; *J. Rajski*, Mentor Graphics

7.2 Partial State Monitoring for Fault Detection Estimation
Y. Shi, Brown University; *K. Kaewtip*, UCLA;
W-C. Hu, MStar Semiconductor;
J. Dworak, Southern Methodist University

7.3 Logic BIST Silicon Debug and Volume Diagnosis Methodology
E. Amyeen, A. Jayalakshmi, S. Venkataraman, S. Pathy, E. Tan, Intel

10:30 a.m. – 12:00 p.m.

SESSION 8
BIST and Fault Tolerance for SRAM
S. Hamdioui, Delft University of Technology (Chair)

8.1 Generic, Orthogonal and Low-Cost March Element-based Memory BIST
A.J. van de Goor, ComTex; *S. Hamdioui, H. Kukner*, Delft University of Technology

8.2 On Using Address Scrambling to Implement Defect Tolerance in SRAMs
R. Alves Fonseca, L. Dilillo, A. Bosio, P. Girard, S. Pravossoudovitch, A. Virazel, LIRMM; *N. Badereddine*, Infineon Technologies

8.3 A Fully Cell-based Design for Timing Measurement of Memory
S-Y. Huang, Y-C. Chang, C-W. Tzeng, National Tsing Hua University, Taiwan;
J. Yao, Elite Semiconductor Memory Technology

SESSION 9
Defects in Advanced Technologies
E. Amyeen, Intel (Chair)

9.1 Cell-aware Analysis for Small-Delay Effects and Production Test Results from Different Fault Models
F. Hapke, J. Schloeffel, W. Redemund, A. Glowatz, J. Rajski, Mentor Graphics;
M. Reese, J. Rearick, J. Rivers, AMD

9.2 Lithography-aware Critical Area Estimation and Yield Analysis
V. Suresh, P. Vijayakumar, S. Kundu, University of Massachusetts

9.3 Using Well/Substrate Bias Manipulation to Enhance Voltage-Test-based Defect Detection
A. Gattiker, P. Nigh, IBM

Wednesday P.M.

2:00 p.m. – 4:00 p.m.

SESSION 10
Pre- and Post-Silcion Validation for µPs and NOCs
I. Bahar, Brown University (Chair)

10.1 A Software-based Self-Test Methodology for Online Testing of Processor Caches
G. Theodorou, N. Kranitis, A. Paschalis, D. Gizopoulos, University of Athens

10.2 Design-for-Debug Layout Adjustment for FIB Probing and Circuit Editing
K-A. Chen, M-C. Wu, T-W. Chang, M. Chao, J-Y. Jou, National Chiao Tung University; *S. Chen*, Spirox

10.3 End-to-End Error Correction and Online Diagnosis for On-Chip Networks
S. Shamshiri, A. Ghofrani, K-T. Cheng, UC Santa Barbara

10.4 Efficient Combination of Trace and Scan Signals for Post-Silicon Validation and Debug
K. Basu, P. Mishra, University of Florida; P. Patra, Intel

SESSION 11
Taming High-Speed Digital Interfaces > 10 Gbps
Y. Cai, LSI (Chair)

11.1 Analyzing ATE Interconnect Performance for Serial Links of 10 Gbps and Above
M. Lin, T. Tolman, Broadcom

11.2 Elegant Construction of SSC-implemented Signal by AWG and Organized Undersampling of Wideband Signal
H. Okawara, Advantest Verigy Group

11.3 Real-Time Testing Method for 16-Gbps 4-PAM Signal Interface
M. Ishida, K. Ichiyama, D. Watanabe, M. Kawabata, T. Okayasu, Advantest

11.4 Multifunction Multi-GHz ATE Extension Using State-of-the-Art FPGAs
A. Majid, D. Keezer, Georgia Institute of Technology

2:00 p.m. – 4:00 p.m.

SESSION 12
Timing and Power-aware DFT
L. Dilillo, LIRMM (Chair)

12.1 A Novel Scan Segmentation Design Method for Avoiding Shift-Timing Failures in Scan Testing
Y. Yamato, Fukuoka Industry, Science & Technology Foundation; *X. Wen, M. Kochte, S. Kajihara, K. Miyase*, Kyushu Institute of Technology; *L-T. Wang*, SynTest Technologies

12.2 Test-Clock Domain Optimization for Peak Power-Supply Noise Reduction During Scan
K-Y. Laio, J-Y. Wen, Y-C. Huang, M-H. Tsai, J. Li, National Taiwan University; *M-T. Chang, M-H. Tsai, C-M. Tseng, H-C. Li*, Global Unichip

12.3 State-of-the-Art Low-Capture-Power Methodology
S. Bahl, R. Mattiuzzo, S. Khullar, A. Garg, S. Graniello, STMicroelectronics; *K. Abdel-Hafez, S. Talluto*, Synopsys

12.4 Adaptive Parametric BIST of High-Speed Parallel I/Os via Standard Boundary Scan
S. Sunter, A. Roy, Mentor Graphics

SESSION 13
Microprocessor Testing
TBD (Chair)

13.1 Hardware Hooks for Transition Scan Characterization
P. Pant, E. Skeels, Intel

13.2 Transition Test Bring-Up and Diagnosis on UltraSPARC™ Processors
L. Chen, P. Dahlgren, P. Dickinson, S. Davidson, Oracle

13.3 Test Access and the Testability Features of the Poulson Multicore Intel Itanium® Processor
D. Bhavsar, S. Poehlman, Intel

13.4 Optimal Manufacturing Flow to Determine Minimum Operating Voltage
S. Chakravarty, B. Dang, D. Escovedo, A. Haas, LSI

Free
Exhibits Admission
Tuesday, Wednesday and Thursday

8:30 a.m. – 10:00 a.m.

SESSION 14
DFT for Complex SOCs
J. Dworak, Southern Methodist University (Chair)

14.1 EDT Channel Bandwidth Management in SOC Designs with Pattern-independent Test Access Mechanism
J. Tyszer, J. Janicki, Poznan University of Technology; *A. Dutta, M. Kassab, G. Mrugalski, N. Mukherjee, J. Rajski,* Mentor Graphics

14.2 A Novel Test Access Mechanism for Failure Diagnosis of Multiple Isolated Identical Cores
M. Sharma, A. Dutta, W-T. Cheng, B. Benware, M. Kassab, Mentor Graphics

14.3 Techniques to Improve Memory Interface Test Quality for Complex SOCs
VR. Devanathan, S. Vooka, Texas Instruments (India)

SESSION 15
Learning from Data: Diagnosis and Data Mining
V. Mehta, NVIDIA *(Chair)*

15.1 Die-level Adaptive Test: Real-Time Test Reordering and Elimination
K. Gotkhindikar, R. Daasch, Portland State University; *K. Butler, J. Carulli, Jr., A. Nahar,* Texas Instruments

15.2 Forward Prediction Based on Wafer Sort Data—A Case Study
N. Sumikawa, D. Drmanac, L. Wang, UC-Santa Barbara; *L. Winemberg, M. Abadir,* Freescale Semiconductor

15.3 Deterministic I_{DDQ} Diagnosis Using a Net-Activation-based Model
A. Kun, R. Arnold, P. Heinrich, G. Maugard, Infineon Technologies; *H. Tang, W. Cheng,* Mentor Graphics

10:30 a.m. – 12:00 p.m.

SESSION 16
Advancing Mixed-Signal Test
N. Ben-Hamida, Ciena (Chair)

16.1 A Novel Robust and Accurate Spectral Testing Method for Noncoherent Sampling
S. Sudani, D. Chen, Iowa State University; *M. Wu,* Xi'an Jiaotong University

16.2 Application of a Continuous-Time Level-Crossing Quantization Method for Timing Noise Measurements
T. Yamaguchi, Advantest Laboratories; *M. Soma,* University of Washington; *T. Aoki,* Tohoku University; *Y. Furukawa, K. Degawa,* Advantest; *K. Asada, M. Abbas, S. Komatsu,* University of Tokyo

16.3 Adaptive Multidimensional Outlier Analysis for Analog and Mixed-Signal Circuits
E. Yilmaz, S. Ozev, ASU; *K. Butler,* Texas Instruments

SESSION 17
Stacked Device Test
A. Yiin, Intel (Chair)

17.1 Pre-Bond Probing of TSVs in 3-D Stacked ICs
B. Noia, K. Chakrabarty, Duke University

17.2 Evaluation of TSV and Micro-Bump Probing for Wide I/O Testing
K. Smith, P . Hanaway, M. Jolley, R. Gleason, E. Strid, Cascade Microtech; T. Daenen, L. Dupas, *B. Knuts, EJ. Marinissen, M. Van Dieval,* IMEC

17.3 Post-Bond Testing of 2.5D-SICs and 3D-SICs Containing a Passive Silicon Interposer Base
C-C. Chi, National Tsing-Hua University; *EJ. Marinissen,* IMEC; *SK. Goel,* TSMC; *C-W. Wu,* National Tsing-Hua University

Lecture Series and Advanced Industrial Practices

ITC's Lecture Series provides a showcase for topics that are important to the test industry either because they are at the leading edge of technology or because they are foundational in nature. All three sessions will provide a solid background for as well as a snapshot of the current state of the art.

Advanced Industrial Practices (AIP) sessions provide an opportunity for attendees to learn the latest methods and techniques used by industry leaders in addressing some of today's most important test challenges. .

Tuesday 2:00 p.m.–3:30 p.m.

LECTURE 1
Partner Conference Showcase 1
E. Volkerink, Verigy (Chair)

L 1.1 ISTFA: When Test Meets FA...
M. Keim, Mentor Graphics

L 1.2 DFM&Y: Designing Approximate Circuits for Error-Tolerant Applications to Improve Performance Yield
D. Shin, S. Gupta, University of Southern California

L 1.3 D2T: Effective Post-Silicon Validation
S. Mitra, D. Lin, T. Hong, Stanford University; *N. Hakim, D. Gardner*, Intel

Tuesday 4:00 p.m.–5:30 p.m.

LECTURE 2
Small-Delay Faults
B. Benware, Mentor Graphics (Chair)

L 2.1 How Real Are Small-Delay Defects? A Silicon Case Study
SK. Goel, C. Liu, W. Changchien, N. Tseng TSMC; *G. Vandling*, Cadence Design Systems

L 2.2 In-System Characterization Using On-Chip Test Clock Generators
H-S. Jun, Cisco Systems

L 2.3 At-Speed Test Frequency Optimization for Small-Delay Defect Testing
M. Mateja, J. Rivers, M. Reese, A. Over, J. Schulze, J. Zeng, AMD

Wednesday 8:30 a.m.–10:00 p.m.

LECTURE 3
Elevator Talks
S. Mitra, Stanford University (Chair)

The always-popular elevator talks feature the latest studies and results from leading test researchers.

Wednesday 10:30 a.m.–12:00 p.m.

Partner Conference Showcase 2
Highlights from ISSCC
R. Aitken, ARM (Chair)

L 4.1 A 0.013-mm^2 5-uW DC-Coupled Neural Signal Acquisition IC with 0.5-V Supply
R. Muller, J. Rabaey, University of California, Berkeley

L 4.2 Design of a 1-mm^3 Implantable Pressure Sensor Node
H. Ghaed, G. Chen, R. Haque, M. Wieckowski, Y. Kim, G. Kim, D. Fick, D. Kim, M. Seok, K. Wise, D. Blaauw, D. Sylvester, University of Michigan

L 4.3 Fine-Grain Power Management in Multicore SOCs Using Integrated Voltage Regulators
W. Kim, Harvard University

Tuesday 2:00 p.m.–3:30 p.m.

AIP SESSION 1
New Developments in Boundary-Scan Standards
W. Eklow, Cisco Systems (Chair)

A 1.1 Proposed Changes for Improving IEEE Std 1149.1
C. J. Clark, K. Parker, Agilent Technologies: W. Eklow, Cisco Systems

A 1.2 IEEE P1687 (IJTAG) In Practice
J. Rearick, AMD; *K. Posse*, AVAGO Technologies

Thursday 8:30 a.m.–10:00 a.m.

AIP SESSION 2
Electrical Validation from First Chip to Product
W. Eklow, Cisco Systems (Chair)

A 2.1 Design-For-Validation (DFV): On-Chip Features to Accelerate Post-Silicon Coverage
E. Rentschler, AMD

A 2.2 Electrical Validation and Test to Estimate Product Quality of High-Speed Interfaces
S. Puligundla, Intel

A 2.3 Re-Engineering the Power Microprocessor Test Flow —Towards Improved Cost and Time to Market
M. Knox, IBM

Thursday 10:30 a.m.–12:00 p.m.

AIP SESSION 3
Adaptive Test in Production
D. Armstrong, Advantest (Chair)

A 3.1 Adaptive Test Beyond Component Level
P. Maxwell, Aptina Imaging; *P. Nigh*, IBM, *M. Kamm*, Cisco Systems

A 3.2 Production Issues, and Solutions, When Implementing Adaptive Test
J. Roehr, Texas Instruments

A 3.3 Improving the Efficiency of Adaptive Test Considering the Design and Production Environment
Y. Nakamura, Renesas Electronics

Corporate Presentations

The corporate presentation track allows you to stay on top of the latest commercial products in the semiconductor test industry and helps you understand how the innovations behind the products can add value to your work. The corporate track allows you to gain an in-depth understanding of how some of the technology innovations presented at ITC impact the product portfolios of companies. In this interactive forum, ITC exhibitors and supporters will make presentations describing their company, its products and product roadmaps. Company representatives are free to hand out relevant literature such as papers or marketing material. Typical presentations include case studies, best practices and testimonials.

Corporate presentations are scheduled for Tuesday, September 20. Optimal Test, our Diamond Sponsor, will present from 11:00 a.m. to 12:00 p.m. Afternoon presentations, 20 minutes in length each, will be given between 1:00 p.m. and 5:00 p.m. Check back in July for the detailed presentation schedule.

Tuesday 11:00 a.m.–12:00 p.m.

11:00 a.m. OptimalTest
OptimalEnterprise™ Solution–A Customer's Experience

Tuesday 1:00 p.m.–5:00 p.m.

1:00 p.m. Advantest

1:20 p.m. OpenATE, Inc.
OpenATE's 16-site System for a Complete, Lowest-Cost Motion Sensor (Gyroscope/Accelerometer) Test Solution

1:40 p.m. Corelis
Celebrating 20 Years of Test Innovation

2:00 p.m. GOEPEL Electronics
Multidimensional JTAG/Boundary-Scan Instrumentation for Enhanced Test

Tuesday 2:20 p.m.–4:00 p.m.

2:20 p.m. Cadence Design Systems
A Different Synthesis and Test Flow – Cadence Encounter Test

2:40 p.m. Roos Instruments
High-Speed Phase Noise Measurements of VCOs using ATE

3:00 p.m. Johnstech
Optimize Critical Test Objectives Using Kelvin-Ready Configurability

3:40 p.m. Test Insight
Production Test Life Cycle Challenges

Posters

Wednesday 12:00 p.m. – 2:00 p.m.

The poster session is being held in the exhibit hall.

W. Eklow, Cisco Systems (Chair/Coordinator)

PO 1 On-Chip Calibration of the Scan-Enable for Launch-on-Shift Testing
Z. Lak, N. Nicolici, McMaster University

PO 2 Challenges in High-Volume Manufacturing Test of HSIO and Correlation to System Performance
A. Meixner, M. Claudius, E. Fledel, Intel

PO 3 Automation of 3-D DFT and Interconnect Test Generation
E.J. Marinissen, M. Konijnenburg, IMEC, *S. Deutsch, B. Keller, V. Chickermane,* Cadence Design Systems, *S. Goel,* TSMC

PO 4 Using Scan Diagnosis Analysis to Improve Fab Process Debug
S. Palosh, Freescale Semiconductor, *G. Eide,* Mentor Graphics

PO 5 A Novel BIST Design for Testing Quantum-Dot Cellular Automata FPGAs
T. Raviraj, M. Niamat, University of Toledo

PO 6 Early Detection of Gate-Oxide Defects Using Timing Tests at Reduced Supply Voltages
X. Qian, C. Han, A. Singh, Auburn University

PO 7 Hybrid Wireless Pre-Bonding Test Framework Design for 3-D Stacked ICs
D. Zhao, U. Chandran, University of Louisiana at Lafayette

PO 8 Voltage-sensitive Transition Scan-Chain Fault Isolation Using Laser Modulation Mapping and Continuous Wave Probing
S. Kasapi, W. Lo, J. Liao, B.Cory, H. Marks, NVIDIA

PO 9 Intel Post-Si Chipset Logic Validation
C. Angderson, J. Spotswood, J. Crouter, Intel

PO 10 Thermal Margining Tools for Post-Silicon Debug
Y. Pang, R. Mohammed, R. Sahan, A. Xia, P. Shatdarshanam

PO 11 Application of Inter-Die Rank Statistics in Defect Diagnosis
V. Bakshi, R. Daasch, Portland State University

PO 12 Functional Test Abstraction
A. Sivaram, Advantest America

PO 13 Analysis of Resistive-Open Defects in TAS-MRAM Array
J. Azevedo, A. Virazel, A. Bosio, L. Dilillo, P. Girard, A. Todri, LIRMM; *G. Prenat,* CEA/SPINTEC; *K. Mackay,* CROCUS Technology

PO 14 Monte Carlo Algorithm for Compressing Corner Tests
T. Nirmaier, G. Pelz, Infineon

PO 15 Portable Fault Modeling for Memories
K. Jani, Saravanan M.D., ARM

PO 16 GPU Acceleration of Test Selection for N Detections of Transition Faults
D. Xu, H. Li, Y. Han, X. Li, Chinese Academy of Sciences; *K-T. Cheng,* University of California, Santa Barbara

PO 17 Diagnosing Interconnect Open Defects with Test-Pattern Generation
I. Chen, L. Chang, J. Ku, C. Wen, National Chiao Tung University

PO 18 Shorts Detection Improvement Through New Boundary-Scan Output Buffer
Y-F. Lee, C-L. Tee, K. Ram, T-H. Tan, Intel

PO 19 Low-Distortion Single-Tone and Two-Tone Sinewave Generation Using ΣΔ DAC
T. Yamada, K. Kato, K. Wakabayashi, H. Kobayashi, T. Matsuura, K. Niitsu, N. Takai, T. Yamaguchi, Gunma University; *O. Kobayashi, Y. Yano, T. Gake,* Semiconductor Technology Academic Research Center (STARC)

PO 20 Does Conductive Elastomeric Socket Have the Same Electrical Performance as the Soldered Unit Attachment?
G. Oren, E. Dahan, A. Manukovsky, Intel

PO 21 Leveraging P1687 for Verification, Chip ATE, Silicon Debug and more….
W. Bruce, J. Johnson, W. Atwell, Silicon Aid Solutions

PO 22 Test Scheduling with Constraints for IEEE P1687
G. Asani, F. Zadegan, U. Ingelsson, E. Larsson, Linkoping University; *G. Carlsson,* Ericsson

PO 23 Thorough Inspection of Interconnect Capacitance Using Direct Charge Measurement (DCM)
J. Taniguchi, M. Goto, Agilent Technologies

PO 24 De-Embedding Errors in Protocol-aware EVM Test Using Vector Signal Analysis
D. Morris, Roos Instruments

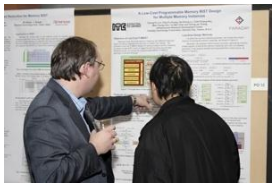
PO 25 Test Method to Efficiently Detect 3-ppb Frequency Variation
E. de Ledinghen, Presto Engineering

PO 26 Multiple Inputs Selector for High-Speed Masking
K-H. Chen, J-T. Huang, P-H. Wu, J-C. Rau, Tamkang University

PO 27 Area Per Yield and Defect Level of Cascaded TMR for Pipelined Processors
M. Arai, K. Iwasaki, Tokyo Metropolitan University

PO 28 Non-destructive diagnostic control of FPGA's
M. Krasnov, A. Sashov, TJSC Russian Space Systems

PO 29 Meet the Working Groups
Working Group Chairs and Representatives from various standards





Panels

Monday, 4:30 p.m. – 6:00 p.m.

PANEL 1 Industry Leaders Panel—How Will Testing Change in the Next 10 Years?

P. Nigh, IBM (Moderator/Organizer)

We will ask a set of industry test experts to answer a set of questions to understand how the testing industry will change in the next 10 years. Fundamental questions will address how test equipment, design-for-test, EDA software, test steps/processes—and the companies that support these—will be changing. The discussion will start with a small set of questions that each panelist must address during their opening statements. Questions from attendees will be solicited before the session. What is the biggest problem in the industry that gets little discussion ? How will be requirements for ATE change in the next 10 years? How will fundamental design-for-test requirements change? What is the best area for creating a new business in the "test field"? Will design reconfiguration at test or new adaptive test applications change how we test? End-to-end testing (wafer probe through field)—will we develop methods to truly optimize across all steps?

Panelists: *B. Cory*, NVIDIA • *W. Eklow*, Cisco Systems • *D. Josephson*, Intel • *R. Madge*, GLOBALFOUNDRIES • *J. Rajski*, Mentor Graphics • *E. Volkerink*, Advantest Verigy Group

Tuesday, 4:00 p.m. – 5:30 p.m.

PANEL 2 Challenges and Best Practices in Advanced Silicon Debug

J. Rearick, AMD (Moderator) • *J. Zeng*, AMD (Organizer)

In the deep submicron technology node, it is impossible to bring a complex chip design to production without going through a number of respins. Silicon debug is becoming one of the most crucial stages that affect the time-to-market of semiconductor designs these days. Debug effort to improve performance and reduce power consumption is traditionally done based on functional/system tests, which can be very expensive. Structural testing, including at-speed scan tests and test-structure-based parameter tests etc, on the other hand, can provide useful information of the performance and power related issues that facilitate the post-silicon design optimization strategy of the design team. This panel will discuss whether structural-based tests, including at-speed scan tests, test-structure-based parametric tests etc., can have a greater role to play in debugging performance and power related issues. The advantages and disadvantages of system test versus structural test for validation will also be explored.

Panelists: *H. Chen*, MediaTek Wireless; *W. Cheng*, Mentor Graphics; *M. Kamm*, Cisco Systems; *P. Pant*, Intel; *E. Rentschler*, AMD

Wednesday, 10:30 a.m. – 12:00 p.m.

PANEL 3 In-Circuit Test (ICT): The King Is Dead; Long Live the King!

D. Dubberke, Intel (Moderator) • *B. Balangue, Jr.* Agilent Technologies (Organizer)

The objective of the panel is to have a good honest discussion from the board test industry experts about the future of ICT. The panel consists of experts from various parts of the industry and groups them according to the following: 1. board test managers/experts from the original equipment manufacturing (OEM), contract manufacturing (CM) and original design manufacturing (ODM) side who strongly believe that the current ICT system is insufficient to test the new generation of PCBA; 2. ICT marketing managers/experts from ICT suppliers (Agilent/Teradyne/TRI) that believe that the current ICT system has enough capabilities and features to maintain test coverage and cost needs for new generation of PCBA; 3. board test managers/experts at OEM/CM/ODM who are dependent on ICT system as their main board test manufacturing strategy and have invested substantial ICT equipment and infrastructure in their manufacturing.

Panelists: *S. Butkovich*, Cisco Systems • *P. Geiger*, Dell • *K. Parker*, Agilent Technologies • *T. Suto*, Teradyne

Thursday, 2:00 p.m. – 3:30 p.m.

PANEL 4 The Gap: Test Challenges from the Asia Manufacturing Field and Today's Available Tools

X. Gu, Huawei Technologies (Moderator/Organizer)

Today more and more electronic manufacturing is moving to Asia. Test, as one of the important parts of the manufacturing process, is used to guarantee the product quality and manufacturing smoothness. By presenting the gap between the test challenges that the Asian companies are facing and the tools they have available today, we hope to give the ITC community an opportunity to better understand the needs for innovation in test technologies and tools.

Panelists: *J. Cho*, Hynix Semiconductor, *R. Fang*, Cisco Systems (China), *J. Qian*, AMD, *J. Yun*, Huawei Technologies

IEEE Computer Society Test Technology Technical Council Workshops

Thursday and Friday

General Workshop Information

Three workshops are being held in parallel immediately following ITC 2011. They start with an opening address on Thursday afternoon, September 22, followed by a technical session. A reception for all workshop participants will be held on Thursday evening, September 22. The remaining the technical sessions will be held on Friday, September 23. The technical scope of each workshop is described below.

Workshop Registration

All workshop participants require registration. To register in advance for one of the workshops, do so online or by faxing the download form. Otherwise, register on-site at regular rates during Test Week at the **ITC registration counter** at the **Disneyland Hotel Conference Center.** *Admission for onsite registrants is subject to availability.* Discount workshop registration rates apply until September 2, 2011. See page 28 for details. Workshop registration includes the opening address, technical sessions, digest of papers, workshop reception, break refreshments, continental breakfast and lunch.

Digest of Papers

A digest of papers will be distributed only to attendees at the workshops as an informal proceedings.

Workshop Schedule

All three workshops will adhere to the same schedule:

Thursday, September 22		Friday, September 23	
Registration	2:00 p.m. – 7:00 p.m.	Registration	7:30 a.m. – 10:00 a.m.
Opening Address	4:00 p.m. – 4:30 p.m.	Technical Sessions	8:00 a.m. – 4:00 p.m.
Technical Session	4:30 p.m. – 6:30 p.m.		
Reception	7:00 p.m. – 9:00 p.m.		

Note: Workshop schedule is subject to change

Further Information

For more information on the three workshops contact their organizers by e-mail or check the TTTC Web site http://computer.org/tttc

WORKSHOP RECEPTION

Thursday, September 22
7:00 – 9:00 p.m.

Workshop Summaries

3D-TEST: 2nd IEEE International Workshop on Testing Three-Dimensional Stacked ICs

Scope: The second 3D-TEST Workshop focuses exclusively on test of and design-for-test for three-dimensional stacked ICs (3D-SICs), including systems-in-package (SIP), package-on-package (POP), and especially 3D-SICs based on through-silicon vias (TSVs). While 3D-SICs offer many attractive advantages with respect to heterogeneous integration, smaller form-factor, higher bandwidth and performance, and lower power dissipation, there are many open issues with respect to testing such products. The 3D-TEST Workshop offers a forum to present and discuss these challenges and (emerging) solutions among researchers and practitioners alike. Topics to include:

Defect due to wafer thinning
Defect due to intro-stack interconnects
DFT Architecture for 3D-SICs
Failure Analysis for 3D-SICs
Known-good die/stack testing
Reliability for 3D-SICs
Standardization for 3-D testing
Test cost modeling for 3D-SICs
Test flow optimization for 3D-SICs
Tester Architecture for 3D-SICs
TSV test, redundancy, and repair

General Chair: Yervant Zorian, *zorian@viragelogic.com*
Program Chair: Erik Jan Marinissen, *erik.jan.marinissen@imec.be*

SDD: 7th IEEE International Workshop on Silicon Debug and Diagnosis

Scope: Troubleshooting how and why systems and circuits fail is important and is rapidly growing in industry significance. Debug and diagnosis may be needed for yield improvement, process monitoring, correcting the design function, failure-mode learning for R&D, or just getting a working first prototype. This detective work is, however, very tricky. Sources of difficulty include circuit and system complexity, packaging, limited physical access, shortened product creation cycle and time-to-market. New and efficient solutions for debug and diagnosis have a much needed and highly visible impact on productivity. SDD is the seventh of a series of highly successful technical workshops that consider issues related to debug and diagnosis of semiconductor circuits and systems—from prototype bring-up to volume production. Topics to include: SDD vs. Yield & TTM

Debug techniques and methodologies
Design and debug
DFT reuse for debug and diagnosis
Manufacturing and prototype environment
Debug standardization
Case studies
Microprocessor, FPGA, IP, SOC debug
Infrastructure IP for SDD
System-level debug and diagnosis
Emulation and hardware accelerator
Cross-geography turn-on, debug & diagnosis
SDD vs. Yield and TTM

General Chair: Teresa McLaurin, *Teresa.McLaurin@arm.com*
Program Chair: Ismed Hartanto, *Ismed.Hartanto@xilinx.com*

DATA: IEEE Workshop on Defect and Adaptive Test Analysis

Scope: New initiatives in getting more out of testing have opened up new avenues of research and development in the areas of extracting information about defects and IC behavior through the use of innovative analysis techniques. As the need for these novel processes is becoming more widely accepted in the industry, new questions about how these techniques should be executed and controlled in production, the types and sizes of database requirements, and even the format of test data and storage itself are being reviewed and discussed. The definition of what is "Adaptive testing" is still being reviewed and defined. Closing the knowledge gap about these issues, the process, new test techniques, database requirements, and how defect models are being used to adapt test flows will be the goals of this year's DATA workshop. Paper presentations on topics related to the topics listed below are expected to generate active discussion on the challenges that must be met to ensure high IC quality through the end of the decade.

Outlier identification
Data-driven testing
Test data analysis
Adaptive testing
Data mining methods for test data processing
High/low voltage and stress testing
Noise and crosstalk testing
Nanometer test challenges
Defect coverage and metrics
Mixed-current/voltage testing
Economics of defect-based testing
Fault localization and diagnosis

General Chair: Jeff Roehr, *JLRoehr@Gmail.com*
Program Chair: Sankaran Menon, *Sankaran.Menon@intel.com*

Fringe Technical Meetings

Sunday to Thursday

ITC arranges for meeting space for appropriate IEEE- or Computer Society TTTC-sponsored groups wishing to hold their meetings during Test Week, September 18– 23.

Tuesday, September 20

10:30 a.m. – 11:30 a.m. New IEEE 1149.1
11:30 a.m. – 1:00 p.m. TTTC ExCom*
1:00 p.m. – 2:00 p.m. TTTC Senior Leadership Council*
3:00 p.m. – 4:00 p.m. TTTC Tutorial & Education Group
4:00 p.m. – 5:00 p.m. BTTAC
5:00 p.m. – 6:00 p.m. TTTC Best Doctoral Thesis Award Committee

Wednesday, September 21

9:00 a.m. – 10:00 a.m. TTTC TMRC*
10:00 a.m. – 11:00 a.m. TTTC Standing Committee Group*
11:00 a.m. – 12:00 p.m. TTTC Standards Group (TTSG)
12:00 p.m. – 1:00 p.m. IEEE P1687 Working Group (IJTAG)
1:00 p.m. – 2:00 p.m. TTTC Operation Committee*
2:00 p.m. – 3:00 p.m. SJTAG Initiative Group
3:00 p.m. – 4:00 p.m. IEEE P1581 Working Group

Thursday, September 22

8:00 a.m. – 10:00 a.m. IEEE P1388 Working Group (3D-Test)
10:00 a.m. – 12:00 p.m. ETS Steering Committee
12:00 p.m. – 1:00 p.m. TTTC Communications Group*

* Members or invitation only

ITC Welcome Reception

Tuesday, September 20, 6:00 p.m. – 9:30 p.m.

Disney California Adventure

The 2011 ITC Welcome Reception will take place at the Disney California Adventure, part of the Disneyland Resort. The evening begins in **A Bugs Land**, a popular attraction reserved for our exclusive use. Guests can socialize with friends old and new while enjoying food, drinks and fun elements of this attraction. The second part of the Welcome Reception will be a private showing of the spectacular **World of Color**, a new Disney nighttime show that premiered in June 2010. World of Color has more than 1,200 fountains and includes lights, water, fire, fog, and lasers, with high-definition projections on mist screens accompanied by musical scores. Please note that this does not include general admission to other park areas.

Each full-conference ITC attendee will receive one free admission to the event. For all other Test Week attendees and/or companions, the admission fee is $42 per person. Extra admissions may be purchased during online registration or onsite at the ITC registration desk.

Categories & Fees

Register Online | Download Form

All Test Week activities require a registration badge for admittance. Register in advance online or by faxing the download form. Otherwise, register on-site at regular rates during Test Week at the **ITC registration counter** at the **Disneyland Hotel Conference Center.** See page 29 for registration hours. To obtain a **substantial discount** register no later than September 2, 2011.

▶ITC Full-Conference Registration Includes ITC technical paper and panel sessions, lecture and advance industrial application series, exhibits, ITC welcome reception, lunch in the exhibit hall, break refreshments, ITC proceedings CD-ROM, ITC tote and shirt. Registration does not include the tutorials/test clinic on Sunday and Monday or the workshops on Thursday and Friday. May purchase additional CD-ROM proceedings at $25 each; one presentation CD-ROM at $25; proceedings CD-ROM set at $100; additional ITC welcome reception admission at $42 per person.

▶ITC One-Day Registration (Onsite-only) Includes ITC technical program activities, exhibits, lunch in the exhibit hall and break refreshments—all for the day of registration only. Also includes ITC proceedings CD-ROM, ITC tote and shirt. Registration does not include ITC welcome reception. May purchase: additional CD-ROM proceedings at $25 each; one presentation CD-ROM at $25; CD-ROM set at $100; ITC welcome reception admission at $42 per person.

▶ITC Free Exhibits-only Registration (Onsite-only) Includes admission to exhibits on Tuesday, Wednesday and Thursday and corporate presentations on Tuesday. Lunch not included.

▶Disney Institute (Online-only),
Includes only enrolment in the Disney Institute session on Monday, September 19.

▶Tutorial/Test Clinic Registration Includes **one** tutorial or the test clinic, study material, continental breakfast, lunch and coffee breaks. The study material includes a hardcopy of the presentation material; and, when applicable, a relevant textbook (textbooks are provided to attendees who register at IEEE/CS member or nonmember rates). You may register for two events (one on Sunday and one on Monday). Registration does not include the ITC technical program, ITC welcome reception, exhibits, exhibit hall lunches, ITC CD-ROMs, ITC tote, shirt or the workshops on Thursday and Friday. May purchase ITC welcome reception admission at $42 per person.

▶Workshop Registration Includes the items specified on page 23. Registration does not include the ITC technical program, exhibits, ITC welcome reception, exhibits, exhibit hall lunches, ITC CD-ROMs, ITC tote, shirt or the tutorials/test clinic on Sunday and Monday. May purchase ITC welcome reception admissions at $42 per person.

▶Discount Rates Early registration rates apply only when your completed registration form and payment are postmarked or faxed by September 2, 2011. Online registrations must also be received by this date. To receive IEEE/Computer Society member or student member reduced rates, you must include your member number, which will be verified.

▶Student Rates IEEE student members must also present their current IEEE Student Member card at the ITC registration counter. Student nonmembers must present their current school student ID.

Registration Fees

Discount Rates*	Full Conference	1-Day-only Conference†	One Tutorial	Test Clinic	Workshop	Disney Institute
IEEE/CS Member	$600	n.a.	$320	$320	$240	$300
Nonmember	$770	n.a.	$400	$400	$300	$300
IEEE/CS Student Member	$300	n.a.	$320	$110	$130	$300
Nonmember Student	$380	n.a.	$320	$130	$165	$300

Onsite Rates	Full Conference	1-Day-only Conference†	One Tutorial	Test Clinic	Workshop	Disney Institute
IEEE/CS Member	$750	$320	$395	$385	$295	$300
Nonmember	$940	$400	$495	$485	$360	$300
IEEE/CS Student Member	$380	n.a.	$395	$130	$165	$300
Nonmember Student	$480	n.a.	$395	$150	$200	$300

*not available after September 2, 2011, †Online registration not available,

Refunds

Registration fees paid by September 2 are refundable on written request to ITC, c/o BADGEGuys, 1959 Jester Circle, Lawrenceville, GA 30043 USA, postmarked or faxed (+1 678.669.1802) by September 2, 2011. A $75 processing fee is charged for each refund.

	Conference and Tutorials	Workshops	Exhibitors
Sun, Sept 18	7:30 a.m. – 5:00 p.m.		7:30 a.m. – 5:00 p.m.
Mon, Sept 19	7:30 a.m. – 5:00 p.m.		7:30 a.m. – 5:00 p.m.
Tues, Sept 20	7:30 a.m. – 7:00 p.m.		7:30 a.m. – 7:00 p.m.
Wed, Sept 21	7:30 a.m. – 5:00 p.m.		7:30 a.m. – 5:00 p.m.
Thurs, Sept 22	7:30 a.m. – 1:30 p.m.	2:00 p.m. – 7:00 p.m.	7:30 a.m. – 12:30 p.m.
Fri, Sept 23		7:30 a.m. – 10:00 a.m.	

Need More Registration Information?

Contact the ITC office
2025 M Street, NW, Suite 800, Washington, DC 20036, USA
Tel. +1 202.973.8665 Fax. +1 202.331.0111

ITC Proceedings Distribution

All ITC full-conference and one-day attendees, including students, will receive free of charge at the conference the 2011 ITC proceedings on CD-ROM.

Ordering Additional Proceedings with Advance Registration

Full-conference attendees may also order additional copies of the 2011 CD-ROM proceedings, beyond the free copy, at $25 each.

Purchasing Additional Proceedings at the Conference

Full-conference and one-day attendees may also purchase onsite additional copies of the 2011 CD-ROM proceedings for $25 each.

ITC Proceedings Five-Year Set

Five ITC CD-ROM proceedings for the years 2010, 2009, 2008, 2007 and 2006 are being sold as a set for $100. The set can be ordered with your online registration for pick-up at the conference or purchased onsite. One set per attendee. *Quantities are limited.*

Minimize note taking! Cover more sessions!

ITC Technical Paper Presentation CD-ROM

The ITC Program Committee has compiled the slides used for this year's technical paper presentations—including lectures and advanced industrial practices—and placed them on a CD-ROM*. You can review sessions that you attended and cover those that you could not attend. The summaries of the poster presentations will also be included. They will only be available at the conference to registered full- and one-day conference attendees, including students—one per person. The cost for this very popular item is only is $25 each.The CDs may be ordered with your advance registration or purchased on-site.

The paper presentation slides make the perfect complement to the full manuscripts in the proceedings, as they contain the latest data .

*Some authors have chosen not to participate. These omitted papers will be indicated in a list provided on the CD box. Slides used in panel sessions and corporate presentations are not included.

Online Hotel Reservations

Reserve a Disneyland Hotel room online by clicking the button above.

1. Rooms may be reserved for the period from **September 13, 2011 to September 27, 2011.**
2. All room must be guaranteed with a major credit card.
3. **Cancellation: Guests must cancel their reservation more than 72 hours prior to arrival (three full days prior to the scheduled date of arrival). Cancellations may be subjected to a penalty fee equal to one night's room rate and tax if less than 72 hours notice is given.**
4. The reservation cutoff date is **September 2, 2011 at 5:00 p.m. EDT.** Reservations made after that date will be made at the ITC rate on a space-available basis.
5. Discounted Disneyland theme park tickets may be purchased when you make your reservation. The online store for tickets closes **September 12, 2011**. Tickets are valid **September 13 – 26, 2011**
6. Parking for hotel guests is $15/night for self-parking and $22/night for valet parking. Follow the "Hotels" signs directly to your destination; do not park in a theme park lot. Those staying at the Disneyland Hotel should park in the *Fantasy* parking lot.
7. Sleeping rooms provide free Internet access.

Click here for more hotel information, location and driving instructions.

Disneyland Hotel Rate
(exclusive of taxes and fees)

Standard Room $169.00

Message to Attendees: ITC has made every effort to secure the best possible group nightly room rate for you at this event. That rate results from a negotiated overall package of event needs such as sleeping rooms, meeting room space and other requirements. Contracts with the venue include a provision to reduce event costs if ITC meets or exceeds its minimum sleeping room block guarantee. Conversely, event costs will increase if ITC falls short of its minimum room block guarantee. Please help ITC keep the costs of this event as low as possible by booking your housing needs at the designated host hotel and through the reservation process created by ITC. Reserving elsewhere means you are booking outside the contracted room block, jeopardizing ITC's ability to meet its contracted obligations and to keep registration fees to a minimum. ITC appreciates your support and understanding of this important issue. Thank you.

Location & Travel

Location

The ITC conference and all associated Test Week events will be held at the Disneyland Hotel Conference Center in the Disneyland Resort, Anaheim, California. The Disneyland Hotel, our conference hotel, is only a short walk to the Disneyland and California Adventure theme parks with their popular rides and attractions.. (Discount theme park tickets are available online until September 12, 2011.) You can also walk to the nearby Downtown Disney area, a lively promenade featuring unique shopping and dining, as well as nighttime entertainment.

Travel

Air

The three airports in closest proximity to the Disneyland Resort are Orange County (John Wayne) Airport (SNA), Long Beach Airport (LGB) and Los Angeles International Airport (LAX). There are several transportation options from these airports to the Disneyland resort. ITC has set up the discount fares for travel to/from airports.

Disneyland Express Bus

The Disneyland Express is a full-size motor coach that operates between the resort and John Wayne (SNA) and Los Angeles International (LAX) airports. A discount fare coupon is available for ITC participants.

SuperShuttle

SuperShuttle shared-ride van service available at all airports. An ITC discount fare is offered for reservations that are made and paid online. You may also arrange for your trip without a reservation (at regular rates) upon arrival at the airport. Reservations for travel to the airport should be made the day before your departure.

Taxi

Taxi service is available at all airports. Some offer flat-rate fares to the Disneyland resort.

Car

See the Disneyland Web site for driving instructions. Registered hotel guests at a Disney Resort hotel should follow signs to their hotel's parking lot. Those staying at the Disneyland Hotel park in *Fantasy* parking lot. Attendees not staying at a Disney hotel should also park in the *Fantasy* parking lot. A daily self-parking fee of $15 is charged. Valet parking is available at hotel entrances for $22 per day.

Information

1. The Advance Program was generated with Adobe Acrobat 8.2.6 on 1-September-2011.

2. The program will be updated periodically as new material is available—check back often.

3. Navigate using the tabs at the top of each page.

4. Use underlined links in the At-a-Glance to find specific items.

5. Most of the papers have a "summary." Place your cursor over the paper number to see it.

3.3 Paper Title

6. For more information contact:

Subject	Contact	Email
Advance Program	Don Denburg Scott Davidson	testweek@rcn.com scott.davidson@oracle.com
Advanced Industrial Practices	Rob Aitken	rob.aitken@arm.com
Corporate Presentations	Ken Mandl	kenneth.mandl@teradyne.com
Exhibits and Exhibiting	Bill Lowd Mike Purtell	bzintrnatl@aol.com m.purtell@ieee.org
Fringe Technical Meetings	Courtesy Associates	itc@courtesyassoc.com
Hotels	Connections Housing	jay@connectionshousing.com
Lecture Series	Rob Aitken	rob.aitken@arm.com
Plenary and Invited Talks	Tim Cheng	timcheng@ece.ucsb.edu
Registration	Courtesy Associates	itc@courtesyassoc.com
Support and Advertising	Cassandra Koenig	Cassandra.koenig@verigy.com
Technical Papers and Panels	Shawn Blanton	blanton@ece.cmu.edu
TTTC Tutorials	Yervant Zorian	zorian@viragelogic.com
Workshops	Yervant Zorian	zorian@viragelogic.com
All Other Questions	Courtesy Associates	

國科會補助計畫衍生研發成果推廣資料表

日期:2011/10/15

國科會補助計畫	計畫名稱: 子計畫四：應用計算智慧推理處理後深次微米時代電路設計上的可靠度挑戰(3/3)	
	計畫主持人: 溫宏斌	
	計畫編號: 99-2220-E-009-011-	學門領域: 晶片科技計畫--整合型學術研究計畫

無研發成果推廣資料

99 年度專題研究計畫研究成果彙整表

計畫主持人：溫宏斌	計畫編號：99-2220-E-009-011-
計畫名稱：後次微米時代新興電子設計自動化技術之研究--子計畫四：應用計算智慧推理處理後深次微米時代電路設計上的可靠度挑戰(3/3)	

成果項目			量化			單位	備註（質化說明：如數個計畫共同成果、成果列為該期刊之封面故事...等）
			實際已達成數（被接受或已發表）	預期總達成數(含實際已達成數)	本計畫實際貢獻百分比		
國內	論文著作	期刊論文	0	0	100%	篇	
		研究報告/技術報告	0	0	100%		
		研討會論文	1	1	100%		
		專書	0	0	100%		
	專利	申請中件數	0	0	100%	件	
		已獲得件數	0	0	100%		
	技術移轉	件數	0	0	100%	件	
		權利金	0	0	100%	千元	
	參與計畫人力（本國籍）	碩士生	0	0	100%	人次	
		博士生	0	0	100%		
		博士後研究員	0	0	100%		
		專任助理	0	0	100%		
國外	論文著作	期刊論文	2	2	100%	篇	在高品質國際期刊(TODAES)發表了全世界第一篇針對於製程變異對積體電路地軟性電子錯誤率估計的論文，並提出統計性軟性電子錯誤率(Statistical Soft Error Rate, SSER)的概念
		研究報告/技術報告	3	3	100%		
		研討會論文	3	3	100%		
		專書	0	0	100%	章/本	
	專利	申請中件數	0	0	100%	件	
		已獲得件數	0	0	100%		
	技術移轉	件數	0	0	100%	件	
		權利金	0	0	100%	千元	
	參與計畫人力（外國籍）	碩士生	8	8	100%	人次	
		博士生	2	2	100%		

		博士後研究員	0	0	100%		
		專任助理	0	0	100%		
其他成果 (無法以量化表達之成果如辦理學術活動、獲得獎項、重要國際合作、研究成果國際影響力及其他協助產業技術發展之具體效益事項等，請以文字敘述填列。)		無					

	成果項目	量化	名稱或內容性質簡述
科教處計畫加填項目	測驗工具(含質性與量性)	0	
	課程/模組	0	
	電腦及網路系統或工具	0	
	教材	0	
	舉辦之活動/競賽	0	
	研討會/工作坊	0	
	電子報、網站	0	
	計畫成果推廣之參與（閱聽）人數	0	

國科會補助專題研究計畫成果報告自評表

請就研究內容與原計畫相符程度、達成預期目標情況、研究成果之學術或應用價值（簡要敘述成果所代表之意義、價值、影響或進一步發展之可能性）、是否適合在學術期刊發表或申請專利、主要發現或其他有關價值等，作一綜合評估。

1. 請就研究內容與原計畫相符程度、達成預期目標情況作一綜合評估

■達成目標

□未達成目標（請說明，以 100 字為限）

□實驗失敗

□因故實驗中斷

□其他原因

說明：

2. 研究成果在學術期刊發表或申請專利等情形：

論文：■已發表 □未發表之文稿 □撰寫中 □無

專利：□已獲得 □申請中 ■無

技轉：□已技轉 □洽談中 ■無

其他：(以 100 字為限)

3. 請依學術成就、技術創新、社會影響等方面，評估研究成果之學術或應用價值（簡要敘述成果所代表之意義、價值、影響或進一步發展之可能性）(以 500 字為限)

由於近年來在先進的電路設計上軟性錯誤被發現的頻率越來越高，商業電子產品的可靠度有了新的挑戰。而製程變異使得軟性電子錯誤變得難以分析，本計畫成功地研究了在深次微米時代下，軟性電子錯誤率的行為。不僅發現了在製程變異下，軟性電子錯誤率的行為與以往傳統上的分析不同，且於本計畫也建立了三種架構來分析在製程變異下軟性電子錯誤率的複雜行為。此三種架構分別為 1)蒙地卡羅分析(Monte-Carlo)架構 2)機器學習(machine learning)分析架構 3)閉合模式(closed-form)分析架構。此三種架構各有其優缺點，在蒙地卡羅分析架構中，提供了相當高的準確率來預測軟性電子錯誤率之行為，但其缺點為所需計算時間也較長。而閉合模式分析架構中，提供了相當快的計算，但其精準度就稍微差了一點。而機器學習分析架構中，其運算速度及精準度都介於蒙地卡羅分析架構及閉合模式分析架構之間。

未來，將可以透過此三種分析架構進行軟性電子錯誤率設計最佳化，設計工程師可依其所需選取適合之分析架構，並經由這些分析架構中獲得一些容錯設計的建議，藉此強化原先電路設計中的弱點或者架構中需要修正的特性以期達成相容的功能性。功率及效能因素也將會在這個階段一併被考量以其達成系統穩健性的最佳化。

是故，過去三年的研究成果中，由於過去的研究只針對電路對輻射干擾的抵抗性配合製程變異做分析，無法計算其全晶片錯誤率。於是在本實驗室成功地運用物理模型結果與計算智能模型化技術，在高品質國際期刊(TODAES)發表了全世界第一篇針對於製程變異對積體電路地軟性電子錯誤率估計的論文，並提出統計性軟性電子錯誤率(Statistical Soft

Error Rate, SSER)的概念，希冀能誘發更多研究能量的投入。目前更進一步地準備分析空間關係性(spatial correlation)與全電量分布(full-spectrum charge collection)對電路設計的影響。

尤其當越來越多的積體電路要使用於車載或生醫相關零件時，可靠度的要求就更高。在圖 4.3 中，SIA (Semiconductor Industry Association) 對可靠度的預估的里程碑對 IC 長期故障率(Long Term Failure Rate) 從過去的幾十個 FIT(Failure in Time, Failure unit, or Failure instance/Time)降到目前只有數個 FIT(甚至希望零瑕疵)。國際車用電子協會(Automotive Electronics Council)也因此把軟性錯誤率的分析納入其最新的設計規範(AEC-Q100-Rev-G)當中。而更如圖 4.4 所示，日本車廠在追求汽車的可靠度上普遍優於歐美國家的車商。而以國內大廠 TSMC 而言，到 2010 年也才有了符合車用電子的半導體製程技術，可見其積體電路可靠度的困難度。本主持人未來將以車載專用的 CAN 控制設計為基礎，發展以零瑕疵為目標的軟性電子錯誤率最佳化方法，並融合其他設計可靠度/可製造性/可測性等對車載與生醫電路影響做全面分析。