行政院國家科學委員會補助專題研究計畫成果報告

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※ 量子點傳輸特性與元件應用 ※
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量子點的傳輸特性與其元件應用

"Transport Property and Device Application of Quantum Dots"

計畫編號：NSC98-2221-E-009-175-MY2
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主持人：林聖迪 交通大學電子工程系副教授

一、中文摘要

在此為期兩年的計劃中，我們進行自組式量子點的傳輸特性與其元件應用的相關研究，不同於一般使用光學激發與偵測來研究量子點的方法，電容與電流的量測能提供單一載子元件應用所需的資訊。在第一年中，我們利用一倒置的高電子遷移率電晶體(inverted high electron mobility transistor)，來探討電子在量子點周圍被捕捉與逃逸的動力學；基於先前對負微分電容的觀測與模擬，我們使用量子點儲存電荷狀態來製作記憶體元件，由於量子點的充電狀態會決定下方二維通道的電導率，所以量測該元件的汲極源極電流可以讀取其記憶狀態；我們利用分子束磊晶成長所設計的結構並設計了各種閘極長度的光罩，完成了元件製作後，量測發現該元件基本電晶體特性完整，而且在特定偏壓下，具有之前所觀察到的電容與頻率的相依特性，顯示我們已達到設定的目標。

I. Abstract

In this two-year project, we study a field effect transistor (FET) with self-assembled quantum dots (QDs) at room temperature. The frequency-dependent capacitance-voltage (C-V) characteristics of the device show a charging-discharging time of 10^{-3} second for the ground states of QDs. The AC source-drain conductivity of the FET device correlates with the electron occupation at the ground state of QDs. Our result reveals that the charge accumulation in InAs QDs modulates the conductivity of the 2D channel underneath.

II. Background Introduction

In the past two decades, self-assembled quantum dots (QDs) draw increasing attention of researchers because of their interesting properties and potential applications on nano-photonics, nano-electronics and quantum information processing. Although optical methods are mostly used to study the novel features of QDs [1,2], electrical characterization like current-voltage (I-V) and capacitance-voltage (C-V) measurements has the importance on their own. One of the main reasons is that the coulomb interaction between carriers in nano-scaled QDs plays a key role in QDs' behavior [3]. However, it is difficult to optically probe the QDs in the states with only electrons or holes. In the past decade, studies on QDs using C-V measurements have made considerable progress and uncovered many special features [4-13]. In these reports, the parameters of QDs or their related defects, such as concentration, energy levels and capture cross-sections were determined with static or transient C-V. Very recently, an interesting behavior called negative-differential-capacitance (NDC) was observed at low [5] and room temperatures [7-9]. The NDC is caused by the fast charging-discharging process in the confined states of QDs and actually is a zero-dimensional effect. The charging-discharging time is in the order of 10^{-3} s at room temperature so it is possible to make memory devices using the self-assembled InAs QDs [8,13].

To realize QDs memory devices, a straightforward way is to integrate the QDs with the field effect transistors (FET). By placing the QDs near to 2-D electron gases (2DEG), the charge states of QDs can be read out by monitoring the conductance of the 2-D channel. The gate of FET above the QDs and 2DEG can be used to electrically control the charge states of QDs (write-in). Previous papers show pretty good memory function, such as long storage time and fast write-in/read-out time, but mostly at cryo-temperature [14-16]. QDs memory devices operating at room temperature have also been reported but the charged levels may be related to the defects around QDs rather than the QDs themselves [17-18], which would be an issue in

practical applications. Very recently, Marquardt and his co-workers used a similar structure to probe the many-particle spin states in QDs at helium temperature [19], which shows the great potential of the QDs-2DEG system for quantum information processing. In this letter, the GaAs-based FET with InAs QDs layer close to the 2-D channel is studied. We found that the charges in the QDs states are responsible for the dynamic behavior of the conductance of 2-D channel. It is worth noting that all measurements are carried out at room temperature so the structure paves the way to the QDs-based memory devices.

III. Sample Design and Device Preparation

The samples were grown on semi-insulating (100) GaAs substrate by a solid-source molecular beam epitaxy system. The sample (RN0632) is an inverted modulation-doped FET with a QDs layer 20-nm above the 2DEG. The detailed structure consists of ~ 200-nm GaAs buffer, 300-nm $Al_{0.33}Ga_{0.67}As$, 40-nm Si-dpoed $Al_{0.33}Ga_{0.67}As$ (n^+ = $2x10^{18}$ cm^{-3}), 10-nm $Al_{0.33}Ga_{0.67}As$ spacer, 20-nm GaAs, InAs QDs layer and 80-nm GaAs on the surface (see Fig. 1a). A comparison sample (RN0633) without the QDs layer was also grown. The growth condition of QDs has been reported elsewhere [8]. The ground state transition energy of QDs obtained with low-temperature (room-temperature) photoluminescence (PL) is about 1.17 eV (1.02 eV). The low-temperature PL of two samples is shown in Fig.1b. Note that the 1.17 eV signal coming from QDs is not seen in the comparison sample without QDs, as expected. The area density of QDs is about $8x10^{10}$ cm^{-2} from the atomic force microscopy measurement on a separate sample. A standard FET process including mesa etch (etch depth ~ 110 nm), source and drain ohmic contacts (35-nm Ni / 70-nm Ge / 200-nm Au annealed at 395 ^oC for 35 s in forming gas) and Schottky metal gate (20-nm Ti / 100-nm Au), was then carried out to fabricate the devices. The FET gate width is 100 μm. To make the subsequent capacitance measurement easy and comparable, the devices with the gate length of 16 μm are investigated.

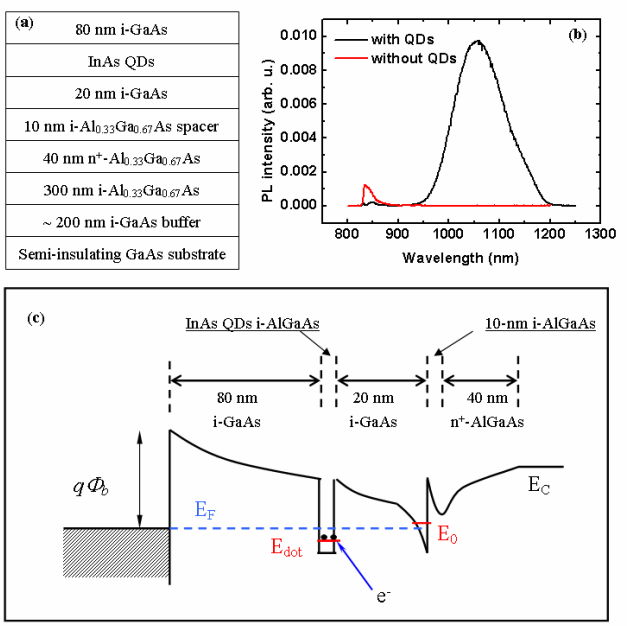

Fig.1. The epitaxy structure (a) and PL spectra (b) of the samples and the schematic band diagram at zero gate bias.

Prior to the discussion of the measurement results, we draw schematically the zero-bias band diagram in figure 1c. The Φ_b, E_F, E_{dot}, E_0 represent the Schottky barrier height, the Fermi energy, the ground state energy of QDs in conduction band and the energy level of the lowest states in 2-D channel, respectively. At zero gate bias, the QDs ground states are lower than the Fermi level but the 2-D state is not, due to the higher energy level of 2-D states. The electrons accumulated in QDs would make the population of electrons in 2-D channel more difficult. We would therefore expect a larger threshold voltage of the FET with QDs. Moreover, because the charging/discharging time of 2-D states is much faster than that of QDs states, one could measure the conductivity of 2-D channel to read out the charging states of QDs. Alternatively, as we have done in this experiment, we could sweep the gate voltage with varying frequency and monitor the frequent dependence of the 2-D channel conductivity.

IV. Result and Discussion

We show the DC characteristics of the two devices in Fig. 2, in which the source-drain current (I_{SD}) is plotted in linear and logarithmic scales v.s. the gate voltage V_{GS}. The inset is the

photo image taken from the processed/measured device with gate length of 16 μm. The measurement was done with the source-drain voltage of 50 mV. Note that the I_{SD} does not enter the saturation region up to V_{GS} = 2.0 V due to the long gate length of our devices. A threshold voltage of 0.5 V of the FET device without QDs was observed clearly. For the device with QDs, the turn-on behavior at about 0.6-0.7 V is not that clear probably due to the leakage current between the gate and QDs layer. Its higher threshold voltage is caused by that the electron accumulation in QDs lowers the electron population in 2-D channel as mentioned above. Beyond the threshold voltage, we can see the transconductance of the device with QDs is lower than that without QDs due to the additional scattering from the nearby QDs.

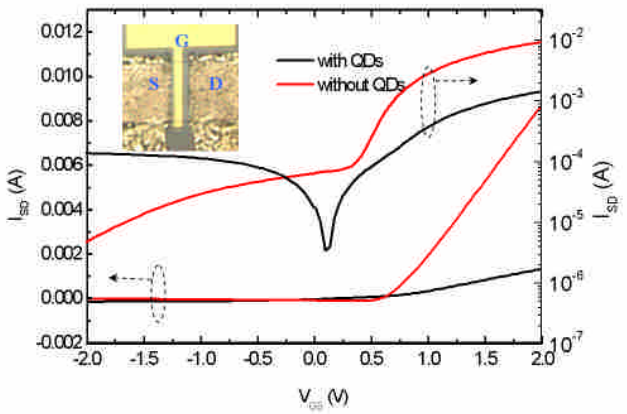

Fig.2. The I-V characteristics of the FET devices with and without QDs. Inset: the photo image of the FET device with the gate length of 16 μm.

To understand the dynamical behavior of QDs, we performed the frequency-dependent C-V measurement with the two terminals of the gate and the source. The measurement setup is similar to that in our previous paper [8]. The frequencies of small AC signal range from 200 to 20 kHz. In Fig.3, the C-V curves of both samples with the positive gate voltages at various testing frequencies are shown. A first glance on both figures reveals that, the C-V dependence on either the frequency or the gate voltage is quite similar for the devices with and without QDs. A rapid increase of capacitance is observed around the threshold voltages of the two devices (0.5 - 0.7 V), because of the formation of 2DEG layer. Comparing with the device without QDs, the capacitance of the device with QDs rises more slowly due to its higher channel resistance. The signals of both devices decrease as the testing frequencies increases, which is probably limited by the parametric RC delay of our testing setup.

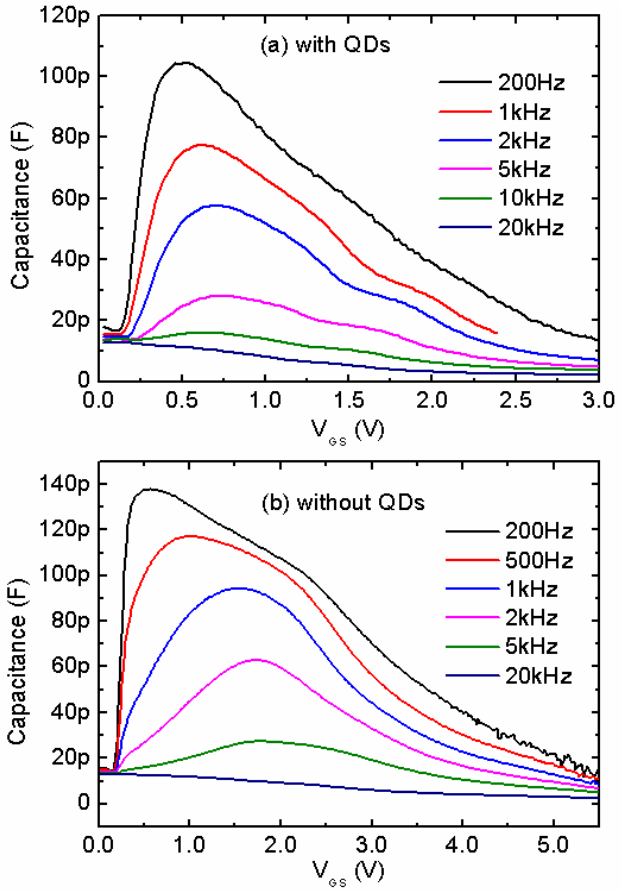

Fig.3. The frequency-dependent C-V curves from the FET device with (a) and without (b) QDs under positive gate voltages.

Let us focus one the C-V curves at the negative gate voltages in Fig. 4, in which there are two signals (peaks around -1.2 V and 0 V) varying with the testing frequency. These two frequency-dependent signals were not observed at all in the FET device without QDs, as shown in the inset of Fig. 4. We suspect that the signal around -1.2 V comes from the charging-discharging of the ground states in QDs for the following reasons. First, considering the distance ratio between gate/QDs (80 nm) and QDs/2DEG (20 nm) (4:1), the voltage difference

between QDs and 2DEG is about 0.24 V at V_{GS} = -1.2 V. It is consistent with the value of conduction band offset of QDs when we take the PL ground state energy of 1.02 eV and the band offset ratio ΔE_c:ΔE_v as 6:4 (that is, $(1.42eV - 1.02eV) \times 0.6 = 0.24eV$). The other reason is that the frequency-dependent C-V shows no any signal after this -1.2 V peak and the ground state of QDs is the lowest state in the structure. In addition, as the testing frequencies increase from 200 Hz to 20 kHz, the capacitance drops quickly, particularly around a few kHz. It indicates that the charging-discharging time is in the order of 10^{-3} second, which is consistent with our previous study [8]. On the other hand, the signal around 0 V can sustain at high testing frequency so it may be due to the higher confined states or 2D states in QDs or caused by the current through the Schottky barrier.

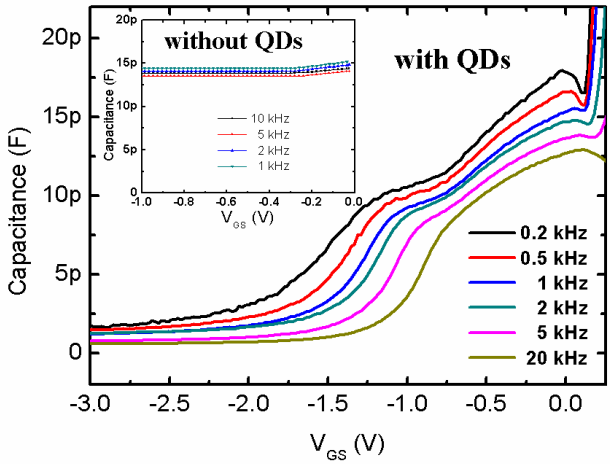

Fig.4. The frequency-dependent C-V curves from the FET device with QDs under negative gate voltages. Inset: the C-V curves from the device without QDs.

To investigate the effect of charged QDs on the 2-D channel, we setup a separate system to measure the frequency-dependent conductivity of the 2-D channel (see the inset of Fig. 5). The 2-D channel between source and drain is serially connected with a resistor of 50 ohms and they together are biased with a DC voltage source (V_p = 0.1 V). The gate voltage is provided with the other DC voltage source added a small AC testing signal (50 mV) whose frequency can be continuously adjusted. The modulated 2-D channel conductivity is amplified with the frequency selective amplifier. Before the measurement, the selective amplifier is calibrated by switching to calibrated mode with definite amplification factor. The output signal of the selective amplifier is taken by the oscilloscope or the analog-digital converter in the computer. In Fig. 5, the measured AC conductivities, named as transmission coefficient here, at 1 kHz to 150 kHz under various gate voltages are plotted. A broad distribution of the transmission coefficient with a maximum around V_{GS} = -1.2 V is clearly observed. Comparing with the frequency-dependent C-V results in Fig. 4, we find that the peak of transmission coefficient located at the nearly same bias point for the charging-discharging of QDs' ground states. More importantly, the frequency dependence of the C-V and the transmission coefficient is also similar, which indicates that the 2-D channel conductivity is related to the charging state of QDs. That is, the accumulated electrons at QDs' ground states affect the 2-D channel conductivity.

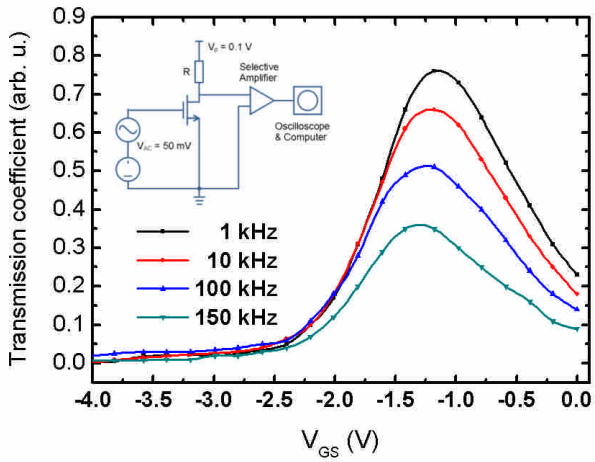

Fig.5 The transmission coefficient of the FET devices with QDs under various gate voltages. Inset: the schematic setup for the transmission coefficient measurement.

Let us discuss the effect revealed in Fig. 5 in more detail. The frequency dependence of 2D channel conductivity is somehow different from those obtained with the C-V measurement shown in Fig. 4. Specifically, the capacitance signal in Fig. 4 almost vanishes when the testing

frequency reaches at 20 kHz but the transmission coefficient survives even at 150 kHz. One possible cause is that the setup in the inset of Fig. 5 is much more sensitive than the C-V measurement as the signal is amplified by the FET first. The other reason may be that their testing conditions are slightly different. When the C-V measurement is carried out, the electric current may pass through either the source contact or the Schottky gate. However, for the transmission coefficient, only the electric current go through the source contact to be measured. In other words, the accumulated/released charges could not be seen directly with the transmission coefficient measurement. The charging/discharging process tends to be slower so the C-V signal dies out at high testing frequencies. This also provides an alternative viewpoint at the effect shown in Fig. 5. The frequency dependence of the transmission coefficient may be caused by the electrons tunneling from the QDs to the 2D channel. At V_{GS} ~ -1.2 V, there is no electron population in the 2D channel but the ground state of QDs is about to be occupied. The small modulation of gate voltage can induce the electron tunneling between the QDs and the lowest states of 2D channel so the channel conductivity is modulated at the same frequency. In addition, different from the C-V curves in Fig. 4, the peak of the transmission coefficient shifts to more negative bias when the testing frequency is higher. We believe that it is caused by the coulomb blockade effect in the QDs. That is, if there is already one electron occupying the ground state of QDs, the second electron has to overcome the potential barrier added by the coulomb repulsion of the existing electron. Because the average occupation number in QDs becomes smaller as the gate voltage is more negative, the energy level of ground state in QDs shifts to lower energy, as well as the peak of the transmission coefficient.

V. Conclusion

We presented the C-V and I-V results of a FET device with an InAs QDs layer in this report. The AC conductivity of the 2-D electron gases formed by a modulation doped GaAs/AlGaAs hetero-structure with the nearby QDs layer has been measured. Comparing with the frequency-dependent C-V data, the charge accumulation in InAs QDs modulates the 2-D channel conductivity. Our results show that the FET-QDs structure can be a promising candidate for memory devices working at room temperature.

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