行政院國家科學委員會專題研究計畫 期中進度報告

三維積體電路(3D IC)之矽晶直通孔(TSV)與其它關鍵技術製程整合研究及應力量測熱傳導模型分析(1/3)
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■期中進度報告

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中英文摘要：

隨著電晶體的微縮，莫爾定律在其物理極限下很難繼續維持。3D IC是個可行並且深具潛力的方法來延續之。本計畫對於3D IC最關鍵的技術做研究，包括銅晶圓接合(Cu wafer bonding)、TSV(Through-silicon via)的製程研究、薄化晶圓(wafer thinning)。今年在TSV製程研究以及銅接合方面有了重大進長，除了確定TSV中填充的深度，並且在蝕刻TSV中產生的micro masking有了具體且有效的解決辦法。再來則是確立了長碳管的製程參數；接合方面則是有新的發現，接合過程中可同時產生一層保護層防止銅氧化。這些成果和機制將被運用在之後的製程條件中，達到更佳的成果。

As integrated circuits (IC) is scaling down, Moore's Law cannot remain because of the physical limitation. Three-dimensional integrated circuits (3D IC) is a feasible approach, and has the potential to extend Moore's Law. This research project is focus on the key technology of 3D IC, including copper wafer bonding, TSV (Through-silicon via) of the manufacturing process, thinning wafer(wafer thinning). This year, TSV process and copper bonding have achieved great results. In addition to determining the depth of TSV after the filling, we also found the concrete and effective solutions to eliminate micro masking after etching TSV. For the aspect of CNT(carbon nano tube), we determine the processing parameters, in addition, there is a new discovery in the bonding research, that during bonding process a passivation layer can form to prevent copper oxidation. These results and mechanisms will be used in the future process to achieve better results.

前言：

至從第一顆電晶體發明至今，積體電路走過了四十多年，隨著電晶體尺寸縮小，使我們漸漸擁有高功能的運算器。一直以來，積體電路維持平面化的規格，但是隨著元件尺寸縮小，如何繼續維持原本的運算功能以及整合更多功能變得相當的關鍵，晶片功能得以不斷的提升，目前晶片的進步基本上依循摩爾定律的預測。在不久的未來，由於微影技術及物理極限，縮小電晶體的發展將會遇到瓶頸。

另一方面，由於單一晶片上電晶體數目的持續增加及晶片複雜化所造成的總導線增加，決定晶片表現的關鍵已經由單一電晶體轉為總導線電阻電容延遲。再者，隨著對晶片功能需求的不斷提升，往往需要特殊製程或是特殊材料的元件的加入，因此，異質元件的整合需求也越來越大。

為了解決上述的挑戰與需求，遂有3D整合與三維積體電路(3DIC)概念的出現。3D IC技術的概念基本上是改變傳統將元件放置在二維XY 平面晶片上的方式，增加第三維也就是直立堆疊的空間(Z 軸)。也因為如此，使用3D 技術可以避免傳統二維電子晶片或元件繼續發展下去所擁有的問題。

3DIC技術是指利用晶圓接合(wafer bonding)或是晶片堆疊(chip stacking)，利用through-silicon via(TSV)連接已薄化的晶圓或是晶片，因此可將傳統的二維積體電路晶片轉變成三維積體電路晶片。也由於3D IC能有效地利用空間及縮短電流信號所傳輸的距離，故可減低電阻電容延遲及總電阻值。又由於利用晶圓接合或是晶片堆疊的特殊概念，因此異質基板材料的元件可以分別製作再行堆疊。因此3D IC技術能在輕薄短小與價格的要求下提供多功能異質整合、高效能(high performance)與低功耗(low power dissipation)等許多優點。

但在3DIC中散熱應力會是一大挑戰，在熱傳導方程式不在是以往漂移擴散公式所描述。現在，熱傳導機制必須引入相關量子熱傳導機制。近年來，所發展出來的hydrodynamic model提供了一個解決的管道。我們可以將此model建構在模擬軟體中，這樣就可以有效的做好散熱的問題。同時TSV不同的材料特性會有不同的熱膨脹係數，導致內部會有應力的產生。作彎曲應力之分析，即可瞭解它們接合時以及遷入TSV和薄膜電晶體是否會對整體晶圓造成彎曲的影響，這樣就能解決一些製程上的問題。

3D IC的特殊概念，此科技將會顛覆傳統的二維積體電路，也因此牽涉的領域包括設計、製程技術與設備、封裝測試方式及終端產品應用及表現，這些領域均缺一不可，也同時息息相關，並將決定3D IC的成熟度與最終產品。換句話說，3DIC事實上乃為一個整合上中下游領域的一個全新科技。而在這些領域中，尤其以關鍵的3DIC 製程技術為最重要的決定因素。

研究目的：

本研究計畫的目的為建立學術界三維積體電路的關鍵技術,包含TSV、應力熱模擬分析、各種材料應用。三維積體電路技術也是延續莫爾定律的關鍵方法，日本早在20年前便嘗試將3D IC技術應用在DRAM上，雖然我國在該領域的發展上，起步較其他半導體大國晚,但我國擁有完整的半導體產業架構，更是全球IC 設計、晶圓代工以及封測的重鎮之地，有著傲視全球的垂直分工完整半導體產業供應鏈，搭配著學術界的研究發展，擁有急起直追的無限潛能。

當前最重要的就是關鍵技術的研發，藉此建立三維積體電路的完整製程模式，並帶動三維積體電路的設計進而生產成熟的產品推至市場。要達到此目的，我們必須要有熟悉該領域並且有經驗的人在台灣從事研究，同時透過學術交流及機構合作的方式來進行跨領域、跨學科的研究。並藉由交流逐步培養三維積體電路的人才，厚植我國三維積體電路實力以期能在下一輪的半導體革命中拔得頭籌。

本研究計畫整合TSV、薄化晶圓與晶圓接合技術並將之應用在其他的半導體技術(CNT或Ni nanowires)，除了該技術之外，也對三維積體電路的應力以及熱傳相關做研究，而這些也是目前相關研究較少涉略的部分，同時也是新穎且具前瞻性的研究題材。並且整合應用其他奈米材料組合並經由電路布局設計，朝向散熱性佳、穩定性高的方向邁進。本研究計畫期許能建立起整個三維積體電路製程及特性的藍圖、模型、參數，來替我國在該領域開疆闢土。

研究方法：

銅晶圓接合：

本年度計畫主要內容為銅晶圓接合之物理特性與材料分析研究，預計需時兩年時間，目前雖然已有銅晶圓接合之基本研究，但是，科學界對於其詳細的物理特性如晶粒生成及材料分析仍有許多不明瞭之處，將以現有的晶圓接合參數進行晶圓接合，然後進行物理特性與材料分析的研究，重點在於建立銅晶圓接合的參數地圖，並測試最佳的參數。

此外，目前雖然已有銅晶圓接合之基本研究，但是大部分的結果都是銅膜接合，科學界對於如何製作pattern的銅與TSV填充物之間關係的最佳參數以供接合所知仍有限，將採用的方法各種不同的方法包括 CMP(化學機械研磨法)進行研究，設計不同形狀的銅pattern與不同形狀、不同材料TSV填充物的填充能力探討與其之間的接合關係，然後利用切割(dicing)的方式及four point bending測試接合強度，本年度主要的重點在於建立銅pattern與TSV關係製程的參數地圖，並測試最佳的參數。

由於科學界對於銅晶圓接合仍缺乏系統性的研究，對於與元件的整合更是缺少，本年度將以進行一連串的銅晶圓接合整合，從設計、製程到測試與分析都將包括在內，本年度主要的重點在於建立銅晶圓接合與TSV間關係的製程整合。

TSV：

本年度的重點在於TSV之蝕刻製程研究，將使用HDPRIE的機台，配合參數的調整進行物理性質的研究並，已達到了解並掌握TSV蝕刻的目的，並建立TSV蝕刻製程的參數地圖，測試最佳的參數。此外，還要研究TSV之材料填充與應力所產生的結果，研究方法將以取得TSV蝕刻試片後，然後使用不同材料加以填充，並發展出最佳填充與最低應力的材料，本年度主要的

重點在於建立不同材料的TSV填充能力，並且確定填充的均勻性。

另外在應力方面使用ANSYS軟體，模擬分析不同材料在不同形狀不同深寬比所造成的應力分佈，以此結果及填充能力為依據以便選擇TSV的材料。目前雖然已有TSV(Through-silicon Via)之基本研究，但是，科學界對於TSV 仍缺乏系統性的研究，對於與元件的整合更是缺少，本研究採用的方法將以進行一連串的TSV製程整合，從設計、製程到測試與分析都將包括在內，本年度主要的重點在於建立TSV填充材料選用上之製程整合。

薄化晶圓：

目前國際上薄化晶圓研究大部分均屬產業應用，學術研究還屬稀少，本年度主要內容為薄化晶圓之研究與特性分析，研究方法將以使用各種薄化晶圓方式來進行晶圓本身研究與特性分析，第一年主要的重點在於建立晶圓薄化的製程參數與其可靠度能力。

結果與討論：

在接合技術上的突破：在晶圓表面有更好的粒子汙染容忍度。然而，這種技術在設備和製造工具上，還是有潛在污染問題。金屬擴散和共晶接合提供直接的連結，但是若在街合時壓力不均勻造成有空氣間隙，未接合區域可能會氧化會導致可靠度問題。矽直接接合提供更高的 via 的密度和更好的對準，但是乾淨的表面和接合環境(真空)的要求是非常重要的。混合接合，結合金屬和高分子材料或者氧化物接合，在封裝的電路上，同時能達到穩定且增強的黏著性。高產出量和可靠性優勢，混合接合成為了3D IC的一種可行方法。

在Via方面，本篇計畫中所用的奈米碳管及鎳奈米線是一個最佳的例子，這兩個奈米材料已經在學界已研究多年，但在三維積體電路的實用面上這是第一次，藉由此計畫，我們預期可以發揮其優點處以增進三維積體電路的成長。

計畫成果自評：

經過實驗團隊一年來的合作與努力，各項研究已有相當進展，成果如下：

(1)　銅晶圓接合

a. 能夠精確觀察銅晶圓接合時兩銅膜之介面的晶粒成長與生成。

b. 解決如何控制不同的晶圓接合參數以供觀察與分析。

c. 解決如何精確控制在銅製程參數下，可以得到最佳形狀的銅 pattern。此計畫成果發表於以下列出之國際期刊論文[9]

d. 解決完整考慮不同銅接合參數與製程整合的關係。

e. 建立可對準pattern面對面晶圓接合的製程參數

(2)　TSV

a. 在機台內控制參數及達到 TSV 在不同晶圓與不同位置的均勻性。

b. 能夠明確的觀察TSV的實際蝕刻深度。

c. 能夠明確的觀察TSV的實際填充深度

d. 建立pattern間距對於TSV蝕刻時

e. 建立奈米碳管之熱傳導與應力模擬分析

(3)　薄化晶圓

a. 建立晶圓均勻薄化與厚度的製程參數

b. 了解在薄化晶圓的過程中因太過薄化而造成晶圓呈彎曲弓狀所帶來的變化及晶圓接合技術上的影響，此計畫成果發表於以下列出之國際期刊論文[10]。

c. 完成量測晶圓薄化後的彎取量測架構

d. 建立薄化厚度與彎曲程度間的可靠度參數

在致力於建立銅晶圓接合、TSV 及薄化晶圓製程整合的過程中，仍有部分成果未達完善，如:如何改善晶圓薄化後的可靠度能力、研究 TSV 之材料填充與應力所產生的結果，對於發展出最佳填充性及最低應力的材料並達成填充得均勻性皆尚在實驗階段。而混和接合中使用高分子材料與錫球混合接合的方式更是提供一個能夠在低溫接合的參數，進而使其在元件製程應用及進階提高晶圓級接合技術的發展及可靠度能力(發表之國際會議論文[4])，另外對於架構出奈米級銅接合pad的技術能提升在元件內訊號傳輸的速率(發表之國際期刊論文[8])，此成果能達到輕薄短小及高效能的應用要求，總括上述成果對於 3D IC 關鍵技術的發展有階段性的提升並為台灣的半導體業跨出重要的一步。

已發表論文:

本計畫實驗成果豐碩，目前已有十一篇國際期刊論文已發表或即將刊出，另外有十二篇的國際會議論文已發表或被接受，其中有一篇是該領域中頂級的會議論文IEDM。此外，由於研究成果傑出，這些論文中包括 三篇邀請論文及二篇邀請演講。

發表論文總表: 已發表或接受之國際期刊論文

1. **Kuan-Neng Chen,** Zheng Xu, and Jiang-Qiang Lu, "Electrical Performance and Alignment Investigation of Wafer-level Cu-oxide Hybrid Bonding," to be published in IEEE Electron Device Letters.
2. Sang Hwui Lee, **Kuan-Neng Chen**, and Jian-Qiang Lu, "Wafer-to-wafer Alignment for 3D Integration", to be published in *IEEE Journal of Microelectromechanical Systems*.
3. S. L. Lin, W. C. Huang, C. T. Ko, and **K. N. Chen**, "BCB-to-Oxide Bonding Technology for 3D Integration", to be published in *Microelectronics Reliability*.
4. ***[Invited Paper]*** Cheng-Ta Ko, and **Kaun-Neng Chen**, "Low Temperature Bonding Technology for 3D Integration", to be published in *Microelectronics Reliability*.
5. ***[Invited Paper]*** Ya-Sheng Tang, Yao-Jen Cheng, and **Kaun-Neng Chen**, "Wafer-Level Cu-Cu Bonding Technology", to be published in *Microelectronics Reliability*.
6. **K. N. Chen,** C. A. Cheng, W. C. Huang and C. T. Ko, "Bonding Temperature Optimization and Property Evolution of SU-8 Material in Metal/Adhesive Hybrid Wafer Bonding," to be published in *Journal of Nanoscience and Nanotechnology*.
7. **K.N. Chen,** A. M. Young, S. H. Lee, and J. -Q. Lu, "Electrical Performances and Structural Designs of Copper Bonding in Wafer-Level Three-Dimensional Integration," to be published in *Journal of Nanoscience and Nanotechnology*.
8. ***[Invited Paper]*** **Kuan-Neng Chen,** and Chuan Seng Tan, "Integration Schemes and Enabling Technologies for Three-Dimensional Integrated Circuits (3D IC)", to be published in *IET Computers and Digital Techniques.*
9. **K. N. Chen,** C. K. Tsang, W. W. Wu, S. H. Lee, and J. Q. Lu, "Fabrication of Nano-Scale Cu Bond Pads with Seal Design in 3D Integration Applications", *Journal of Nanoscience and Nanotechnology*, 11, pp. 3336-3339, Apr. 2011.
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已發表或被接受之國際會議論文

Top Conferences

1. **K. N. Chen,** T. M. Shaw, C. Cabral, Jr., and G. Zuo, "Reliability and structural design of a wafer-level 3D integration scheme with W TSVs based on Cu-oxide hybrid wafer bonding", **2010 International Electron Devices Meeting (IEDM)**, San Francisco CA, Dec. 6-8, 2010.

Proceedings and Conference Presentations

1. S. Y. Hsu, J. Y. Shih, and **K. N. Chen**, "Diffusion Behavior and Mechanism of Co-Sputtering Metals as Bonding Materials for 3D IC Interconnects during Annealing Treatment", 2011 IEEE International Nano Electronic Conference (INEC), Tao-Yuan, Taiwan, Jun 21-24, 2011.
2. S. L. Lin, W. C. Huang, and **K. N. Chen,** "Studies of Oxide to Polymer Bonding for 3D IC", 2011 IEEE International Nano Electronic Conference (INEC), Tao-Yuan, Taiwan, Jun 21-24, 2011.

3. C. A. Cheng, C. T. Ko, and **K. N. Chen,** "Investigation of bonding temperature for SU-8 materials in wafer-level hybrid bonding technology for 3D IC", 2011 IEEE International Nano Electronic Conference (INEC), Tao-Yuan, Taiwan, Jun 21-24, 2011.
4. ***[Invited]*** **Kuan-Neng Chen,** "Three-Dimensional Integrated Circuits (3D IC): Concept, Technology, and Outlook", 18TH Symposium on Nano Device Technology (SNDT), Hsinchu, Taiwan, Apr. 21-22, 2011.
5. **K. N. Chen,** C. A. Cheng, W. C. Huang, and C. T. Ko, "Adhesive Selection and Bonding Parameter Optimization for Hybrid Bonding in 3D Integration", 2011 TMS Meeting, San Diego, CA, Feb 27-Mar. 3, 2011.
6. ***[Invited]*** **Kuan-Neng Chen**, "Taiwan Research and Development Activities for 3D Integrated Circuits", 2010 International Conference of 3-D Architectures for Semiconductor Integration and Packaging, San Francisco CA, Dec. 8-10, 2010.
7. Cheng-Ta Ko, **Kuan-Neng Chen,** Wei-Chung Lo, Chuan-An Cheng, Wen-Chun Huang, Zhi-Cheng Hsiao, Huan-Chun Fu, and Yu-Hua Chen, "Wafer-Level 3D Integration Using Hybrid Bonding", IEEE 3D IC International Conference, Munich, Germany, Nov. 16-18, 2010.
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10. Cheng-Ta Ko, Zhi-Cheng Hsiao, Huan-Chun Fu, **Kuan-Neng Chen,** Wei-Chung Lo, and Yu-Hua Chen, "Wafer-to-Wafer Hybrid Bonding Technology for 3D IC", Electronics System Integration Technology Conferences (ESTC 2010), Berlin, Germany, Sep. 13-16, 2010.
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Fabrication of Nano-Scale Cu Bond Pads with Seal Design in 3D Integration Applications

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A method to fabricate nano-scale Cu bond pads for improving bonding quality in 3D integration applications is reported. The effect of Cu bonding quality on inter-level via structural reliability for 3D integration applications is investigated. We developed a Cu nano-scale-height bond pad structure and fabrication process for improved bonding quality by recessing oxides using a combination of SiO_2 CMP process and dilute HF wet etching. In addition, in order to achieve improved wafer-level bonding, we introduced a seal design concept that prevents corrosion and provides extra mechanical support. Demonstrations of these concepts and processes provide the feasibility of reliable nano-scale 3D integration applications.

Keywords: Cu, Wafer Bonding, Seal, and 3D Integration.

RESEARCH ARTICLE

1. INTRODUCTION

Three-dimensional integrated circuits (3D IC) have become an attractive option for next generation electronic applications.[1] Fabrication of 3D integration has been enabled by layer transfer technology in which bonding of various layers is a key processing step.[1] Various bonding methods utilized for 3D applications include fusion bonding, metal bonding, and adhesive-based bonding.[2–5] The choice of the bonding method is dependent on the process flow of the assembly, alignment tolerance requirements, and the specific applications.[5] In particular, Cu bonding has become a promising candidate for 3D applications, because in addition to a strong mechanical attachment this technology can achieve a high density of electrical connection between the stacked layers.[6–7]

During the thermo-compression Cu bonding process, the bonding alignment accuracy critically depends on precise temperature control during the bonding stage.[8] This is particularly important when a bonding layer is used to provide an electrical contact for various inter-strata input/output (I/O) connections with dimensions close to the standard back-end-of-the-line (BEOL) ground rules.

In addition to alignment, yield and reliability of the Cu–Cu interconnection created during the bonding process also depends on the quality of the bonded interface. The most common cause for bonding yield loss is the lack of contact between two mating metal surfaces during the bonding step, and is directly related to the Cu damascene technology used to fabricate these structures.[9] In such processes, chemical-mechanical planarization (CMP) is usually implemented as the last step, providing a surface with Cu patterns often dished below the level of surrounding dielectric. Such topography is not optimal for good bonding. Therefore, in this work, we have developed a new nano-fabrication surface preparation method that maximizes the metal-bonding area and hence improves the bonding quality and reliability of 3D structures.

When de-bonding tests are performed, the outermost area of the pad or interconnect pattern is most stressed. Therefore, the critical inter-strata I/O signal pads/interconnects in these areas are most prone to failure. In order to achieve improved wafer-level bonding, we have introduced a seal design concept that not only prevents corrosion, but most importantly provides extra mechanical support.

2. FABRICATION OF NANO-SCALE Cu BOND PADS

Typical Cu bond pads for wafer-level 3D application are fabricated using damascene technology. As indicated in Figure 1, the surface of the Cu bond pad typically is recessed after the damascene process up to 50 nm depending on the dimensions of the pad. In this SEM image, the Cu is dished ~20 nm below the oxide level. Even

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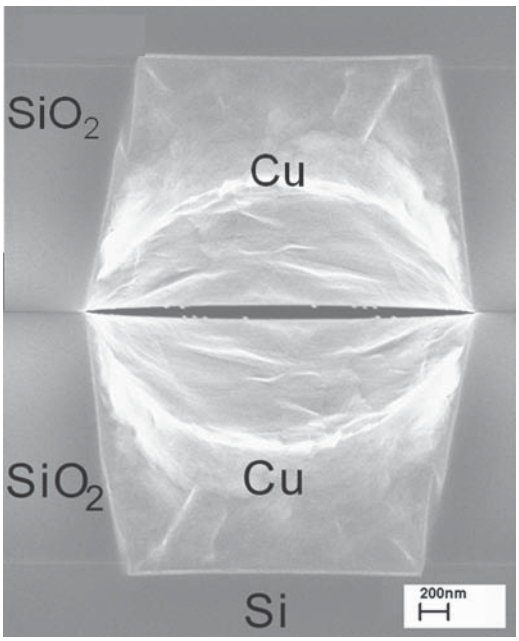

Fig. 1. A schematic diagram showing two standard SiO_2/Cu CMP patterns stacking together.

this small recess results in sub-optimal topography for Cu bonding as the hard oxide surfaces will contact first, thus hindering the contact of Cu at the center of the bond pad. Cu interconnects with various diameters and pattern densities have been fabricated. One option to address this issue is to utilize an optimized Cu reflow process, however the wafer-level yield of this method is difficult to achieve. Therefore, we have developed an approach to recess the oxide below the Cu surface in the order of nanometers, allowing that Cu pads can contact first. In the optimal recess case, when the Cu compresses due to its soft physical property, the oxide surfaces would simultaneously be brought in contact with each other.

The following methods to create pads with oxide recessed below the Cu level are tested: (1) SiO_2 CMP process, (2) dilute hydrofluoric acid (HF) wet etch for 3 or 5 minutes, and (3) a combination of SiO_2 CMP process and dilute HF wet etch. The height of the Cu bond pads (the distance between the Cu and SiO_2 surfaces) and surface roughness were evaluated using profilometry, indicating an oxide recess of 40 to 100 nm.

The first method utilized a SiO_2 CMP process to recess the oxide level. Figure 2 shows the profilometry trace of the Cu pad height (the distance between Cu and SiO_2 surfaces) and surface roughness post-processing. The profile of the Cu pads became dome/round shaped after processing because some Cu near SiO_2 has been removed during the SiO_2 CMP process. As a result, an average recess of 40 nm was achieved at the center of the pad and 30 nm at the pad edge.

The second method to recess oxide uses dilute hydrofluoric acid (HF) wet etch. The time of etch was optimized to

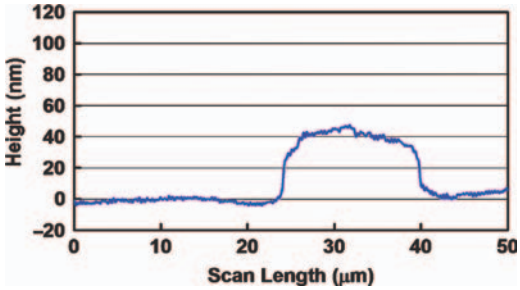

Fig. 2. Profilometry measurement of the height of Cu pads (the distance between Cu and SiO_2 surfaces) and surface roughness after SiO_2 CMP process.

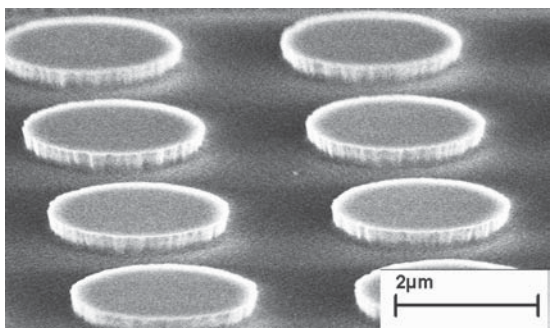

Fig. 3. SEM image of surface morphologies of Cu interconnects after a combination of SiO_2 CMP process and dilute HF etching.

3 minutes to achieve the same oxide recess, namely 40 nm. The silicon dioxide etch rate in dilute HF was approximately 20 nm per min. In contrast to the surface profile after SiO_2 CMP process, the shape of the Cu pads after HF etch is generally flat across the pad because HF does not react with Cu.

The third method uses a combination of first two methods, namely SiO_2 CMP process followed by dilute HF wet etch 3 min. As the result of this combination process, a 100 nm of oxide recess has been achieved. The shape of Cu pads resembles a "dome" shape as a result of the SiO_2 CMP step. The scanning electron micrographs (SEMs) of the Cu pad surface morphology after the combined process are shown in Figure 3.

3. Cu BONDING AND QUALITY ANALYSIS

Prior to the bonding process, wafers were dipped in dilute HCl for 30 seconds to remove the surface copper oxide. The wafer-level bonding process was carried out in an EV Group 501 bonder. Nitrogen was purged before the chamber was evacuated to 2×10^{-4} torr, and then a 1,000 N force was applied to the stacked wafer pair. The temperature was then ramped up to 400 °C at a rate of 32 °C/min, upon which a 10,000 N force was applied for 1 hr to complete bonding. Finally, the bonded wafer pair was kept under vacuum in the chamber until it had cooled down to room temperature.

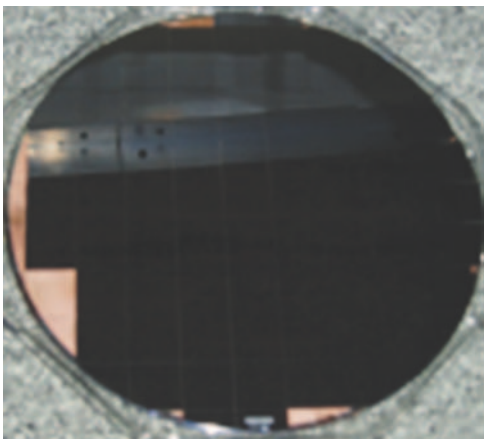

Fig. 4. Image of a bonded wafer (not optimized bonding condition) showing edge regions that did not survive dicing test.

A dicing method was used to examine the quality of the bonded interface. This reliability method is very important as it provides typical "stress" conditions induced upon chip during the packaging process. A typical "fail" of such method is depicted in Figure 4, indicating that the bond strength of the tested bonded wafer pair was too low to withstand dicing stress experienced during sawing.[10] Dies with insufficient bonding strength detach indicating weak bond areas.

Table I describes Cu-oxide topography for each recess method tested and lists the number of dies that failed during dicing test for bonded wafer pairs, respectively. In general, for the same height of oxide recess (∼40 nm) the HF etch method provided a better bonding quality than the process that utilized SiO_2 CMP step to recess oxide solely. The HF etch method resulted in a uniform recess level across wafer, regardless of the pattern size, density and location. It is believed that since HF etch process results in the flat surface of the Cu pads it may not be optimized for bonding, and hence it still results in some unbonded areas.

Conversely, SiO_2 CMP process creates a dome shape which is the preferred surface profile for a good initial bonding contact. During bonding process, two dome-shaped Cu bond pads can contact at the pad center first then deform to complete bonding process to the pad edge. However, the depth of the oxide recess created by this method varies with the pattern density, size and wafer location providing variable surface topography. Under this circumstance, the negative effect of non-uniformity of SiO_2 CMP dominates over the positive effect of the pad shape, creating more non-bonded areas than in the HF etching process case.

If we choose the combination of SiO_2 CMP followed by HF etching process, the SiO_2 CMP process provides the most desirable "dome-shaped" Cu bond pad profile while the HF dip improves the Cu bond pad height uniformity across the wafer. Therefore, this "combined" method results in the strongest bonding quality and successfully withstands the dicing process.

Table I. Summary of Cu surface profiles and dicing failure results under different process techniques.

	SiO_2 CMP	Dilute HF 3 min etching	Dilute HF 5 min etching	SiO_2 CMP + Dilute HF 3 min etching
Average Cu height over oxide (nm) prior bonding	40	40	80	100
Cu surface shape	Round	Flat	Flat	Round
Percentage of failure sites after dicing test (total 198 sites) (%)	19.7	11.1	8.6	1.0

4. SEAL CONCEPT FOR IMPROVING BOND INTEGRITY

After wafers have been stacked through bonding, additional fabrication steps are required to complete the 3D assembly process. These generally include wafer thinning steps which expose the wafers to wet chemistries; dielectric deposition steps which expose the wafers to high temperatures and plasma environment; plating steps which expose the wafers to various etchants; and lastly, the dicing step which results in exposure to particulates. All of these steps may cause degradation to the bonded interface and therefore result in reliability degradation.[11] To address these issues, a hermetic seal design that surrounds and seals (a) each individual chip, (b) all bonded structures and (c) the entire wafer is developed. These seals enable a full-wafer downstream processing and can be utilized for electrical signal propagation, thermal dissipation and additional mechanical stability to the structure.

Seals that surround an individual chip would usually be included in the layout of the Cu bond pad level so that they would be processed simultaneously. If the density of Cu bond pads used for electrical signal propagation is low, it would be necessary for the design to include additional bond structures in the field of the die area to provide mechanical stability and more uniform bonding

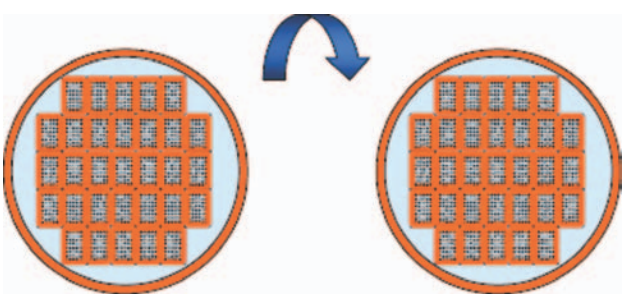

Fig. 5. Schematic diagrams illustrating two wafers to be bonded with potential seal locations at the edges of chips and wafers.

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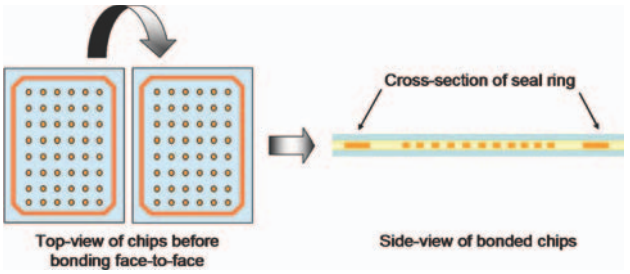

Fig. 6. Schematic diagrams illustrating potential seal and pad configuration (a) before and (b) after bonding.

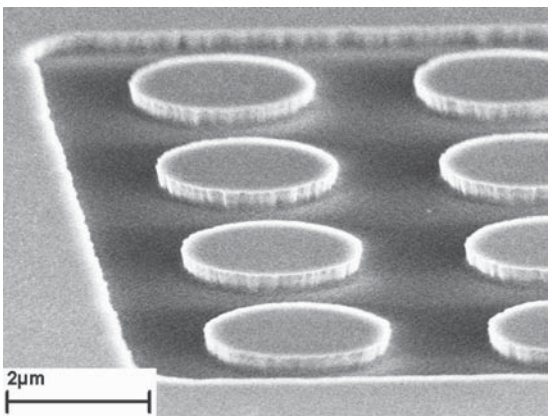

Fig. 7. SEM image showing an example of Cu interconnects surrounded by a Cu seal design.

areas. These seals also contribute to the stability during backside processing of the wafers such as wafer thinning.

Once the structures have all been fabricated, the two face-to-face wafers would be aligned and bonded as depicted in Figure 5. Figures 6(a) and 6(b) show how inner Cu bond pads would be protected from liquid and gas etchants/corrosives and particulate materials by the die level seal ring. In addition, the seals provide mechanical stability to the outer-most bonded Cu pads. An example of Cu interconnects surrounded by the seal design is shown in Figure 7.

5. CONCLUSION

In conclusion, we report a CMOS-compatible nano-fabrication method to improve Cu bonding quality by implementing new surface preparation step prior bonding process, and by optimizing the pattern design layout. Three methods to obtain such a nano-scale oxide recess were studied. The results show that a combination of SiO_2 CMP process and dilute HF wet etching processes provided the optimum bonding quality. The importance of Cu bond quality in demonstrating high yield, reliable, 3D circuits is also discussed. In addition, a seal design was introduced at the same level as the Cu bond pads to enhance bonding quality and prevent damage during processing. The seal design can be implemented as a wafer or die level seal, and a mechanical protection for specific low density interconnect or pad areas. These nano-fabrication process and seal demonstrations make significant steps towards achieving reliable and manufacturable 3D integrated circuits and packages.

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Investigation and Effects of Wafer Bow in 3D Integration Bonding Schemes

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This paper investigates and reviews the effects of wafer bow in three-dimensional (3D) integration bonding schemes, including copper wafer bonding and oxide fusion wafer bonding with silicon on insulator (SOI)-based layer transfer technology. Wafer bow criteria for good bonding quality and fabrication techniques to minimize wafer bow are introduced for 3D integration technology and applications.

Key words: Wafer bow, wafer bonding, 3D integration

INTRODUCTION

Research on the behavior of thin films on substrates has been widely investigated because of their applications in microelectronics.[1–8] Some of these studies on thin films used substrate curvature methods,[2–4,6] which correspond to the measurement of wafer bow. Wafer bow is obtained from the measurement of the overall magnitude of wafer curvature, and usually refers to the height deviation between the center and the edge of a wafer. Wafer bow may result from the device fabrication process or thin film/device stress on the wafer substrate. Since wafer bonding relies on the surface flatness of the two wafers,[9] wafer bow may play an important role in stacking or bonding quality.

In addition, wafer-bonding technology, including copper (Cu) and oxide wafer bonding, has been widely applied in 3D integration application.[10] Wafer bonding has attracted the attention of many researchers.[11–13] Some studies have investigated the materials properties of the bonded layer.[11,13] The relationship between bonding temperature and bonding quality has been investigated as well.[12] However, there is no report about the effect of wafer bow on wafer-bonding quality and methods to minimize wafer bow. Understanding the effect of wafer bow is also helpful to accurately study other bonding parameters. This paper reports the effect of wafer bow on Cu bonding quality under different bonding temperatures. In addition, wafer bow evolution during SOI-based device fabrication for oxide fusion bonding is reviewed. A process technique, post bow compensation, is reviewed and introduced for wafer bow minimization. Finally, suggestions to minimize effects of wafer bow during the bonding process are proposed for 3D integration.

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WAFER BOW IN Cu WAFER-BONDING SCHEME

Experimental Procedures

Wafer bows of unprocessed bare 4-inch (100) prime silicon wafers within the range between −20 μm and 20 μm were investigated in this study. Wafer bows of each silicon wafer before and after depositing 50 nm tantalum (Ta) and 300 nm Cu by electron-beam deposition were measured using a KLA-Tencor thin-film stress measurement. Wafer bow of unprocessed wafers before metal thin-film deposition will be referred to as “initial wafer bow” in the following discussion for convenience.

Two wafers with similar initial wafer bows were chosen as the bonding pair. After Ta and Cu deposition, these two wafers were bonded face to face

using an Electronic Vision EV 450 aligner and AB1-PV under pressure of 4000 mbar for 30 min at a 200°C, 300°C, and 400°C in ambient of 10^{-3} Torr. A DAD-2H/6T automatic dicing saw was used to cut bonded wafers into 5 mm × 5 mm square pieces at a speed of 0.69 mm/s. After the bonded wafer is sawn into pieces, one bonded piece may stay bonded or separate due to the force applied during sawing. The latter case is denoted here as "dicing failure." This approach allows us to characterize bonding quality for different initial wafer bows.

To simulate the *in situ* wafer bow at the bonding temperature, some wafers with different initial wafer bows were subjected to thermal heating from room temperature to 400°C at a ramp rate of 0.4°C/s to measure the evolution of wafer bow. The surface of the Cu film during heating and measurement was capped to avoid oxidation. The ramp rate is similar to the heating rate of the bonding process. In each case, *in situ* wafer bow measurements were taken at 10°C intervals to monitor the change of wafer curvature.

Results of Wafer Bow Measurements and Dicing Analysis

Figure 1 shows an example of wafer bow evolution during the heating process from room temperature to 400°C. The *Y*-axis represents the change of wafer bow at each step of measurement relative to the initial wafer bow, which is set at zero. Immediately after depositing Ta and Cu films, the change of wafer bow is −3 μm due to the difference of thermal expansion coefficient between Si and the metals. For other wafers with the same deposition conditions, the change of wafer bow immediately after deposition usually varies from −2 μm to −5 μm. Then the change in the wafer bow becomes less negative during the heating process. However, a more negative change in the wafer bow is observed from 150°C to 200°C. This is because of the microstructure evolution, which includes grain growth of the Cu film.[5,8,14] Afterwards, the change of wafer bow becomes less negative again with increasing temperature until it reaches zero and then becomes positive.

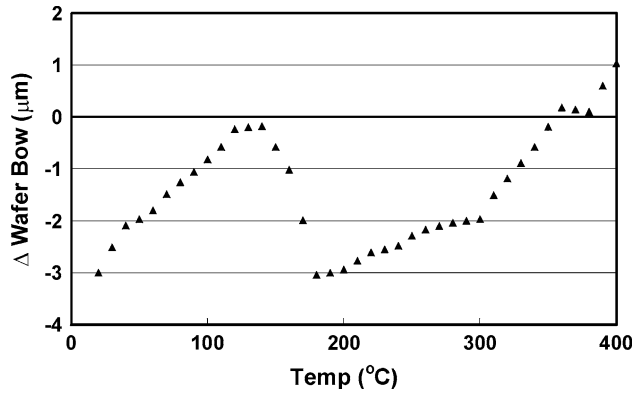


Fig. 1. An example of wafer bow evolution during the heating process from room temperature to 400°C. "Δ Wafer Bow" indicates the difference of wafer bow relative to the initial wafer bow.

Table I. Average change of wafer bow at different temperatures relative to the wafer bow after Ta and Cu film deposition

	200°C	300°C	400°C
Average change of wafer bow from room temperature to heating temperature	+0.3 μm	+1.1 μm	+4.2 μm

Table I lists the average values of wafer bow change at different temperatures relative to the wafer bow after the deposition of the Ta and Cu films; these are average values of measurements from different wafers. The reason for using the wafer bow after metal film deposition as the reference point is that the initial wafer bow varies from wafer to wafer. By applying the information in the table, it is possible to estimate the wafer bow value at the bonding temperature and to understand the relation between wafer bow, bonding temperature, and bonding quality.

Bonding quality mostly depends on the wafer bow at the bonding temperature, but not on the initial wafer bow. Table II shows an example of six pairs of wafers selected to be bonded at 300°C. Each pair includes one top wafer and one bottom wafer. Wafer bows of each silicon wafer before and after metal film deposition were measured. The possible wafer bows at 300°C were also estimated based on the information in Table I. To show the effect of wafer bow on bonding quality clearly, in addition to the absolute values of failure pieces during dicing, the relative values are shown. The value of the lowest dicing failure percentage of the bonded wafer is set as zero. The bonded wafer with the lowest dicing failure percentage can be treated as the strongest bonded wafer in the group. For other wafers, the values of dicing failure percentage are the differences from this lowest dicing failure percentage. By using the method, it is easy to determine the strongest bonded wafer and understand the effects of wafer bow on bond strength.

Discussion

In Table II, the dicing failure percentage increases with increasing bow of the wafers to be bonded, for both larger positive and negative values. Pair K showed the strongest wafer-bonding quality. However, it should be noted that pair K did not have the flattest initial wafer bows. In addition, for pair J, with the lowest initial wafer bows, a 2% increase of dicing failure was observed. Therefore, it is suggested that the factor that determines bonding quality is the wafer bow at the bonding temperature and not the initial wafer bow.

Table II. Relative dicing failure percentages of wafers with different initial bows when bonded at 300°C

	Wafer Bow (μm)			Absolute Dicing Failure Percentage	Relative Dicing Failure Percentage
	Initial	After Ta and Cu Deposition	At 300°C (Based on Table I)		
G					
Top wafer	−13.53	−16.77	−15.67	13	+11
Bottom wafer	−13.26	−16.89	−15.79		
H					
Top wafer	−8.70	−11.80	−10.70	10	+8
Bottom wafer	−8.52	−11.67	−10.57		
I					
Top wafer	−4.43	−6.77	−5.67	6	+4
Bottom wafer	−5.36	−7.05	−5.95		
J					
Top wafer	−0.40	−4.14	−3.04	4	+2
Bottom wafer	0.10	−4.20	−3.10		
K					
Top wafer	4.79	−0.20	0.90	2	0
Bottom wafer	5.03	0.50	1.60		
L					
Top wafer	10.28	6.89	7.99	6	+4
Bottom wafer	9.99	6.25	7.35		

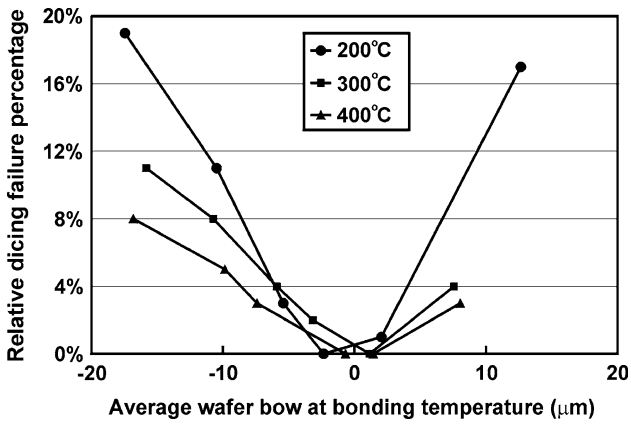


Fig. 2. Relation between wafer bow and bonding quality at different bonding temperatures; average wafer bow is the average wafer bow of the two wafers to be bonded.

Figure 2 shows the relationship between wafer bow and bonding quality for different bonding temperatures. Pairs of wafers with similar initial bows at the desired bonding temperature were bonded. These wafer bows at the bonding temperature were determined from the initial wafer bows and the corresponding wafer bow changes in Table I. Since the wafers of each pair have similar wafer bows, average values of two wafer bows from each wafer pair are used in the figure. It is clear that larger wafer bows result in higher relative dicing failure percentages. When bows of wafers to be bonded increase in magnitude, either positively or negatively, the dicing failure percentage increases. Bonded wafer pairs with lower initial wafer bows have lower failure percentages. Generally speaking, the effect of wafer bow is not obvious when the wafer bow at 200°C, 300°C and 400°C is smaller than ± 5 μm, ± 8 μm, and ± 10 μm, respectively.

Larger wafer bow results in greater local separation between the two surfaces at the beginning of bonding. Although the bonding pressure and the interdiffusion process during bonding can decrease and eliminate a small separation between the two surfaces, there are still some areas that are not close enough and therefore cannot be bonded well when this separation is large. This also explains why the failure percentage does not change much when the wafer bow is small, but increases dramatically when the wafer bow is large.

The effect of wafer bow on bonding quality decreases with increasing bonding temperature. The increase of the dicing failure percentage only reaches 11% when the wafer bows at 300°C are more negative than -15 μm, while with similar wafer bow at 200°C it can reach 19%. In addition, the increase in the relative dicing failure percentage only reaches 8% when the wafer bows are more negative than -15 μm at 400°C. At higher bonding temperature, the greater thermal energy during bonding strengthens the diffusion process within the bonded layer, and the bonding quality is further improved. Therefore, the effect of wafer bow can be balanced by higher bonding temperature to improve bonding quality.

In addition, the failure regions of bonded wafers with positive bows are always located at the edge area, while those with negative bows are located at the center of the wafers. Figure 3 shows a schematic diagram of these two different failure mechanisms.

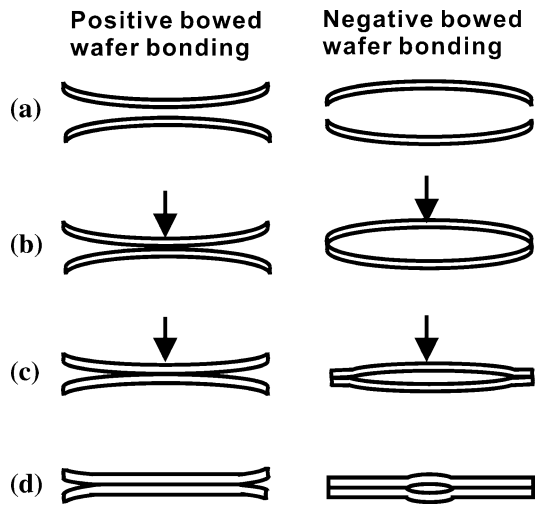


Fig. 3. Schematic diagram of two failure mechanisms for wafers with different types of wafer bow.

Since the bonding force is applied by using a small pin of the bonder to press the center of the upper wafer, the bonding procedure can be treated as if the upper wafer were pressed at the center by a single-point force, as shown in Fig. 3a. In Fig. 3b, when the force is applied to the upper wafer at the bonding temperature, the first contact point of positively bowed wafers is the center area, while the first contact point of negatively bowed wafers is the edge area. The bonding process, including interdiffusion across the interface and grain growth, completes first in the first contact region. Then, the bonded area propagates into neighboring areas until the whole wafer is bonded during the bonding process, as shown in Fig. 3c. However, the total bonding area across the wafer depends on the thermal energy, determined by the bonding temperature and duration, applied by the system. In addition, the initial wafer bow determines the force required to bring the two curved surfaces together for bonding. Therefore, for limited bonding duration at low bonding temperature, two bowed wafers may not be able to bond across the whole wafer, as shown in Fig. 3d. The remaining unbonded area, which had the largest separation between the two surfaces prior to bonding due to the wafer bows, cannot survive the dicing test. Higher bonding temperature or lower initial wafer bow will generate better bonding quality across the wafer.

The common approach to determine the quality of wafer bonding qualitatively is the dicing method. During dicing, well-bonded regions stay bonded while poorly bonded regions separate due to the applied stress. The poorly bonded regions occur at the edge of positively bowed wafers and at the center of negatively bowed wafers (Fig. 3). Figure 4a shows a bonded wafer with a perfect bonding result, while Fig. 4b shows another wafer for which the

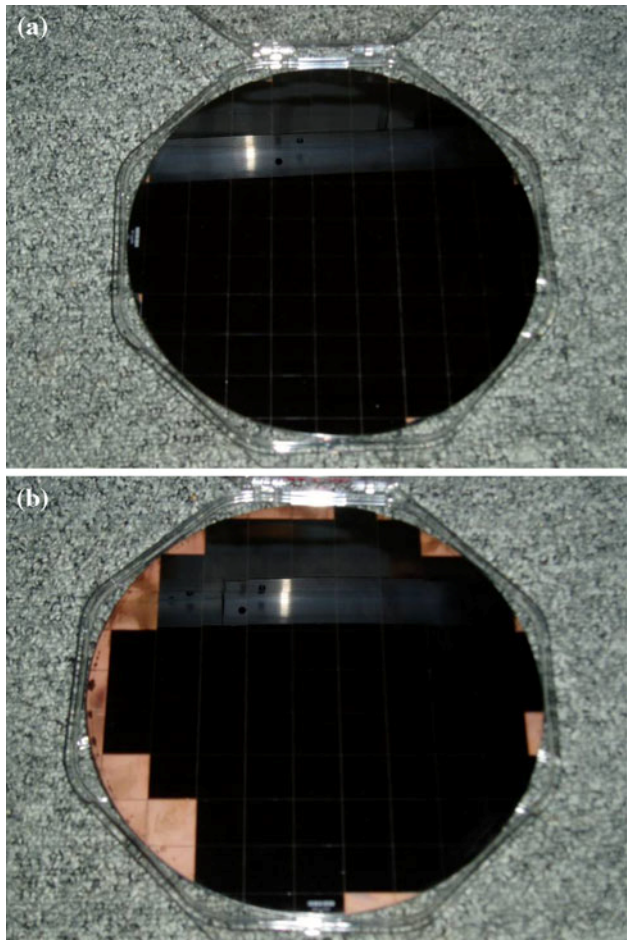


Fig. 4. Images of (a) a well-bonded wafer, and (b) a bonded wafer with poorly bonded regions at the edge after dicing tests.[15]

edge region failed after bonding.[15] In Fig. 4b, the two wafers did not bond optimally as both had positive bows before bonding, a result that is consistent with the prediction based on Fig. 3.

Material characterizations of unbonded and bonded areas can be carried out by transmission electron microscope (TEM), as shown in Fig. 5a and b.[16] As shown in Fig. 5a, the well-bonded area has perfect bonding quality and no obvious bonding interface can be observed. The poorly bonded region can be observed directly in the TEM image in Fig. 5b, and from scanning electron microscope (SEM) and dicing results. The characterization results provide guidelines to determine the bonding parameters for 3D integration.

Since Cu wafer bonding is becoming an attractive choice for future three-dimensional integration,[10] the results from this wafer bow investigation offer an important reference for initial wafer selection. To achieve high-quality bonding, the wafer bow should be considered. By applying the criterion of wafer bow described herein, the effect of wafer bow on bonding quality can be effectively avoided.

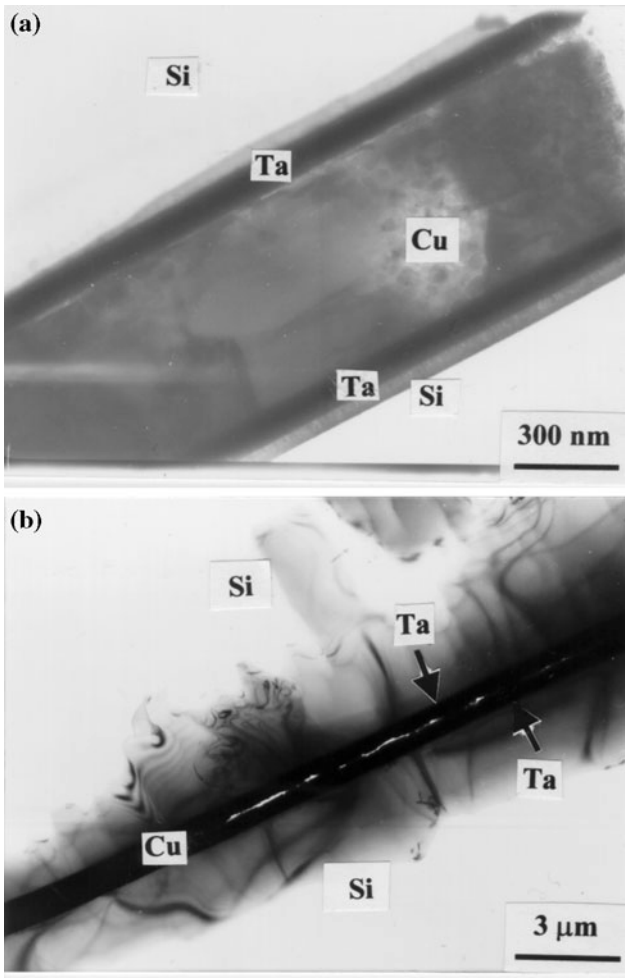


Fig. 5. Cross-sectional TEM images of (a) a well-bonded Cu interface, and (b) a poorly bonded Cu interface at the edge of a bonded wafer.[16]

WAFER BOW IN OXIDE BONDING BASED ON SOI WAFER SCHEME

Scheme Introduction

In this section, wafer bow effects in the scheme of oxide bonding based on SOI wafers are reviewed.[15,16] This 3D integration scheme is also known as the "layer transfer process." A schematic diagram of this scheme is shown in Fig. 6.[17] The top wafer, an SOI wafer, is first attached to a glass handle wafer, followed by removal of the original substrate, as shown in Fig. 6a. In Fig. 6b, the top wafer can be aligned and oxide-bonded to the bottom wafer. Finally the 3D stacked structure (Fig. 6c) can be achieved by releasing the glass handle wafer.[17]

Wafer Bow Evolution in Fabrication Steps

It is interesting to know the relation between wafer bow and each wafer fabrication step. Therefore, the evolution of wafer bow was recorded

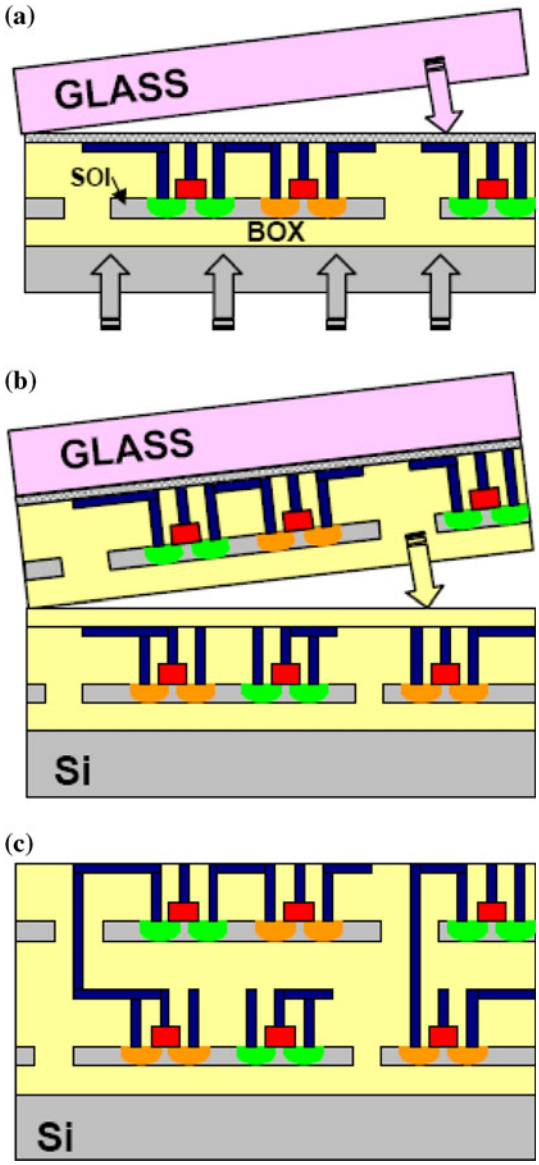
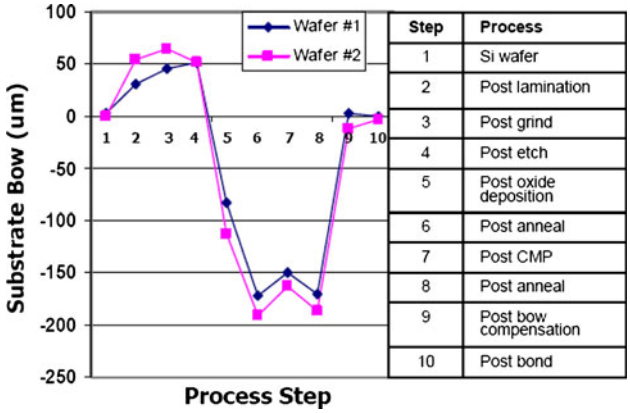


Fig. 6. Schematic diagram of 3D integration based on oxide bonding with SOI wafers: (a) the top SOI wafer is attached to a glass handle wafer, followed by removal of the original substrate; (b) the top wafer is aligned and then oxide-bonded to the bottom wafer; (c) the final 3D stacked structure is achieved by releasing the glass handle wafer.[17]

step by step, as shown in Fig. 7.[18] Two wafers with almost zero bow were selected for the oxide bonding process. The bow became positive (<100 μm) in the first few steps prior to oxide deposition,[18] and this value should be adequate to achieve good bonding quality in the subsequent bonding process at this point.

However, once the oxide was deposited, the bow became drastically negative. In step 6, after the postannealing treatment, a huge bow of approximately -200 μm was measured. The bow did not change much after steps 7 and 8.[18] This large wafer bow was not acceptable for subsequent oxide bonding.



Step	Process
1	Si wafer
2	Post lamination
3	Post grind
4	Post etch
5	Post oxide deposition
6	Post anneal
7	Post CMP
8	Post anneal
9	Post bow compensation
10	Post bond

Fig. 7. Bow measurement at various fabrication steps in the 3D integration process introduced in Fig. 6.[18]

Wafer Bow Compensation

To overcome this issue, an additional process step, called post bow compensation, was introduced to compensate for the wafer bow.[18] As shown in step 9 of Fig. 7, the bows of both wafers could be minimized to around zero again. No obvious wafer degradation after oxide bonding was observed with the final bonded wafer bow around zero.[18] Post bow compensation can be accomplished by thin-film deposition on the backside of both wafer substrates.

CONCLUSIONS

The effects of wafer bow on bonding quality were investigated. Bonding quality degrades with high wafer bow during bonding, especially at low bonding temperature. The effect of wafer bow on bonding quality at different bonding temperatures was explored. A physical mechanism is discussed to explain the relation between bonding quality and bonding parameters. The wafer bow evolution and bow compensation method of oxide bonding based on SOI wafers are reviewed and discussed. The criterion of wafer bow for good bonding quality and the compensation method can be applied in future device applications.

ACKNOWLEDGEMENTS

This research is supported by the Republic of China National Science Grant Council (Grant No. NSC 98-2218-E-009-013-MY2). The authors acknowledge support from National Chiao Tung University, IBM T.J. Watson Research Center, and Massachusetts Institute of Technology.

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Reliability and structural design of a wafer-level 3D integration scheme with W TSVs based on Cu-oxide hybrid wafer bonding

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Abstract

We demonstrate a wafer-level 3D integration scheme with W TSVs based on Cu-oxide hybrid wafer bonding. Hybrid Cu-oxide hybrid bonding shows excellent bond quality and performances in terms of alignment, bond strength, and ambient permeation oxidation. Excellent performances of initial reliability and quality evaluations for Cu-oxide hybrid bonding are key milestones in proving manufacturability of 3D integration technology.

Introduction

Wafer-level 3D integration based on Cu bonding technology is an attractive option for next generation circuit fabrication [1-3]. Although pattern Cu wafer bonding techniques, including oxide-recessed or hybrid bonding with adhesives, were explored [4-6], these approaches may result in reliability concerns due to air gaps and polymers used. Therefore, a reliable polymer-free 3D integration structure will be a good candidate in different 3D schemes. In this study, we demonstrate a wafer-level 3D integration scheme with W TSVs based on Cu-oxide hybrid wafer bonding without any polymers. In addition, lock-n-key structure is designed to fulfill Cu-oxide hybrid wafer bonding. Cu-oxide hybrid bonding using lock-n-key structure has better performances than those of Cu bonding with oxide recessed.

Bond Structure Design and Alignment Evaluation

Figure 1 shows the two bond structures without polymers, "oxide-recessed" and "lock-n-key", considered in this study. "Oxide-recessed" structure is a conventional bond structure in 3D integration. The concept of this structure is to recess the level of surrounding dielectrics, such as oxide, and then metal joins can be fully contact during bonding.

For the lock-n-key structure, the "lock" part is achieved by recessing Cu, while the "key" part is fabricated with recessing oxide. The recessed amounts of both parts are carefully fabricated to make sure two Cu surfaces can contact during bonding. In addition, the advantage of lock-n-key structure is that oxides from both wafers can be simultaneously bonded during Cu bonding, the so-called Cu-oxide hybrid bonding.

For lock-n-key structures, the area of Cu "lock" has to be larger than that of Cu "key" to confine the misalignment value, which make two wafers cannot be bonded at large misalignments, as shown in Fig. 2(a). In other words, misalignments of bonded lock-n-key wafers are always within the tolerance, which guarantees the bond quality, as shown in Fig. 2(b).

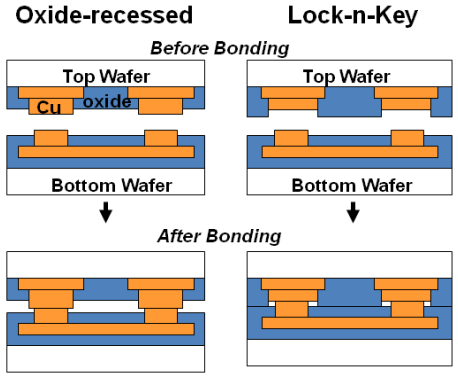

Fig. 1. Schematics of three different bonding structures.

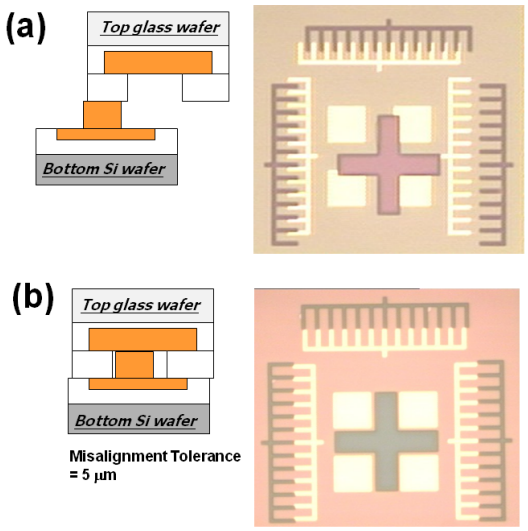

Fig. 2. Schematic and image of lock-n-key structures for (a) a bad alignment out of tolerance; (b) an alignment within tolerance.

In the alignment study, only the effect of alignment process is considered. Therefore, all wafers were investigated after alignment before bonding. Fig. 3 shows alignment accuracy evaluation of 20 successful trials on (a) oxide-recessed and (b) lock-n-key (5 μm tolerance) structures. The size of Cu patterns on top wafers is 10 μm, while that on bottom wafers is 20 μm. In Fig. 3(a), we observe high misalignments of oxide recessed structures in the first several alignment trials because of new pattern recognition process for alignment tool. On the other hand, the results of lock-n-key structures are always confined within the misalignment tolerance if two structures are successfully aligned for bonding.

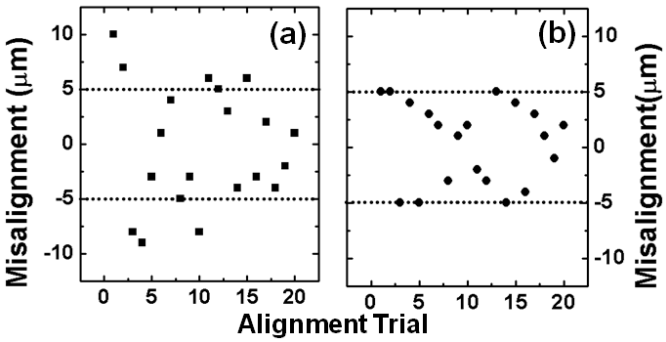

Fig. 3. Statistics of misalignment results for 20 studies of (a) oxide-recessed and (b) lock-n-key (5 μm tolerance) structures.

Reliability and Bond Strength Evaluation

After alignment process, wafers with two types of bonded structures were bonded at 400°C for 1 hour under a 10,000 N force in the ambient of $2x10^{-4}$ torr. The ramp rate was 6°C/min. The bonded wafers for two types of bonded structures were then diced with water for oxidation test (200°C, 70 hr, in atmosphere).

As the results shown in Fig. 4, the lock-n-key structures in Fig. 4(a) still show clear well-bonded structure, indicating excellent ability to against corrosion. On the other hand, it is clear in Fig. 4(b) that some patterns of Cu bonded oxide-recessed structures have become dark and dirty with corrosion and oxidation evidences. Because of the open air gap between two wafers, Cu bonded structures are easily reacted with materials from outside to result in corrosion and oxidation issues.

The preliminary reliability test indicates that lock-n-key structures have better performances than oxide-recessed ones. However, a reliability guideline for bonded structures or 3D integration technology is required. Then, a detailed complete reliability test is necessarily for these structures before they can be applied in any 3D integration products.

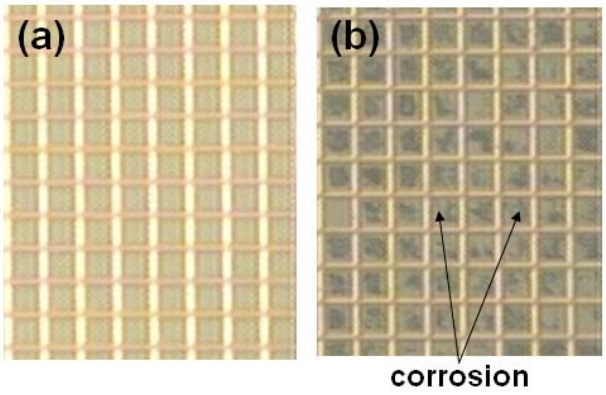

Fig. 4. Oxidation test showing (a) lock-n-key structures have better anti-corrosion ability than that of (b) oxide recessed ones

Matrix of pattern designs and two bond structures were designed to compare the bonding strength of different bond pad sizes (2.5 μm, 5 μm, and 10 μm) and bond pitches (22.5 μm, 25 μm, and 30 μm) by 4-point bending test. A combination of one small signal bond pad (2.5 μm) and one large dummy bond pad (10 μm) was also considered in this study. The matrix design and corresponding bond strength results are listed in Table 1.

Table 1 Bond strengths of different bonding structures and pattern designs from 4-point bending tests.

Signal Bond Pad (μm)	Dummy Bond Pad (μm)	Pitch (μm)	Bonding Structure	Bond Strength (F_{lbs})
10	10	30	Oxide Recessed	14
5	5	25	Oxide Recessed	9
2.5	2.5	22.5	Oxide Recessed	8
2.5	10	30	Oxide Recessed	11
10	10	30	Lock-n-Key	14
5	5	25	Lock-n-Key	12
2.5	10	30	Lock-n-Key	12

The bond strength is generally increased by enlarging the bond size or shortening the bond pitch (increasing the bonding density), both for oxide-recessed and lock-n-key structures. The trend is identical to previous quantitative results [4]. In addition, the bond strengths of lock-n-key structures are higher than those of oxide-recessed ones. This is because of the extra contribution of oxide-oxide bonding for lock-n-key structures. Figure 5 shows the characteristics of 4-point bending result on 10 μm bond pads. Although the numbers of bond strength in Table 1 and Figure 5 need further investigation and analysis for the mechanical meaning, the comparison results of 4-pint bending tests provide good guidelines for designing good bond structures.

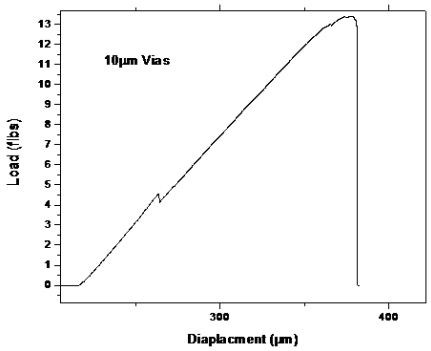

Fig. 5. Characteristics of one 4-point bending result.

Figures 6(a) and (b) show surface images of top and bottom wafers after 4 point-bending test. From the image of bottom wafer in Fig. 6(b), all the bonded structures are remained, indicating failures are located in top wafers, but not in the bonded interfaces, representing 100% bonded Cu pads.

From the preliminary reliability and bond strength tests, lock-n-key structures have better performances than oxide-recessed ones.

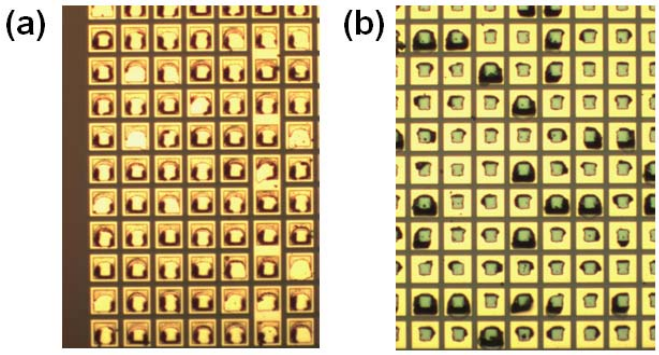

Fig. 6. Images of (a) top and (b) bottom wafers after 4-point bending test, showing a 100% bonding.

Dummy Bond Pad and Seal Design

From the results of previous study [4] and Table 1, maximizing the bond area improves the bond strength of whole structure. Therefore, dummy bond pad design becomes an option to enhance bond quality. Figures 7 (a) and (b) show the bonded chain surfaces without and with dummy bond pads after 4-point bending test. Some area of bonded chain without dummy pads did not survive the test, while those with dummy pads show 100% bonding. This result is identical to the trend shown in Table 1.

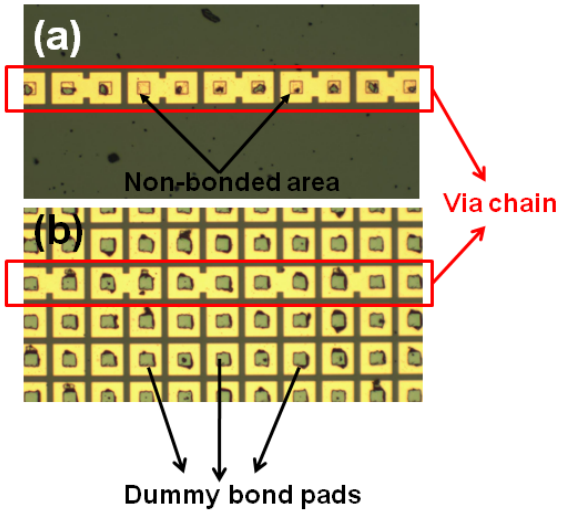

Fig. 7. Images of bonded via chains after bending tests: (a) without and (b) with dummy bond pads.

A seal pattern, which can protect inner structures and increase total bonding density, as shown in Fig. 8(a) was fabricated and then evaluated by using 4-point bending test. The failure region was happened at the Cu-TaN interface, but not Cu-Cu bonding interface, indicating a strong bond quality with seal structure, as shown in Fig. 8(b). The surface images after test in Figs. 8(c) and (d) support this failure scenario.

Wafer-Level 3D Integration Scheme with W TSVs

Lock-n-key bonded structures, with better performance than oxide-recessed ones based on above results, were fabricated to integrate with W TSVs to demonstrate a wafer-level 3D integration scheme. The schematic of the process flow is shown in Fig. 9. W TSVs were fabricated on top wafer by DRIE via etching and then W filling, as shown in Fig. 10(a) and (b). Cu "Key" structures were then fabricated above W TSVs on top wafers (Fig. 10(c)), while "Lock" ones on bottom wafers (Fig. 10(d)).

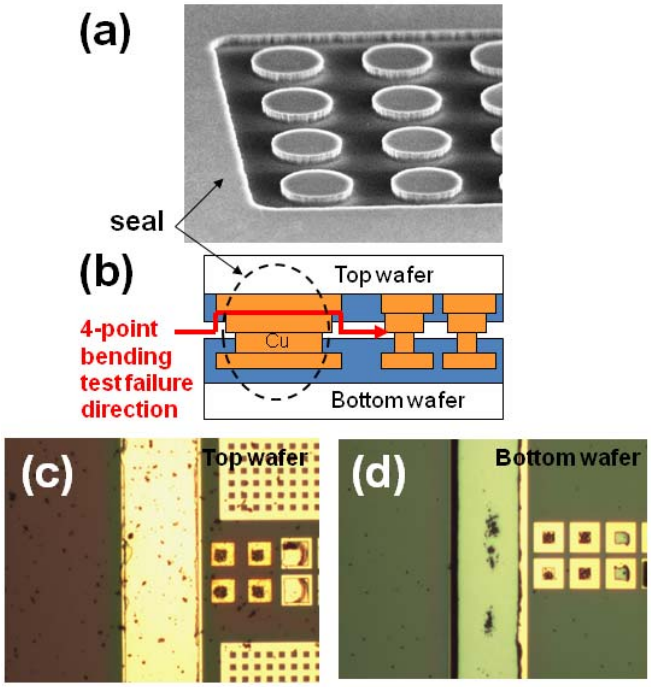

Fig. 8. (a) Image of seal structure before bonding; (b) Schematic diagram showing the failure direction during 4-point bending; (c) top and (d) bottom wafer images after bending test.

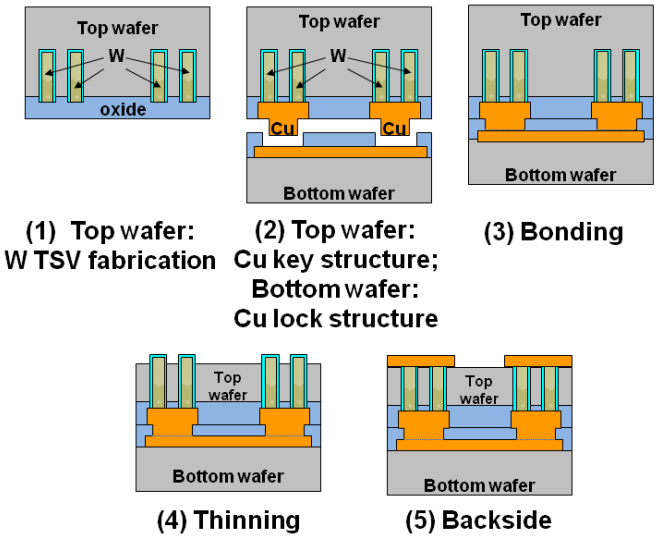

Fig. 9. Schematic diagram of process flow for wafer-level 3D integration scheme: (1) W TSV fabrication of top wafer; (2) lock-n-key bond structure fabrication; (3) Cu-oxide hybrid wafer bonding; (4) top wafer thinning to less than 47 μm and exposure of W TSVs ; (5) backside metallization to complete the process.

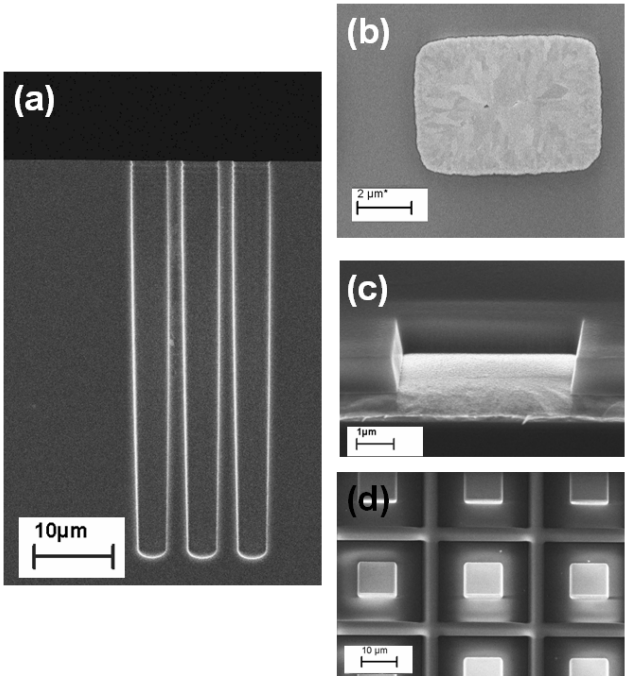

Fig. 10. (a) Cross-sectional SEM image of TSVs after DRIE etching, (b) Top down image of a W filled TSV, (c) a Cu "lock" structure for bonding, (d) Cu "key" structures for bonding.

One pair of top and bottom wafers were bonded and then grinded from the top wafer substrate to expose W TSVs. After backside metallization, the Cu-oxide hybrid bonded wafer with W TSVs is completed. Figs. 11(a) and (b) show this 3D integration scheme with 2.7 μm width of W TSVs and a 47 μm thickness of thin substrate.

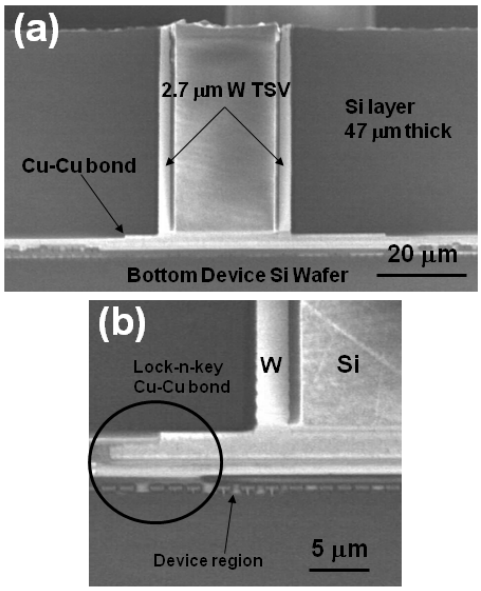

Fig. 11. (a) Image of lock-n-key Cu bond structure integrating 2.7 μm W TSVs in a 47 μm thick Si wafer; (b) no detectable Cu bonding interface of the bond structure.

A wafer-level 3D integration is demonstrated with Cu-oxide lock-n-key structure. As shown in Figures. 11(b), 12(a), and 12(b), the bottom device wafer was able to bond perfectly to the top thinned wafer with no bonding interface, and devices on the bottom wafer then can be connected to outside through W TSVs. Fig. 12(c) shows a defect-free 3D device wafer with this integration scheme.

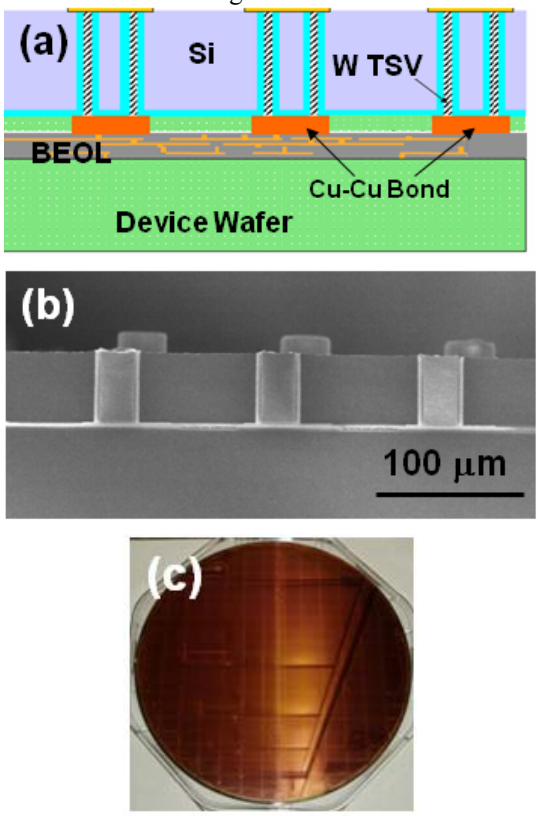

Fig. 12. Demonstration of wafer-level integration scheme with W TSVs using lock-n-key Cu-oxide bonding: (a) Schematic diagram; (b) XSEM image showing W TSVs in the thinned top wafer; (c) a defect-free 3D integration wafer with the structure described in (a) and (b).

Conclusions

A wafer-level 3D integration scheme with W TSVs based on Cu-oxide hybrid wafer bonding is demonstrated. Cu-oxide hybrid wafer bonding shows excellent performances of initial reliability comparison and quality evaluations. Designs of seal structure and dummy bond pads are proved to provide the enhancement of bonding in wafer-level 3D integration.

Acknowledgements

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國科會補助計畫衍生研發成果推廣資料表

日期:2011/05/20

國科會補助計畫	計畫名稱: 三維積體電路(3D IC)之矽晶直通孔(TSV)與其它關鍵技術製程整合研究及應力量測熱傳導模型分析(1/3)
	計畫主持人: 陳冠能
	計畫編號: 99-2628-E-009-093- 學門領域: 固態電子

無研發成果推廣資料

99 年度專題研究計畫研究成果彙整表

計畫主持人：陳冠能	計畫編號：99-2628-E-009-093-
計畫名稱：三維積體電路(3D IC)之矽晶直通孔(TSV)與其它關鍵技術製程整合研究及應力量測熱傳導模型分析(1/3)	

成果項目			量化			單位	備註（質化說明：如數個計畫共同成果、成果列為該期刊之封面故事...等）
			實際已達成數（被接受或已發表）	預期總達成數(含實際已達成數)	本計畫實際貢獻百分比		
國內	論文著作	期刊論文	10	3	100%	篇	
		研究報告/技術報告	0	0	100%		
		研討會論文	12	0	100%		
		專書	1	0	100%		
	專利	申請中件數	2	3	100%	件	
		已獲得件數	1	0	100%		
	技術移轉	件數	0	0	100%	件	
		權利金	0	0	100%	千元	
	參與計畫人力（本國籍）	碩士生	4	4	100%	人次	
		博士生	3	3	100%		
		博士後研究員	0	0	100%		
		專任助理	0	0	100%		
國外	論文著作	期刊論文	0	0	100%	篇	
		研究報告/技術報告	0	0	100%		
		研討會論文	0	0	100%		
		專書	0	0	100%	章/本	
	專利	申請中件數	0	0	100%	件	
		已獲得件數	0	0	100%		
	技術移轉	件數	0	0	100%	件	
		權利金	0	0	100%	千元	
	參與計畫人力（外國籍）	碩士生	0	0	100%	人次	
		博士生	0	0	100%		
		博士後研究員	0	0	100%		
		專任助理	0	0	100%		

其他成果 (無法以量化表達之成果如辦理學術活動、獲得獎項、重要國際合作、研究成果國際影響力及其他協助產業技術發展之具體效益事項等，請以文字敘述填列。)	無

	成果項目	量化	名稱或內容性質簡述
科教處計畫加填項目	測驗工具(含質性與量性)	0	
	課程/模組	0	
	電腦及網路系統或工具	0	
	教材	0	
	舉辦之活動/競賽	0	
	研討會/工作坊	0	
	電子報、網站	0	
	計畫成果推廣之參與（閱聽）人數	0	

國科會補助專題研究計畫成果報告自評表

請就研究內容與原計畫相符程度、達成預期目標情況、研究成果之學術或應用價值（簡要敘述成果所代表之意義、價值、影響或進一步發展之可能性）、是否適合在學術期刊發表或申請專利、主要發現或其他有關價值等，作一綜合評估。

1. 請就研究內容與原計畫相符程度、達成預期目標情況作一綜合評估 ■達成目標 □未達成目標（請說明，以 100 字為限） □實驗失敗 □因故實驗中斷 □其他原因 說明：
2. 研究成果在學術期刊發表或申請專利等情形： 論文：■已發表 □未發表之文稿 □撰寫中 □無 專利：□已獲得 ■申請中 □無 技轉：□已技轉 □洽談中 ■無 其他：(以 100 字為限)
3. 請依學術成就、技術創新、社會影響等方面，評估研究成果之學術或應用價值（簡要敘述成果所代表之意義、價值、影響或進一步發展之可能性）(以 500 字為限)