摘　　要

　　本報告包含本三年期計畫之全部成果。內容分為兩個部分：碳摻雜技術與對 NiSi/Si 結構之影響、全包覆式多晶矽薄膜電晶體。

在碳摻雜技術方面，我們採用電漿浸潤技術、一般離子佈植技術、低能量/低溫離子佈植技術三種。過低的電漿浸潤能量會造成碳膜沈積，無法形成 NiSi，必須避免。三種技術的碳摻雜劑量達到 1×10^{15} cm^{-2} 以上，都可以提高 NiSi 的熱穩定性達攝氏 50-100 度，但是如果同時有高劑量的 As, P, B 等摻雜，碳摻雜的作用則不明顯。低能量離子佈植技術可以形成品質最好的非晶矽層，搭配快速退火+雷射退火，可以得到最高的替代性碳濃度超過 1.1%，具實用價值。即使經過高溫退火，碳摻雜仍會增加矽基板的缺陷密度，Ni 可能藉由這些缺陷快速擴散，因此碳植入深度和接面深度必須適當搭配，以免接面漏電流增加。高劑量的碳摻雜可以微幅降低 NiSi/n-Si 的蕭基位障高度約 30meV，幅度不大，對於接觸電阻影響很小。

　　在全包覆式電晶體部分，以電子束微影、光阻消減、電漿蝕刻技術，製作通道寬度、長度均小於 30nm 的電晶體，通道厚度減薄到 8nm，搭配全包覆式閘極結構，達成全空乏型通道。再搭配修正蕭基位障接面技術，製作出通道長度 18nm 的世界最小的薄膜電晶體。進一步搭配高介電常數介電質，將驅動電流推進到 500μA/μm 以上，接近單晶矽電晶體，創下多晶矽薄膜電晶體的最大電流紀錄。

　　本計畫三年內有三名博士班研究生、六名碩士班研究生參與計畫執行。其中兩名博士生已經畢業，另一名預計一年內亦可獲得博士學位；六名碩士研究生中的四名已經獲得碩士學位。計畫成果已發表兩篇 SCI 期刊論文、五篇研討會論文，一篇期刊論文在審查中，另有一篇期刊論文、一篇研討會論文在撰寫中。以取得的數據，估計至少可以再發表 2-3 篇 SCI 期刊論文。

關鍵字：全包覆式電晶體、金屬矽化物、矽化鎳、碳摻雜、電漿浸潤。

Abstract

This final report summarizes all of the results of the 3-year project. This report is divided into two parts : effect of carbon incorporation techniques on the NiSi/Si structure and gate-all-around (GAA) poly-Si thin film transistor(TFT) technology.

In the part of carbon incorporation, plasma immersion ion implantation (PIII), conventional ion implantation, and low energy/low temperature ion implantation techniques were employed. Carbon film may be deposited on sample surface as the PIII energy is too low. In this case, the Ni/Si interaction will be blocked. All of the three techniques can raise the thermal stability of NiSi/Si by 50-100°C as the carbon dose is higher than $1\text{x}10^{15}$ cm^{-2}. However, with the high dose As, P, or B, this benefit disappears. The low energy ion implantation technique produces the highest quality surface amorphous layer among the three techniques. Low energy carbon ion implantation integrating with suitable rapid thermal annealing and laser annealing can obtain substitutional carbon concentration as high as 1.1%. This value is useful for strained Si application. Unfortunately, high dose carbon implantation produces many defects in Si substrate. These defects can not be fully removed after high temperature annealing. Ni atom may diffuse quickly via these defects and may results in higher p-n junction leakage current. The distribution of carbon and the junction depth should be designed carefully. High dose carbon incorporation may reduce the Schottky barrier height by 30meV on n-Si, which implies that the contact resistance will not be affected by carbon incorporation.

In the part of GAA TFT technology, e-beam lithography, photo-resist trimming, and plasma etching processes were developed to fabricate TFTs with channel length and channel with smaller than 30nm. Due to the 8-nm-thick ultra-thin active layer and the GAA gate structure, fully-depleted channel and good short channel effect is obtained. Integrating with the modified Schottky barrier source/drain junction, the record small TFT with 18-nm gate length is demonstrated. Using high dielectric constant dielectric to replace the SiO$_2$ gate dielectric, the record high driving current of 500 μA/μm is obtained. This driving capability is close to the conventional nMOSFET.

In the past three years, 3 Ph.D students and 6 graduate students involved this project. Among them, 2 of the 3 Ph.D student and 4 of the 6 graduate students have received their Ph.D and MS degrees, respectively. The other one Ph.D student is expected to receive his Ph. D degree in one year. Three undergraduate students have entered the MS program. Parts of the results have been published as 2 SCI journal papers and 5 conference papers. One SCI journal

is under revision. Recent results will be written as 2-3 SCI journal papers at least.

Contents

Part-I

Part-II

Chapter 1

Effect of Carbon Plasma Immersion Ion Implantation on the Thermal Stability of Nickel Silicide Film

1.1 Introduction

Plasma immersion ion implantation is a surface deposition technique, which applies high voltage pulsed DC or pure DC power to extract the accelerated ions from the plasma and targeting the ions into the wafer placed on the sample holder. Figure 1-1 is the schematic diagram of a PIII system, the holder is in a vacuum chamber which is connected to a high voltage power supply and insulated from the chamber wall. When the process begins, the substrate is applied with a negative bias, the electric field drives electrons away from the substrate and forms a Debye sheath layer. The Debye sheath layer contains only positive ion and no electrons in it. The biased substrate will accelerate the ions in the Debye sheath layer and implant the ions into the wafer on the holder.

The benefit of PIII process is that the implantation energy is controlled by the voltage of the pulsed DC signal, so the dopants can be implanted into the shallow region of the object surface by very low implantation energy. And because the object is totally immersed in the plasma, so PIII can implant high density of dopants into the wafer in a relatively short time compare to traditional ion implanter. In that way, the throughput of implantation process can be increase.

Several applications of PIII have been implemented by researchers. Using nitrogen PIII process to improve the surface property of stainless steel is one of the applications. By performing NPIII process, the surface hardness of stainless steel can be improved [1, 2]. Another important application is performing oxygen PIII on the metallic biomaterials which are used on medical purposes such as osteosynthesis plates used in jaw or skull surgery. After OPIII treatment, the biocompatibility of the biomaterials will be improved [3-7]. Diamond like carbon (DLC) film forming is another application of PIII [9-10]. The DLC film has a high hardness and Young's modulous, a good wear and abrasion resistance and a low friction coefficient. So it can be used in semi-conducting, biomedical, automotive and aerospace industries. And PIII is a promising way of efficiently forming DLC film on object's surface.

PIII has several applications on semiconductor device fabrication. First, because PIII can

do low energy ion implantation, it can be used on ultra-shallow junction fabrication. In the research of C.A. Pico et al., PMOS is successfully fabricated by using BPIII process [11]. PIII is also used on sidewall doping of trench structure [12]. Since PIII has immersion type doping characteristic, the sidewall doping of high aspect ratio trench structure is easier by using PIII. Nitrogen PIII can use on suppressing thermal hillock formation in aluminum metallization [13], or improve the electrical characteristics of high-k gated MOS devices [14].

In this chapter, we use PIII as carbon ion implantation source. First, we discuss the basic characteristic of the CPIII silicon substrate. Then the thermal stability improvement of CPIII on the NiSi/Si structure is discussed, both without As doping and with As doping samples are included.

1.2 Experimental Procedure

A. Carbon Plasma Immersion Ion Implantation (CPIII)

The PIII system used in this project consists of process chamber, electrical power system, vacuum system, and gas providing system. Fig.1-2 shows the whole PIII equipment. The process chamber is a chamber with sample chuck at the bottom and an antenna to light the plasma on. A valve control panel is linked to the chamber to control all the valves linked to the process chamber. Fig.1-3 shows the control panel of the valves. Fig.1-4 and Fig.1-5 show the electrical power system, it includes a DC power supply and a DC pulse signal source. The vacuum system includes two pumps and one pressure meter. One pump is for the first step vacuum to make the pressure down from air pressure, the other pump is a turbo pump which can make the chamber pressure down to 10^{-6} torr. The gas providing system includes CH_4 gas source and a gas flow meter.

At the beginning of the process, we put the wafer on the sample chuck. Then we use the vacuum system to make the chamber pressure down to 10^{-5} torr. After the process pressure reached, CH_4 gas is pour into the process chamber with a flow rate of 50 sccm. DC power supply is turned on to light on the plasma with a value of 150V. In the final step, DC pulse signal is applied to the chuck and the carbon ions are implanted into the silicon substrate, the process pressure is about 1.2×10^{-3} torr.

B. Sample Preparation

Six-inch-diameter p-type (100) silicon wafers with nominal resistivity of 15~25 Ω-cm were used as substrates. The PIII was performed at 3 keV and 5 keV, and the implantation

time is 1 min and 5 min. The samples are labeled in the form of xKyM, where the xK indicates the implantation energy is at x keV and the yM indicates the plasma immersion time is y min. After PIII, the 3K5M and 5K5M samples accepted additional arsenic ion implantation at 30 keV to a dose of 5×10^{15} cm^{-2}. Then, all samples were dipped in diluted HF solution with (H_2O：HF = 50：1) to remove the native oxide on sample surface. A 10-nm-thick Ni film was deposited by an E-gun system. The process pressure is 6×10^{-7} torr and the Ni deposition rate is 0.5A/sec. After Ni deposition, samples were cut into small pieces and were annealed in N_2 ambient by a rapid thermal annealing (RTA) system at temperatures ranging from 500 °C to 900 °C for 30seconds. The unreacted Ni was selectively etched by a mixture of H_2SO_4 : H_2O_2=3:1.

C. Material Analysis

Several Material Analysis techniques include XRD、SEM、SIMS and TEM were used in our experiment. Electrical measurement of sheet resistance was performed, too.

XRD analysis is used to find out the nickel silicide phase transformation temperature. Scanning Electron Microscope (SEM) is used to inspect the surface morphology of the carbon implanted nickel silicide samples after annealing at different conditions. The surface continuity and the level of agglomeration can be observed by SEM inspection. Secondary Ion Mass Spectrometry (SIMS) is used to analysis the depth profiles of carbon and phosphorus atoms in samples after ion implantation and annealing. Transmission Electron Microscopy (TEM) is used to observe the microstructure of samples. It can help to figure out the thickness of amorphous layer and the level of amorphization.

1.3 Basic Material Analyses of CPIII on Si Substrate

TEM was used to analyze the surface condition of the implanted silicon surface and SIMS was used to measure the depth profile of the carbon distribution after carbon plasma immersion ion implantation. Fig.1-6 and Fig.1-7 shows the SIMS result of the carbon implanted silicon substrate, we can find that if the implantation time is 15 minutes, the effective carbon dose could achieve 1.52×10^{18}cm^{-2} and most of the implanted carbons are located in the top 50 nm from the surface of the substrate. When the implantation time decreases to 5 minutes, the effective carbon dose is 2.515×10^{16}cm^{-2} and the implanted carbons are mostly located at the region which is near the surface. Fig.1-8 is the TEM result of 3K5M

CPIII sample, we can see that there is a 32nm thick amorphous layer on the surface of silicon substrate.

Since too many carbon implanted into silicon will deactivate other dopants and increase the interface contact resistance [15]. The suitable carbon dose in the silicon substrate should be between 1×10^{15} cm^{-2} and 1×10^{16} cm^{-2}. Base on all the experimental data, the carbon implantation time will be controlled less than 5 minutes in the following experiments, which is expected to produce better experimental results.

1.4 Impact of CPIII on NiSi/Si Structure

In this section, thermal stability of the NiSi/Si structure after performing carbon PIII process is examined. First, the thermal stability of the pure NiSi/Si structure is discussed and used as reference, then the thermal stability of the carbon PIII NiSi/Si structure is discussed. Both NiSi/Si structure with N$^+$ doping and without N$^+$ doing are included.

A. Pure NiSi/Si Structure

From the sheet resistance value of the samples shown in Fig.1-9, the resistance value of NiSi is very stable when the annealing temperature is lower than 700°C. This indicates that agglomeration and phase transformation do not occur when the annealing temperature is not higher than 700°C. From the SEM images in Fig.1-10(a) ~Fig.1-10(c), it is also found that the surface of the sample is smooth when the annealing temperature is not higher than 700°C. This indicates that agglomeration does not occur. As the annealing temperature increases to 800°C, the sheet resistance increases obviously. This result indicates that agglomeration and/or phase transformation occurs. From the SEM image shown in Fig.3-10(d), it is observed that the nickel silicide surface agglomerates and some holes appear. From the XRD spectra shown in Fig.3-11, it is observed that the phase of nickel silicide transforms from NiSi to NiSi$_2$ when the annealing temperature increases to 900°C. Fig.3-10(e) shows that the agglomeration is very sever, there is no continuous nickel silicide film on the surface.

In summary, pure NiSi can form stable nickel silicide thin film when the annealing temperature is not higher than 700°C. Agglomeration and phase transformation occur at temperatures higher than 800°C.

B. CPIII NiSi/Si Structure without Arsenic Doping

Fig.1-12 shows the sheet resistance values of the 3K1M and 5K1M CPIII samples after

annealing at various temperatures. It is surprised that the sheet resistance values of the 3K1M CPIII samples are all higher than 160Ω/□ in the whole annealing temperature range from 500°C to 900°C. On the contrary, the 5K1M samples exhibits better thermal stability than the reference samples shown in the previous sub-section, i.e. the non-carbon implanted samples.

Fig.1-13 shows the XRD spectra of the 3K1M samples. There is no nickel silicide formed in the temperature range from 500°C to 700°C. As temperature increased to 800°C and 900°C, evident peaks with respect to $NiSi_2$ phase are observed. But, in Fig.1-14, SEM inspection observed that when the annealing temperature increases to 800℃ and 900℃, the surface agglomerates severely. Since the $NiSi_2$ is totally not continuous, the sheet resistance value is very high.

Fig.1-15 shows the surface morphology of the 5K1M CPIII samples inspected by SEM. Even when the annealing temperature increases to 800°C, the surface agglomeration is very slight. Only a few pin holes occur on the surface and the nickel silicide film is continuous. The XRD spectra of the 5K1M samples are shown in Fig.1-16. The $NiSi_2$ phase observed on the 700°C annealed sample indicates that means phase transformation occurs. As annealing temperature increased to 900°C, the sheet resistance increased to a very high value. From the SEM micrograph, we can see the surface agglomeration is very severe which results in the high sheet resistance.

C. CPIII NiSi/Si Structure with Arsenic Doping

The effect of As doping on the thermal stability of the CPIII NiSi/Si structure is evaluated. After CPIII, all samples accepted additional As^+ ion implantation at 30keV to a dose of 5×10^{15} cm^{-2}. Sheet resistance measurement、XRD and SEM were done to analysis the thermal stability.

Fig.1-17 shows the sheet resistance results of the 3K1M, 3K5M, 5K1M, and 5K5M CPIII samples. It is found that the 3K1M CPIII sample has stably low sheet resistance around 12Ω/□ to 15Ω/□ when the annealing temperature is in the range of 500°C to 700°C. As the annealing temperature increases to 800℃, the sheet resistance increased to 124 Ω/□. This means that agglomeration occurs. When the annealing temperature further increases to 900°C, the sheet resistance is 92.08Ω/□, which is lower than the value of the 800°C annealed sample. The cause of this phenomenon may be explained as followed. The nickel silicide phase transformation speed is slower when annealing temperature is 800°C, the nickel silicide film

partly agglomerates before phase transformation, so the sheet resistance is high. When the annealing temperature increases to 900°C, the phase transformation speed is higher. NiSi phase can transform to $NiSi_2$ phase before severe agglomeration occurs, so the extent of agglomeration is slighter than that on the 800℃ annealed sample, and the sheet resistance is lower. The SEM micrographs shown in Fig.1-18 proofs the agglomeration on the 800°C annealed sample is more severe than that on the 900°C annealed sample. This observation confirms previous hypothesis.

The sheet resistance results of the 5K1M CPIII sample are similar to the results of the 3K1M CPIII sample. That means the agglomeration and phase transform on the samples are similar. The surface morphology of the 3K1M and 5K1M CPIII samples inspected by SEM are shown in Fig.1-18 and Fig.1-19, respectively. It is observed that both 3K1M and 5K1M samples has very smooth surface without agglomeration when the annealing temperature is 500°C and 600°C. This observation matches with the sheet resistance results. As the annealing temperature increases to 700°C, both 3K1M and 5K1M samples reveal pin holes on part of the surface. Since most part of the surface is still continuous, the sheet resistance does not change significantly. From the SEM micrographs shown in Fig.1-18 and Fig.1-19, the surface morphologies of the 3K1M and 5K1M samples are very similar at every annealing temperatures, this result is consistent with the sheet resistance result.

The sheet resistance values of the 3K5M and 5K5M PIII samples are very different from the 1 minute CPIII samples. When the annealing temperature is 500℃ and 600℃, the sheet resistance values of both 3K5M and 5K5M samples are between 160 Ω/□ and 200 Ω/□. The surface morphologies of both samples are shown in Fig.1-20 and Fig.1-21. It is observed that the surface of both samples were smooth, which implies that the high sheet resistance value is not due to agglomeration. The XRD analysis reveals that there's no nickel silicide formed on sample surface when the annealing temperature is 500°C and 600°C, as shown in Fig.1-22. As the annealing temperature increases to 700°C, $NiSi_2$ forms so the sheet resistance decreases. However, the SEM images shown in Fig.1-20 and Fig.1-21 show that the silicide film significantly agglomerates when the annealing temperature increases to 700°C, so the sheet resistance is still around 130Ω/□. In the 800°C annealing case, the agglomeration is severer, so the sheet resistance further increases. When the annealing temperature increases to 900°C, because the phase transform speed increases as mentioned before, the agglomeration is slighter than the 800℃ annealed sample, so the sheet resistance is lower.

The experimental results of the CPIII NiSi/Si structure are summarized as follows. In the

CPIII process, CH$_4$ plasma was used as implantation source. The CH$_4$ plasma contains some low energy (< 100eV) radicals, those radicals deposited on the surface and formed a carbon thin film. This carbon film will affect the forming of nickel silicide. In addition, the DC pulse signal was not a perfect square wave. In the rise time and fall time regions, the voltage changed with time and created some low energy ions. If the energy of ions is lower than 100eV, the ions might pile up on the surface and form a carbon film [16]. In the TEM micrograph shown in Fig.1-8, no carbon film is seen clearly because the carbon atom density on the surface is near the silicon atom density as the SIMS result shows (Fig.1-6 and Fig.1-7). The contrast between silicon substrate and carbon film is very close, so the carbon film could not be clearly identified. On the samples without arsenic doping, when the annealing temperature is between 500℃ to 700℃, nickel silicide couldn't form on the 3K1M CPIII sample because of the existence of the carbon film. Until the annealing temperature increased to 800°C, the nickel silicide could form. The 5K1M CPIII samples have thinner carbon film on the surface because the carbon implantation energy was higher, and the nickel silicide formation was not affected. On the samples with arsenic doping, since the 3K1M and 5K1M CPIII samples has thinner carbon film, the high energy arsenic doping could remove or destroy the surface carbon film. In this case, NiSi could form on the surface when the annealing temperature is as low as 500°C. The 3K5M and 5K5M CPIII samples have thicker carbon film because the process time is longer. For that reason, arsenic doping could not remove all the carbon film and the nickel silicide could not form on the surface when the annealing temperature is between 500°C and 600°C. However, arsenic doping still reduce the carbon film thickness, and NiSi$_2$ could form when the annealing temperature is 700°C.

It is also observed that the thermal stability of the CPIII NiSi/Si structure is better than that of the pure NiSi/Si structure. The agglomeration temperature increased to 800°C and the phase transform temperature is between 700°C and 800°C. However, after arsenic doping, the thermal stability of the CPIII NiSi degrades. The agglomeration temperature reduces to 700°C and the phase transform temperature is lower than 800°C. The cause of this effect is the doped arsenic. Since arsenic atom is bigger than silicon, after implanted into silicon substrate, arsenic will change the interfacial energy between nickel silicide and silicon. High energy implanted arsenic will also interact with silicon and nickel in the nickel silicide, the nickel will diffuse to the substrate and the silicon may form SiO$_2$ with the residual oxygen in the annealing environment. All the effects will lower the nickel silicide thermal stability [17].

1.5 Conclusions

Carbon plasma immersion ion implantation can implant large amount of carbon into silicon substrate in a short time. The SIMS depth profile indicates that the effective dose after 15minutes CPIII process can achieve 1.52×10^{18} cm^{-2} and most of the implanted carbons are located in the top 50 nm from the surface of the substrate. From the TEM image we can find there's no evident amorphous layer on the surface. We perform CPIII on N$^+$P junction structure at energy 3keV、5keV for 1minute、5minutes, and we find the CPIII process would not increase junction leakage because implanted carbon can repair the secondary defects caused by ion implantation by capturing Si interstitials, and further reduce the leakage current brought by secondary defects. As CPIII applied to NiSi/Si structure without arsenic doping, we find 5K1M CPIII process can improve the agglomeration temperature to 800℃. In the case of arsenic doped NiSi/Si structure, we find CPIII could not increase NiSi thermal stability because arsenic atom will change the interfacial energy between nickel silicide and silicon.

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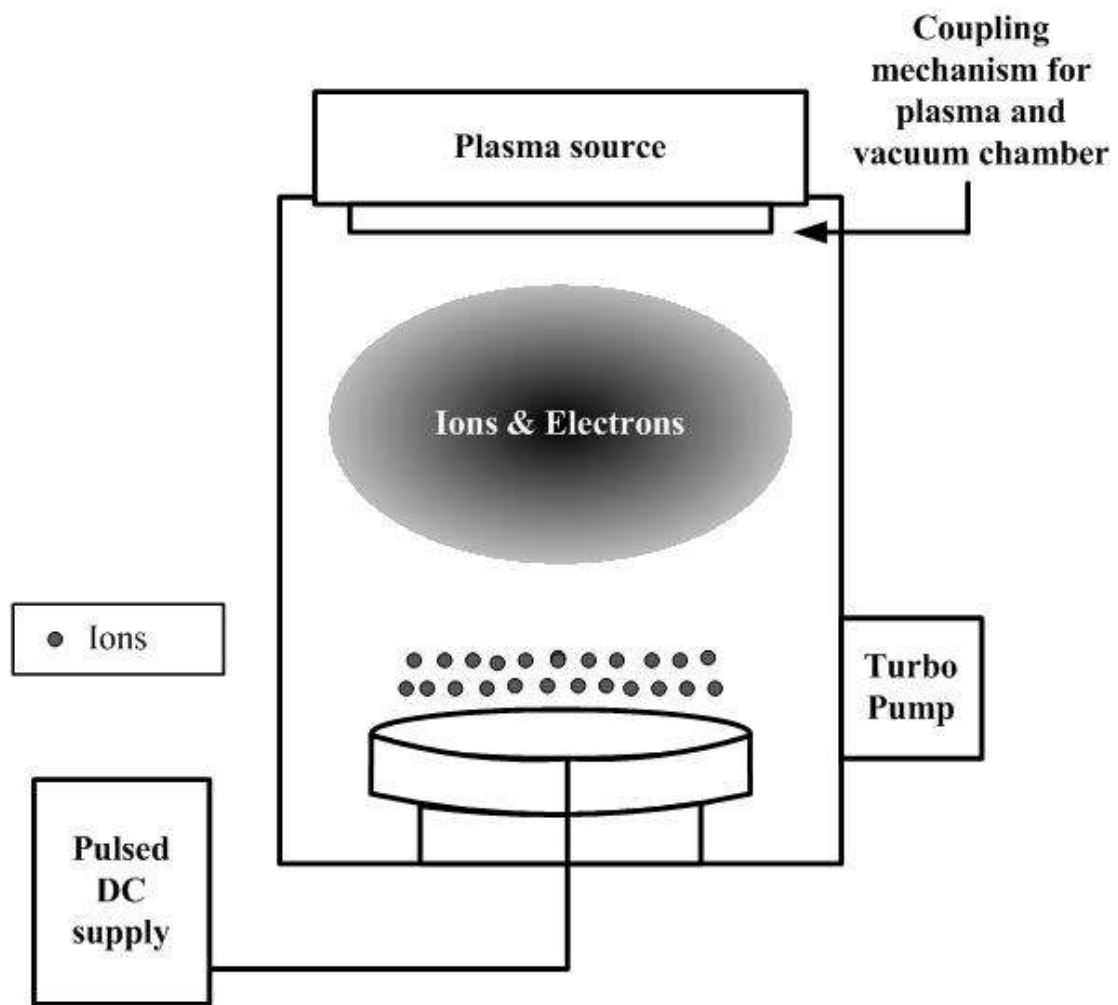
Fig.1-1.   The schematic diagram of PIII system.

Fig.1-2.   The process environment and equipment of PIII.
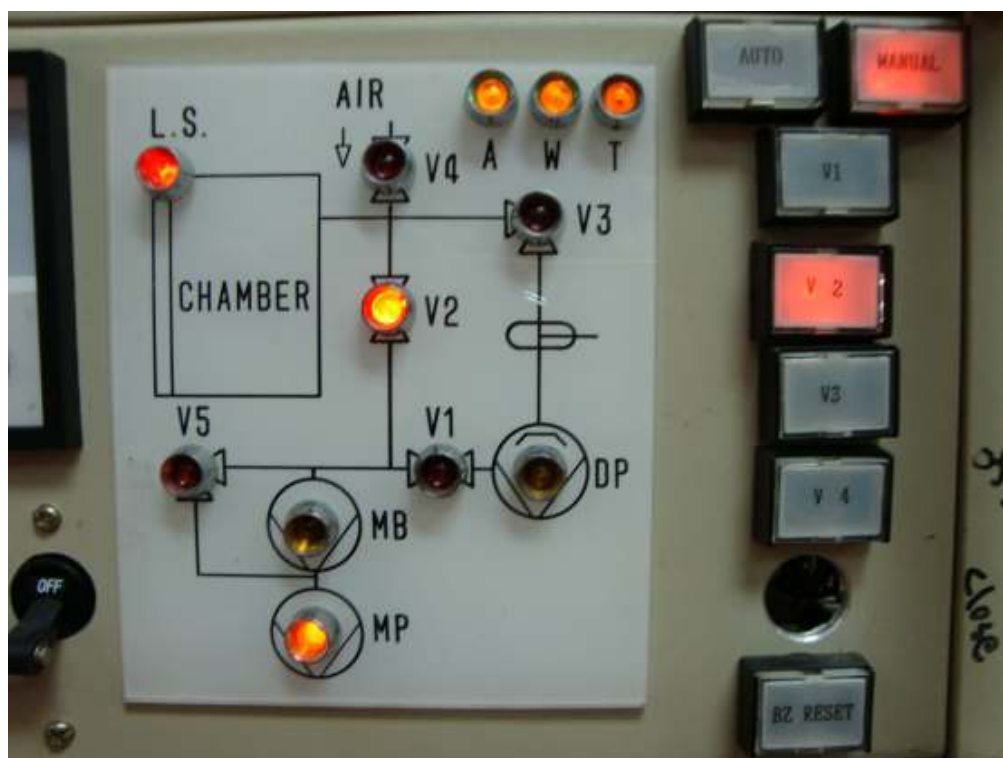
Fig.1-3.   The control panel of process chamber valves

Fig.1-4.　The DC power supply of electrical power system

Fig.1-5.　The DC high voltage power supply of electrical power system
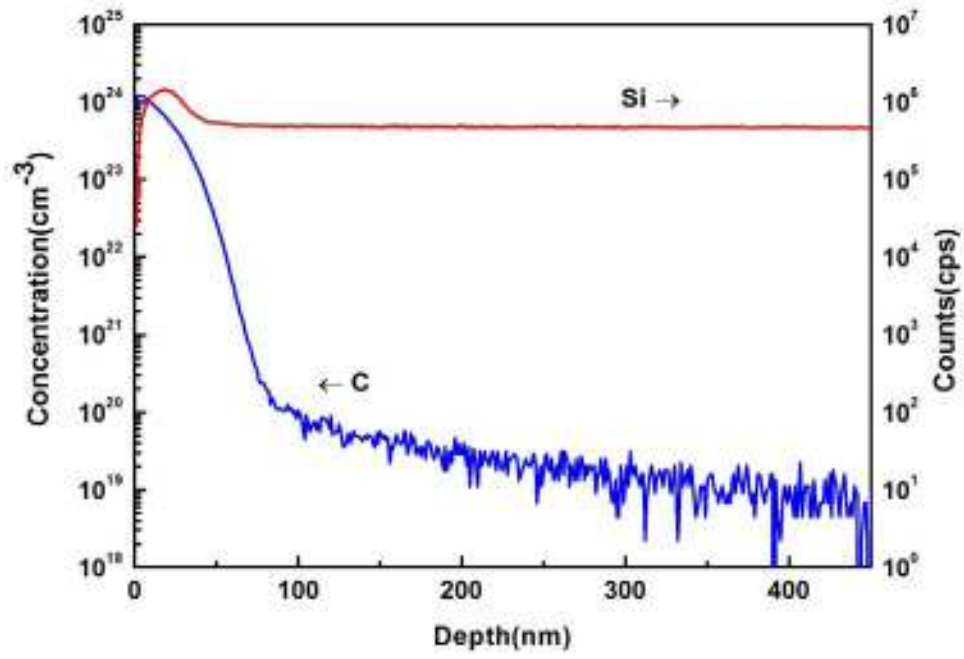
Fig.1-6.   SIMS depth profile after CPIII process (10keV/15min)
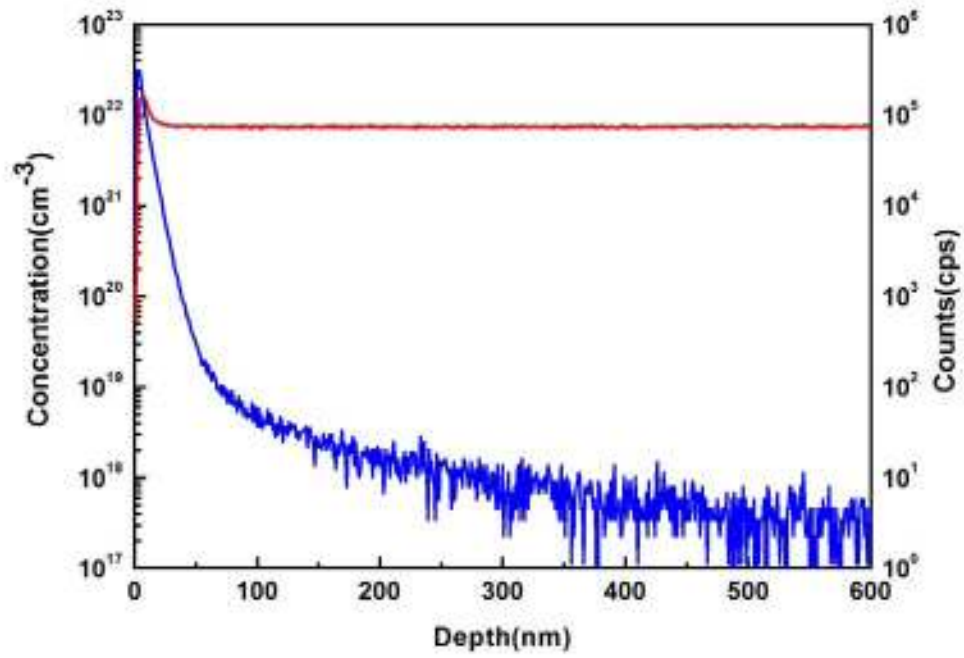
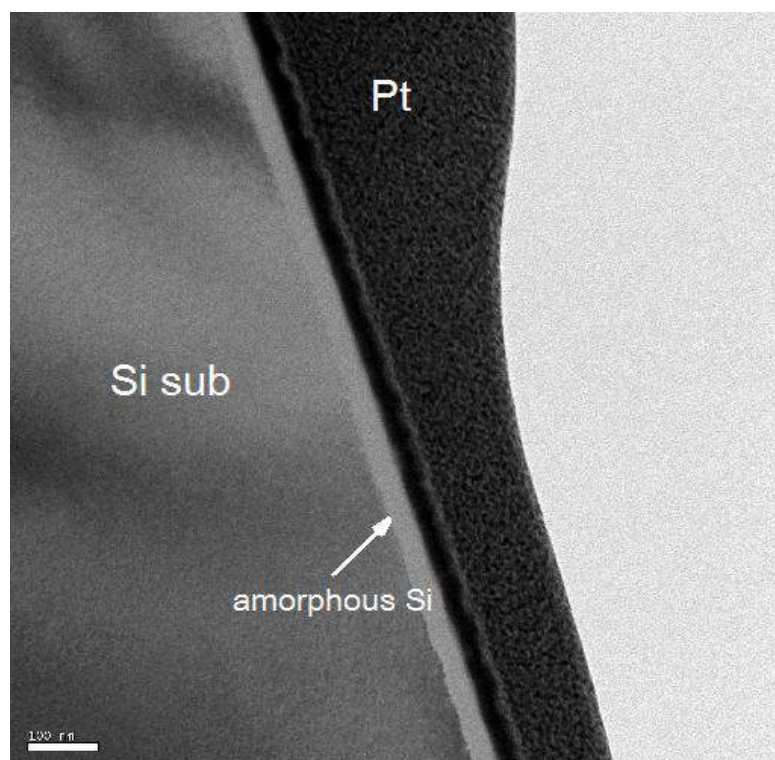Fig.1-7.   SIMS depth profile after CPIII process (3keV/5min)
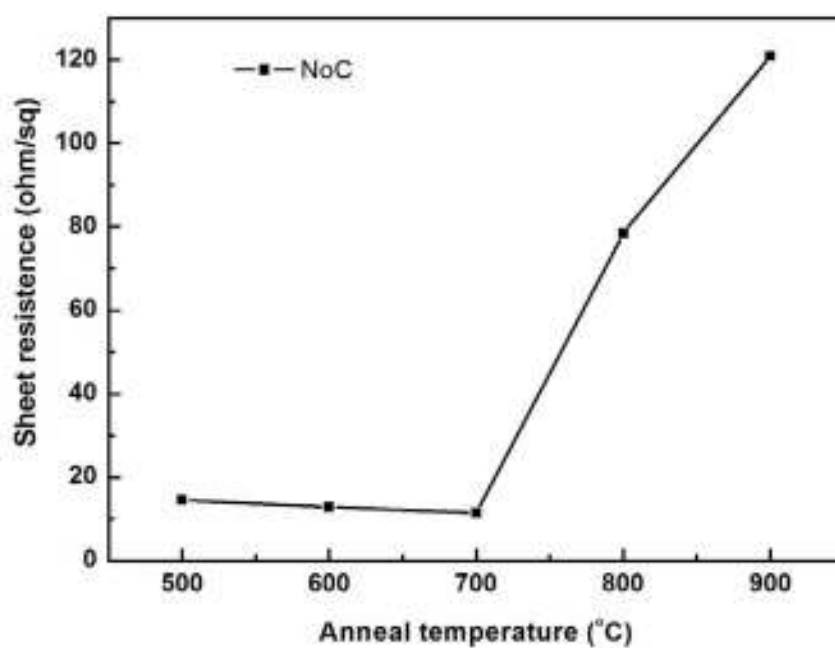
Fig.1-8.　The TEM image of 3keV/5min CPIII sample

Fig.1-9.　The sheet resistance value of pure NiSi sample with annealing temperature 500℃
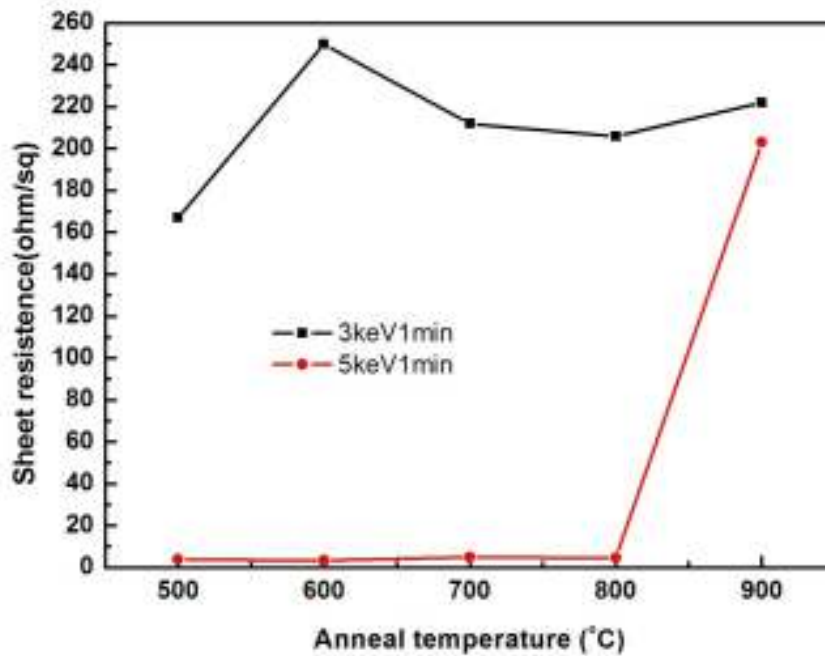　　　　　to 900℃, annealing time 30secs.

(a) 500℃   NDL   SEI   15.0kV   X10,000   1μm   WD 10.1mm

(b) 600℃   NDL   SEI   15.0kV   X10,000   1μm   WD 10.1mm

(c) 700℃   NDL   SEI   15.0kV   X10,000   1μm   WD 10.0mm

(d) 800℃   NDL   SEI   15.0kV   X10,000   1μm   WD 10.0mm

(e) 900℃   NDL   SEI   15.0kV   X10,000   1μm   WD 10.0mm
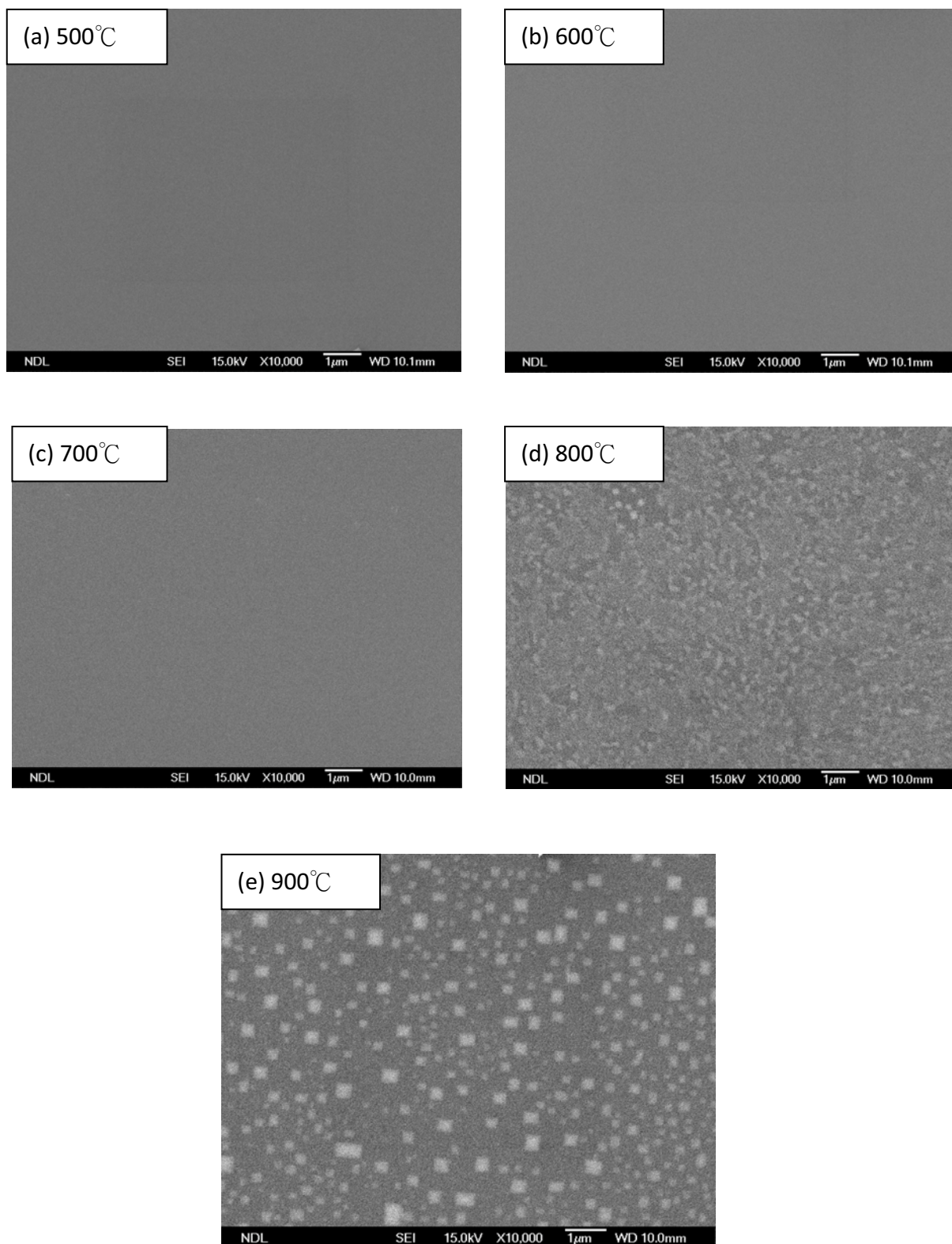
Fig.1-10.   The SEM images of pure NiSi sample with annealing temperature 500℃ to 900℃, annealing time 30secs.
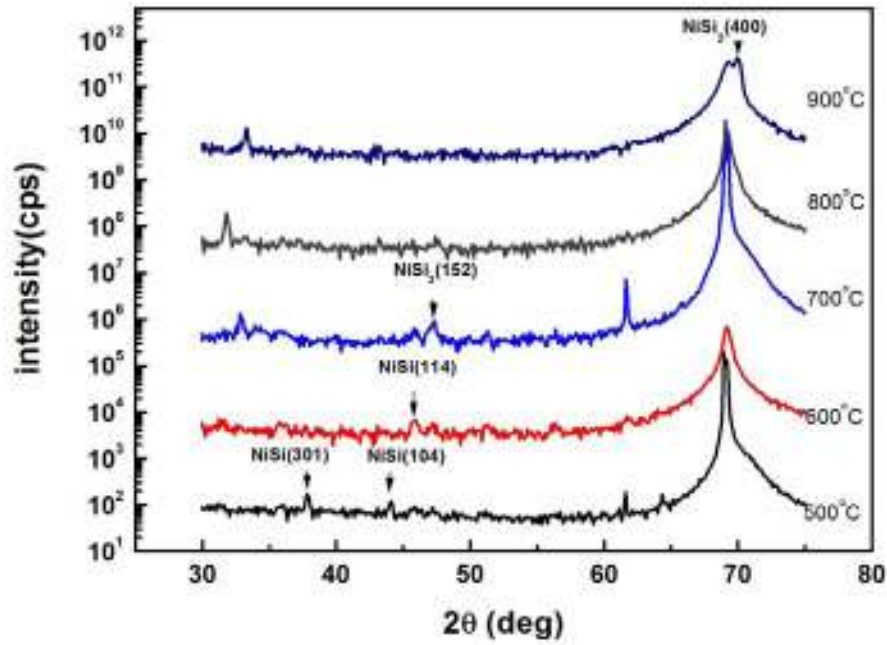
Fig.1-11. The XRD patterns of pure NiSi sample with annealing temperature 500℃ to 900℃, annealing time 30secs.

Fig.1-12. The sheet resistance value of 3keV1min and 5keV1min CPIII samples with annealing temperature 500℃ to 900℃, annealing time 30secs. (No As)
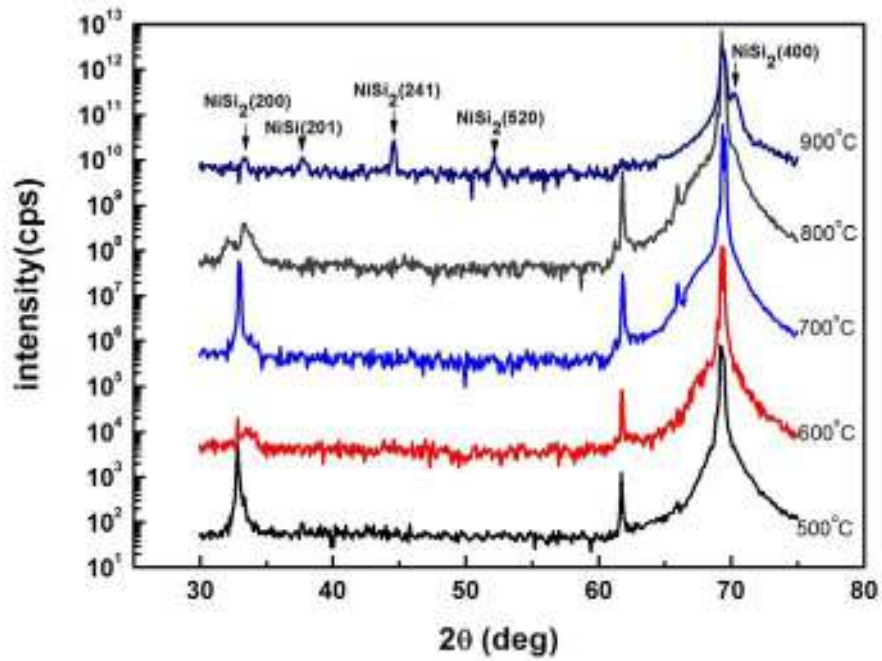
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Fig.1-13. The XRD patterns of 3keV1min CPIII NiSi samples with annealing temperature 500℃ to 900℃, annealing time 30secs. (No As)
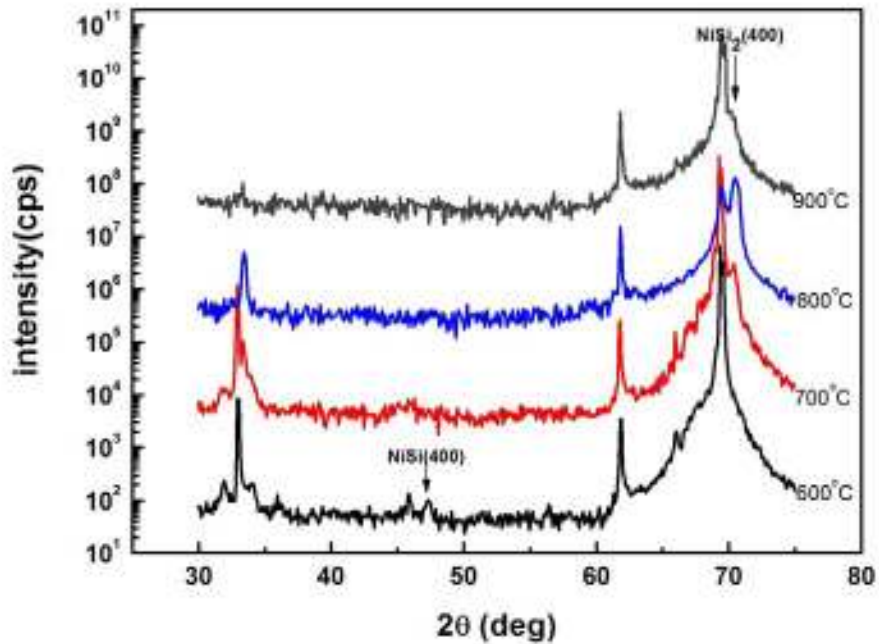

Fig.1-14. The XRD patterns of 5keV1min CPIII NiSi samples with annealing temperature 500℃ to 900℃, annealing time 30secs. (No As)
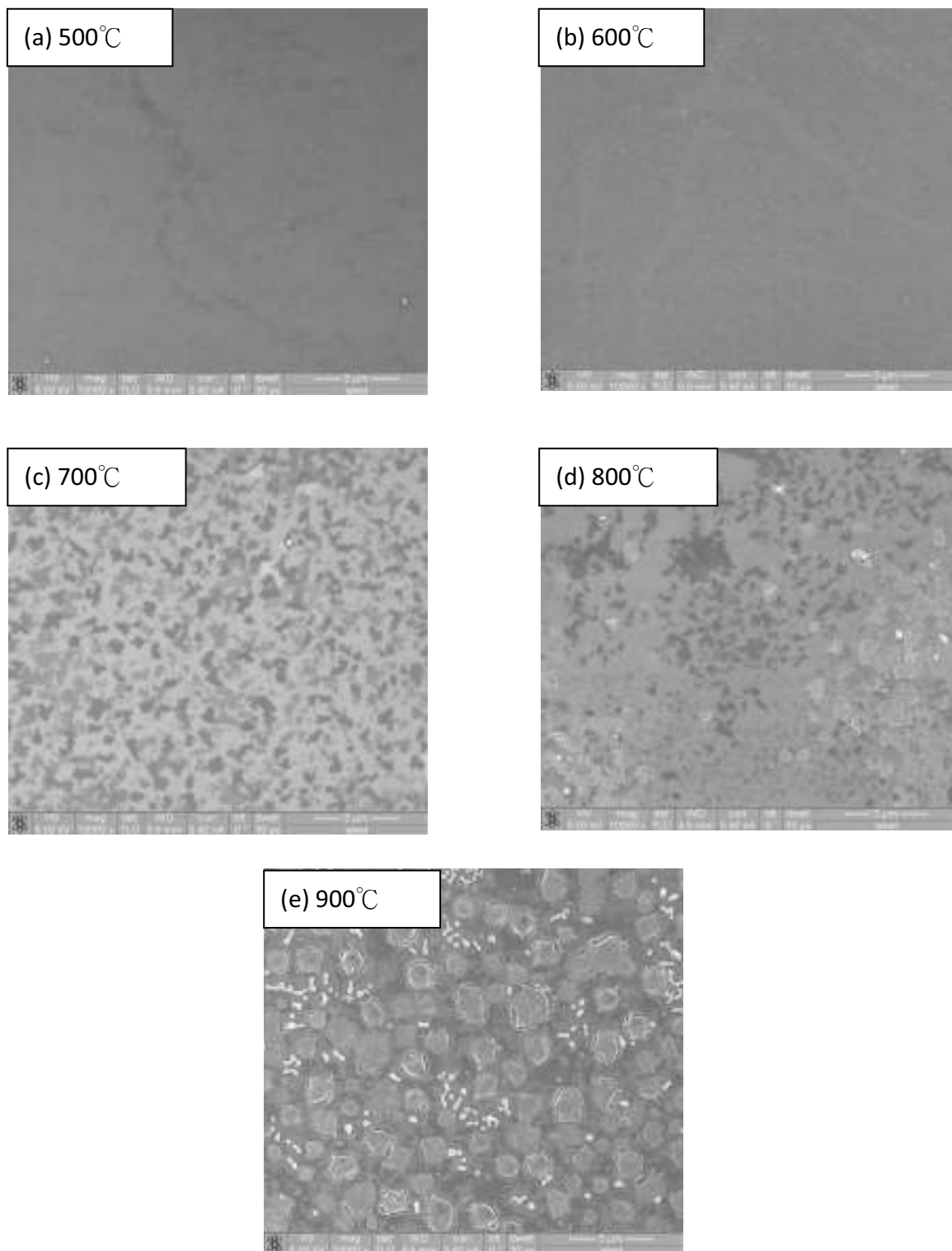
(a) 500℃

(b) 600℃

(c) 700℃

(d) 800℃

(e) 900℃

Fig.1-15. The SEM images of 3keV1min CPIII NiSi samples with annealing temperature 500℃ to 900℃, annealing time 30secs. (No As)
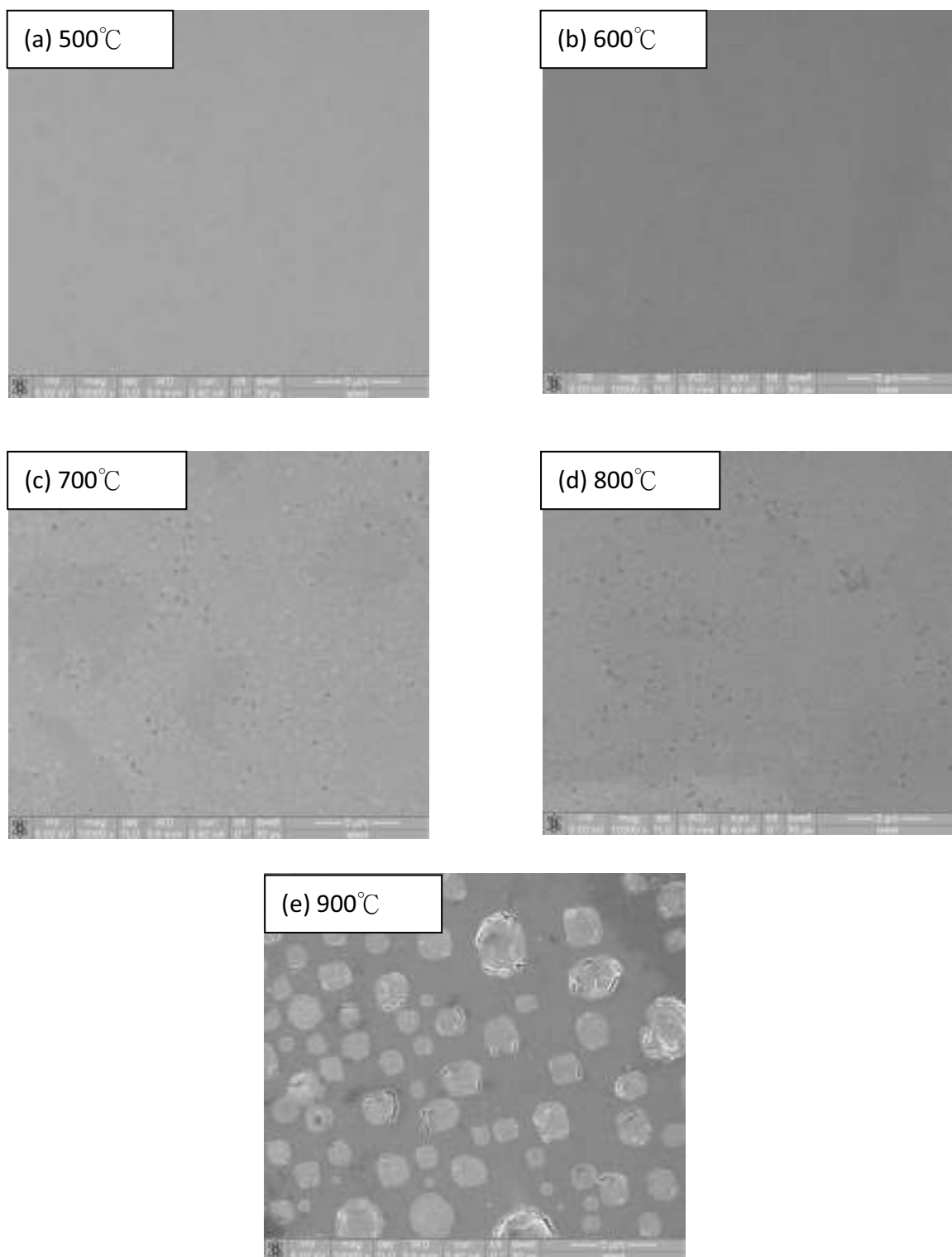
Fig.1-16. The SEM images of 3keV1min CPIII NiSi samples with annealing temperature 500℃ to 900℃, annealing time 30secs. (No As)
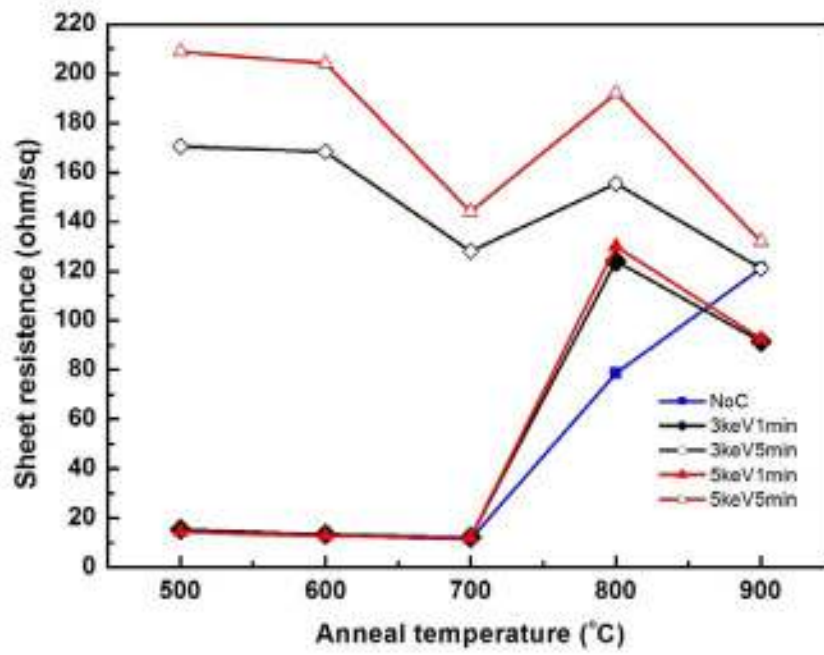
Fig.1-17. The sheet resistance value of implant energy 3keV and 5keV implant time 1min and 5mins CPIII and pure NiSi samples with annealing temperature 500℃ to 900℃, annealing time 30secs. (with As)
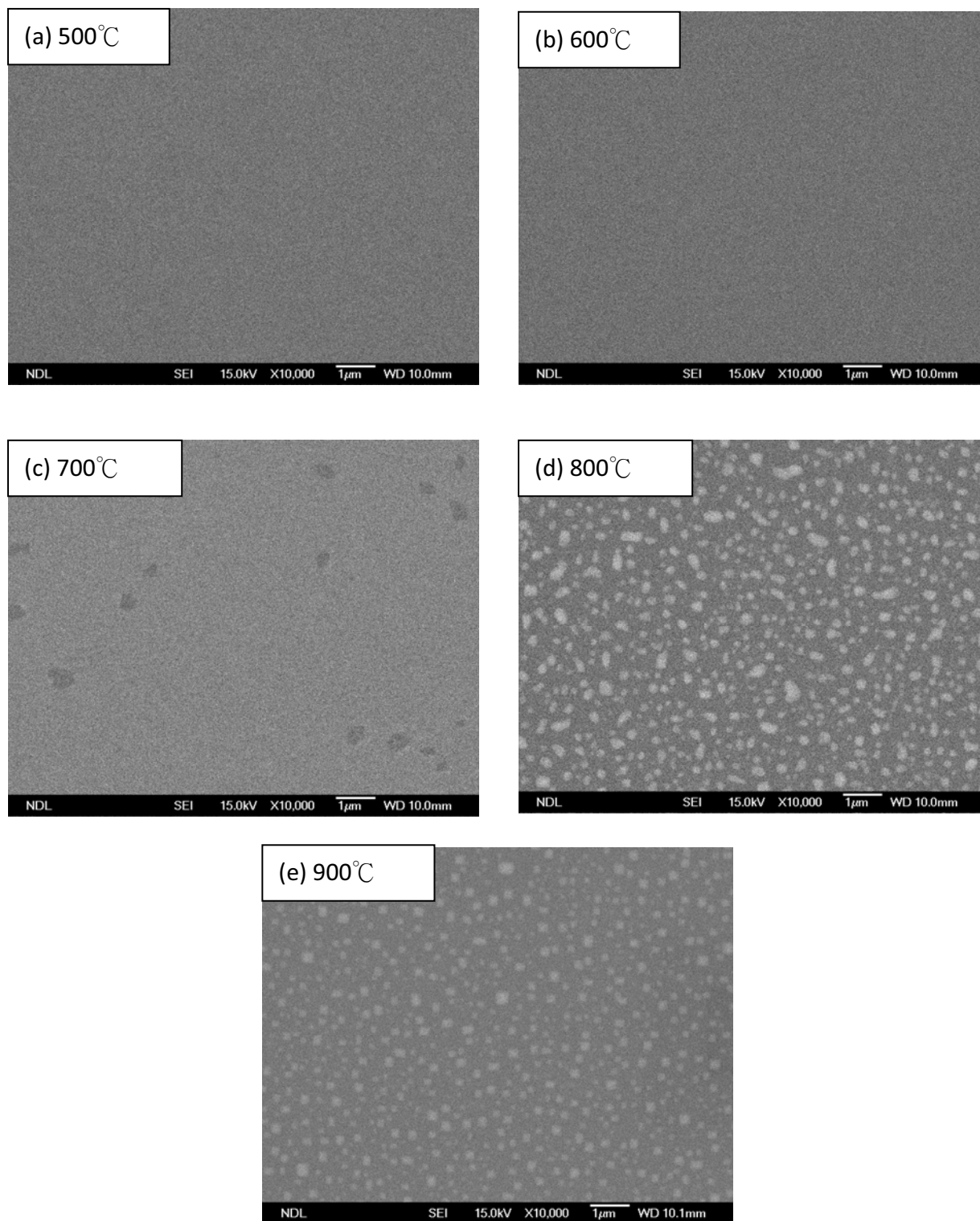
Fig.1-18. The SEM images of 3keV1min CPIII NiSi samples with annealing temperature 500℃ to 900℃, annealing time 30secs. (With As)
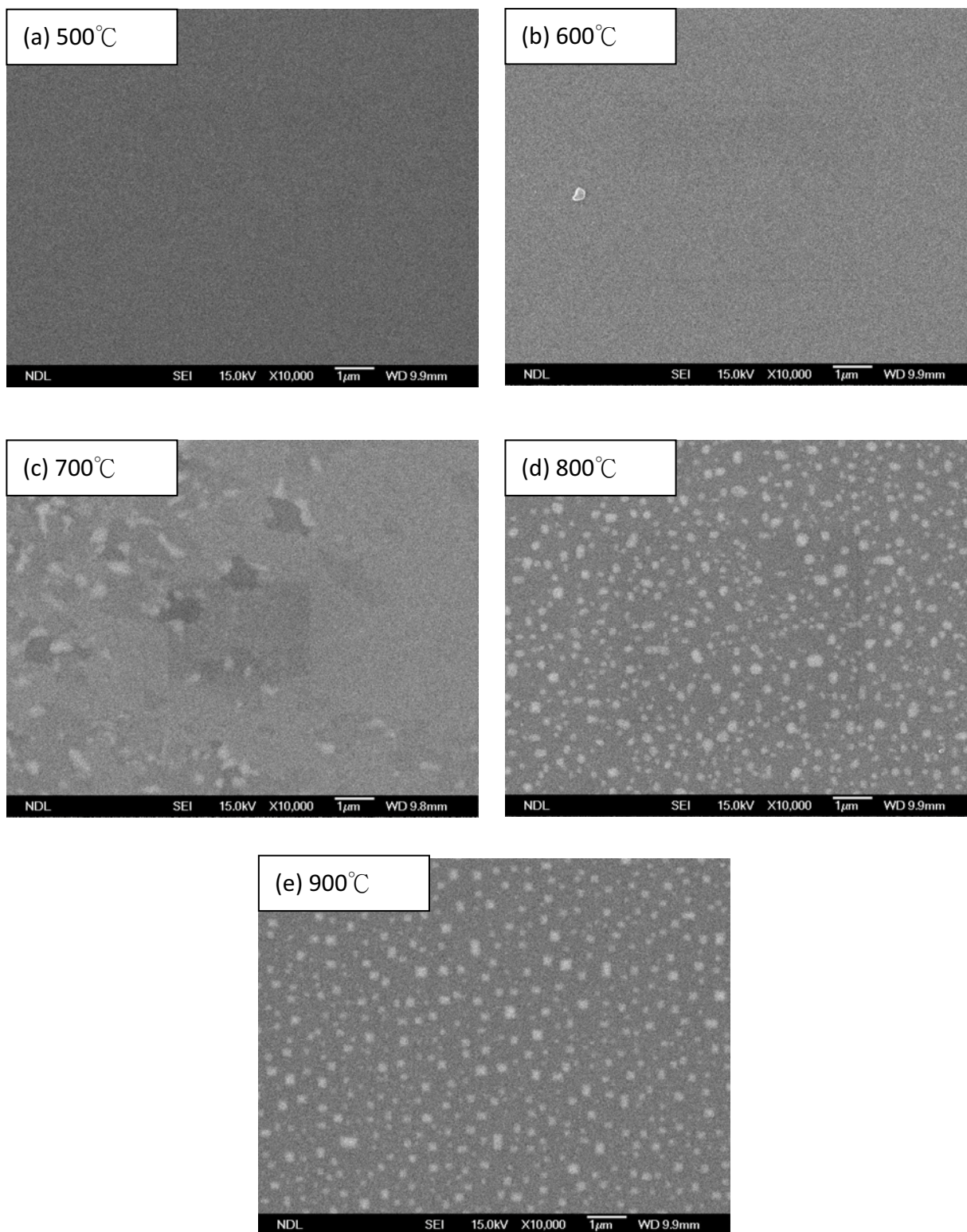
Fig.1-19. The SEM images of 5keV1min CPIII NiSi samples with annealing temperature 500℃ to 900℃, annealing time 30secs. (With As)
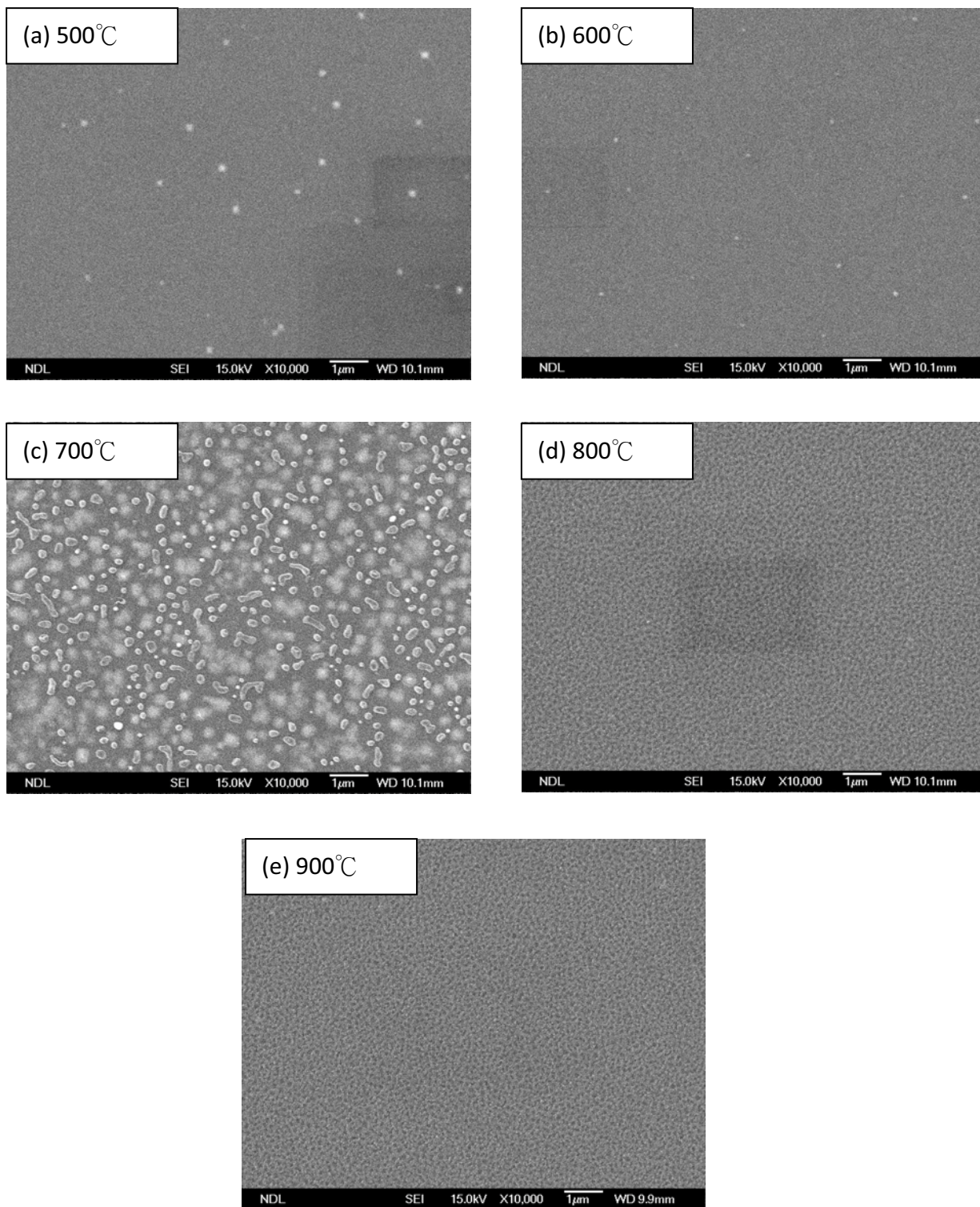
Fig.1-20. The SEM images of 3keV5min CPIII NiSi samples with annealing temperature 500℃ to 900℃, annealing time 30secs. (With As)
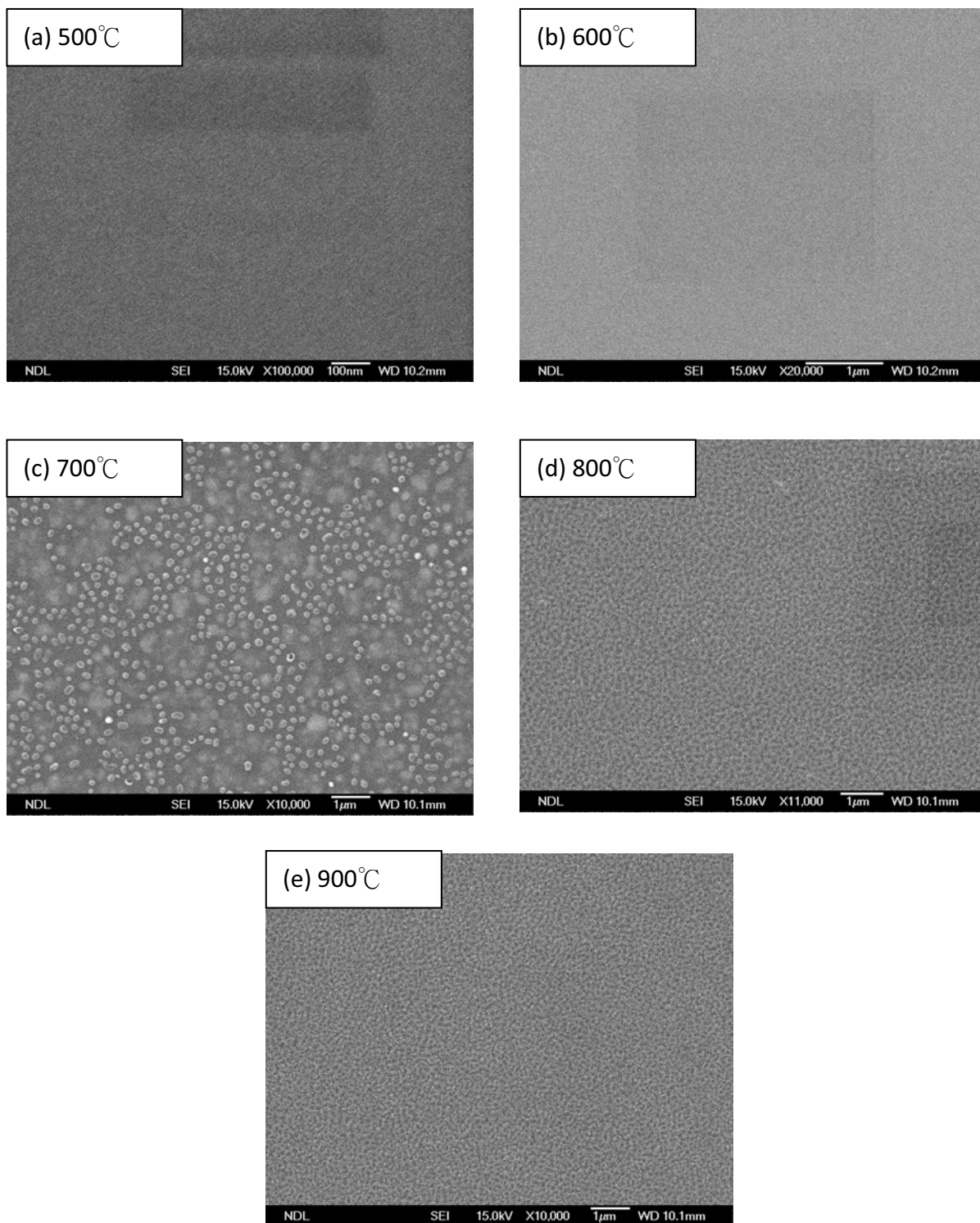
Fig.1-21. The SEM images of 5keV5min CPIII NiSi samples with annealing temperature 500℃ to 900℃, annealing time 30secs. (With As)
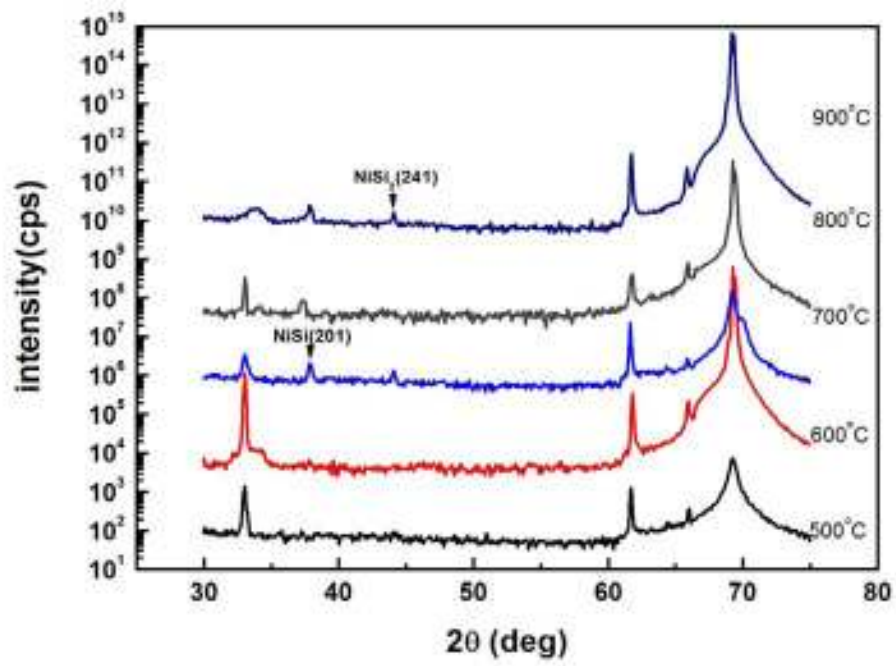
Fig.1-22. The XRD patterns of 5keV5min CPIII NiSi samples with annealing temperature 500℃ to 900℃, annealing time 30secs. (With As)

Chapter 2

Effect of Carbon Ion Implantation on the Thermal Stability of Nickel Silicide Film

2.1 Introduction

NiSi has been used as source/drain (S/D) contact material of sub-100 nm MOSFETs technology because of its several advantages including low resistivity, low contact resistivity, low temperature process, less Si consumption during silicide formation, and no narrow line effect and bridging failure [1]. For further scale-down, one of the main issues of NiSi is its poor thermal stability. It has been known that NiSi film agglomerates at 700 °C and transforms into $NiSi_2$ at 750 °C. These factors result in an increasing sheet resistance of nickel silicide and poor morphology, and then degrade device performance. Consequently, raising the thermal stability of NiSi is very important. Many different solutions have been proposed by several authors to improve the thermal stability of nickel silicide. These solutions involve the ion implantation utilizing F or N_2 ions before NiSi formation, Ti or Pt deposition as a capping layer or a interposing layer, and $Ni_{1-x}Ti_x$ or $Ni_{1-x}Pt_x$ alloy [2-7].

Recently, S. Zaima et al. reported that Ni film on p^+ $Si_{0.996}C_{0.004}$ epitaxial layer grown by low-pressure chemical vapor deposition (LPCVD) can suppress NiSi agglomeration effectively after annealing at 750 °C and retard its phase transformation until the annealing at 850 °C [8]. This result indicates that adding carbon (C) atoms in Si substrate is a feasible method to enhance the thermal stability of NiSi. Since the solid solubility of carbon in Si and NiSi is very low [9], carbon atoms segregate to the NiSi grain boundary and NiSi/Si interfaces and modify grain boundary and interfacial energy to suppress agglomeration and phase transformation [10]. However, when adopting selectively embedded S/D process of MOSFETs in order to produce strained Si channel, it is difficult to grow $Si_{1-x}C_x$ with substitutional C concentration exceeding 1 % (x>1 %) due to extremely low solid solubility of C in Si.

In this chapter we introduce the ion implantation method with C ions into Si substrate so that high substitutional C concentration can be achieved, and this process is an easier than epitaxy process and can be integrated with conventional CMOS process flow. The correlation between the C dose of the ion implantation and the NiSi thermal stability is also discussed.

2.2 Experiments

The starting material was phosphorus-doped (100) 6-in Si prime wafer with a resistivity of 2~7 Ω-cm. A 70-nm-thick screen SiO_2 was thermally grown. Then C ions were implanted into Si substrate through screen oxide with a dose range of $1x10^{15}$, $5x10^{15}$ cm^{-2} to study the influence of C concentration on nickel silicide thermal stability. The ion energy is 30 and 40 keV. A sample without C^+ implantation is also prepared as reference. The C^+ implanted samples are named CIA samples. After C^+ implantation, some samples were annealed in a rapid thermal annealing (RTA) system in N_2 ambient at 1050 °C for 30 sec to make C atoms in the substitutional site of the Si lattice. These samples are called the CIA samples. The samples without post implantation annealing are called the w/o CIA samples. Samples without C^+ implantation were also prepared as reference.

After etching screen oxide by DHF dip, a 25 nm Ni layer was deposited in a physical vapor deposition (PVD) system. One step RTA process was performed to form nickel silicide at the temperature range of 500~850 °C for 30 sec. Finally, un-reacted Ni was removed by H_2O_2:H_2SO_4 (1:3) mixture to finish sample preparation. Four-point probe technique was performed to measure the sheet resistance (R_s) values of all samples. X-Ray Diffraction (XRD) was adopted to distinguish NiSi phase from $NiSi_2$ phase. The plan-view Scanning Electron Microscope (SEM) was used to inspect whether nickel silicide agglomerates.

2.3 Results and Discussion

Fig.1 shows the measured R_s values of CIA samples and the reference samples as a function of annealing temperature for 30sec. Low energy or high dose C^+ implantation result in slightly higher R_s value. As comparing with the reference sample, it is observed that the R_s values of CIA samples are slightly higher because of C atoms existence in nickel silicide. According to the R_s values measured after Ni film deposition, we found that the CIA samples with C^+ implantation to a dose of $5x10^{15}$ cm^{-2} at 30 keV is deposited with thinner Ni film thickness, so these R_s values after nickel silicide formation are higher than the other samples.

The R_s values of reference samples increases monotonically after 700°C because of serious agglomeration and phase transformation. At the same time, the R_s values of CIA samples with a dose of $1x10^{15}$ cm^{-2} is almost stable until 700 °C and become increase at 800 °C because phase transformation and lightly agglomeration occur simultaneously as shown in Fig.2 and 3, respectively.

As the C^+ implantation dose increases up to 5×10^{15} cm^{-2}, the R_s values are stable without increasing until 850 °C. For the CIA samples with C+ implantation to 5×10^{15} cm^{-2} at 30 keV, the R_s values increase slightly at 850 °C, but for the reference samples, the R_s values increase greatly at 850 °C due to serious agglomeration. Hence the function of carbon atoms within nickel silicide is suppressing agglomeration. For the CIA samples with C^+ implantation to 5×10^{15} cm^{-2} at 40 keV, the R_s values are unchanged even at 850 °C. According to the XRD result as shown in Fig.4, no phase transformation occurs, and the NiSi film is still continuous without agglomerating after 850 °C annealing as shown in the plane-view SEM micrographs of Fig.5.

Fig.6 shows the measured R_s values of w/o CIA samples and the reference sample as a function of annealing temperature for 30sec. For the w/o CIA samples with a dose of 1×10^{15} cm^{-2}, lightly agglomeration and phase transformation (not shown) take place at 800 °C as the same as the CIA samples with the same dose. When C+ implantation dose increases to 5×10^{15} cm^{-2}, as comparing between Fig.1 and Fig.6, the temperature dependence of the R_s value of the w/o CIA samples is more apparent than that of the CIA samples. We speculate that the grain size variation dominates this phenomenon. Because the Si surface was amorphized by the high dose C^+ implantation, the poly-NiSi grain size of the w/o CIA samples is lager and the R_s value is lower with the increase of temperature during nickel silicide formation. For the w/o CIA samples with a dose of 5×10^{15} cm^{-2}, grain growth effect dominates R_s value at the temperature range of 500~800 °C as shown in Fig.6. On the contrary, phase transformation and agglomeration dominate R_s value at 850 °C as shown in Fig.7~8, so that the R_s values increase at 850 °C.

Table 2-1 summarize the phase transforming and agglomerating temperature of all samples. It is clear that carbon ion implantation with a dose of 1×10^{15} cm^{-2} can raise the agglomeration and phase transformation temperature of nickel silicide to 800 °C. Increasing carbon dose to 5×10^{15} cm^{-2}, it is able to further raise the agglomeration and phase transformation temperature of nickel silicide to 850 °C.

2.4 Conclusions

We have investigated the impact of carbon ion implantation on the thermal stability of nickel silicide. Although carbon atoms exist within nickel silicide, may increase the sheet resistance at low silicide-formation temperature ($\leqq$700 °C) due to C segregation at grain boundary, the increased sheet resistance value is only slightly larger than that of the reference

sample without C^+ implantation. For the CIA samples, the increased of sheet resistance value is smaller than 1 $\Omega/\square$. Sufficient carbon atoms, a dose of 5×10^{15} cm^{-2}, can effectively suppress the agglomeration and phase transformation. For the CIA samples with a dose of 5×10^{15} cm^{-2} at 40 keV, agglomeration and phase transformation indeed can be suppressed completely even at 850 °C. Hence as the silicide-formation temperature exceeds 700 °C, samples with C^+ implantation have lower R_s values than the reference samples. The thermal stability of nickel silicide can be improved by as high as 150 °C with the optimum C+ implantation condition of 5×10^{15} cm^{-2} at 40 keV.

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Table 2-1. Table I Summary of results of the agglomeration and phase transformation temperature of all samples.

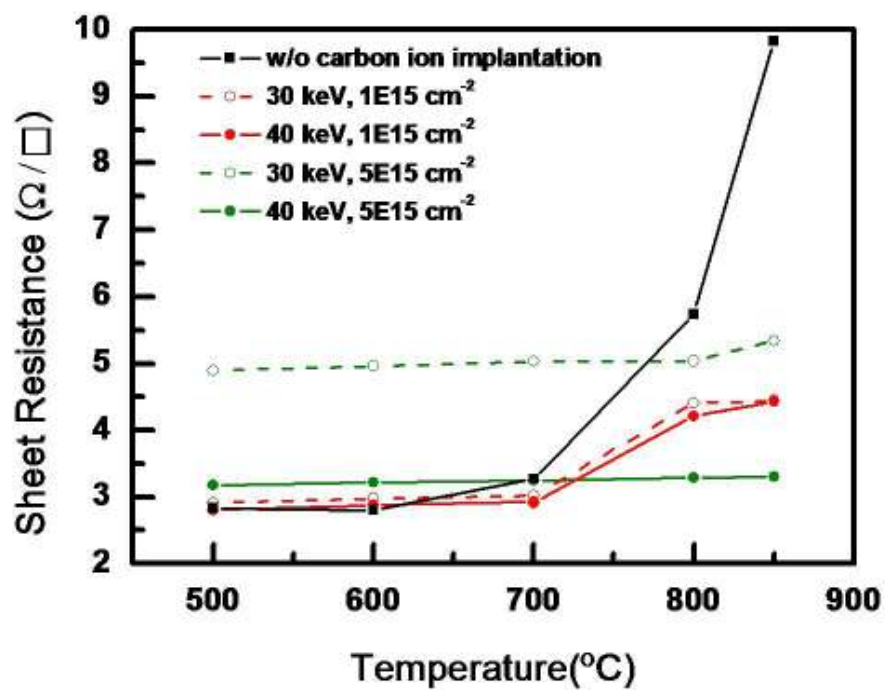| Spilt condition		Agglomeration	Phase transition
30keV, $1x10^{15}$ cm^{-2}	CIA	800 °C	800 °C
	w/o CIA	800 °C	800 °C
40keV, $1x10^{15}$ cm^{-2}	CIA	800 °C	800 °C
	w/o CIA	800 °C	800 °C
30keV, $5x10^{15}$ cm^{-2}	CIA	850 °C	850 °C
	w/o CIA	850 °C	850 °C
40keV, $5x10^{15}$ cm^{-2}	CIA	>850 °C	850 °C
	w/o CIA	850 °C	>850 °C

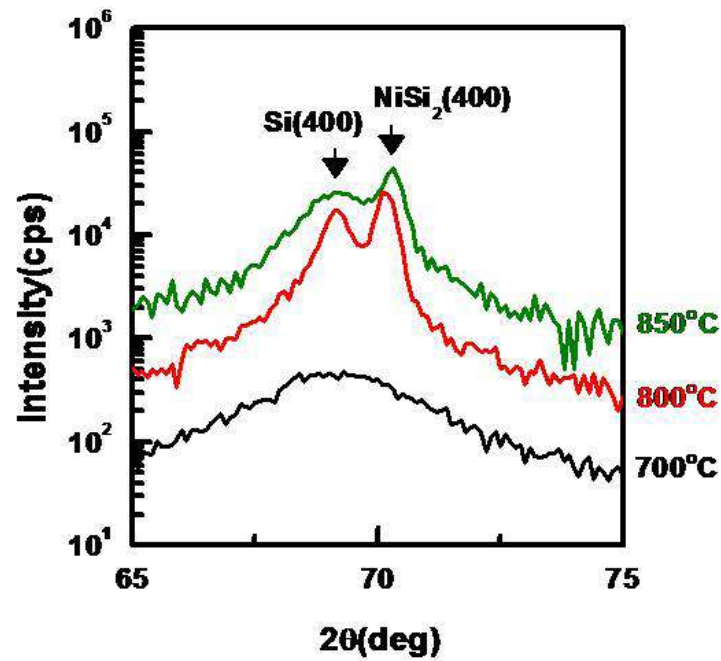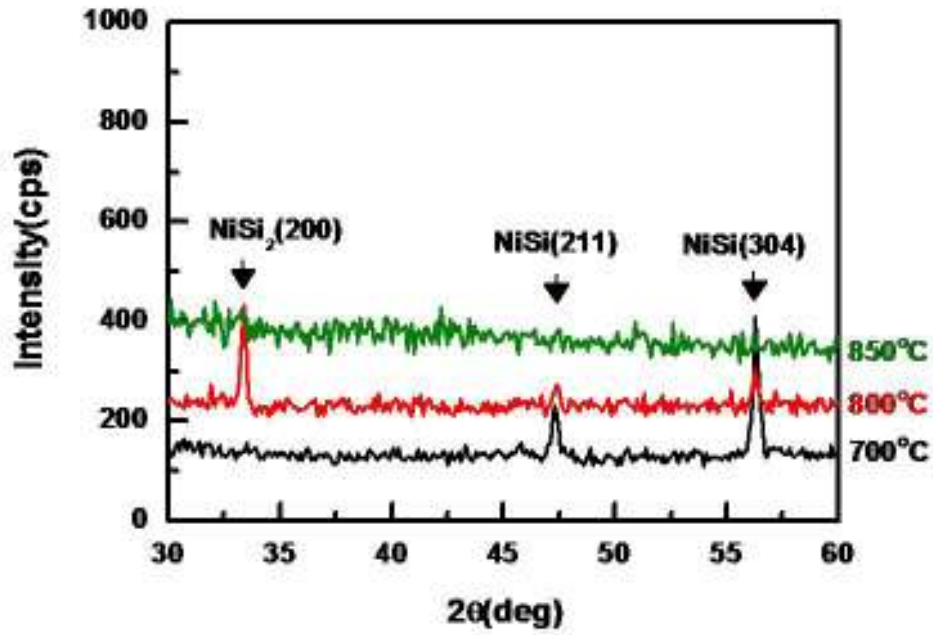Fig.2-1.   Sheet resistance of the CIA samples and the reference samples as a function of annealing temperature.

Fig.2-2.   XRD spectra of the CIA samples with a dose of 1×10^{15} cm^{-2} at 40 keV. Phase transformation occurs at 800 °C and NiSi$_2$ XRD phase can be observed.
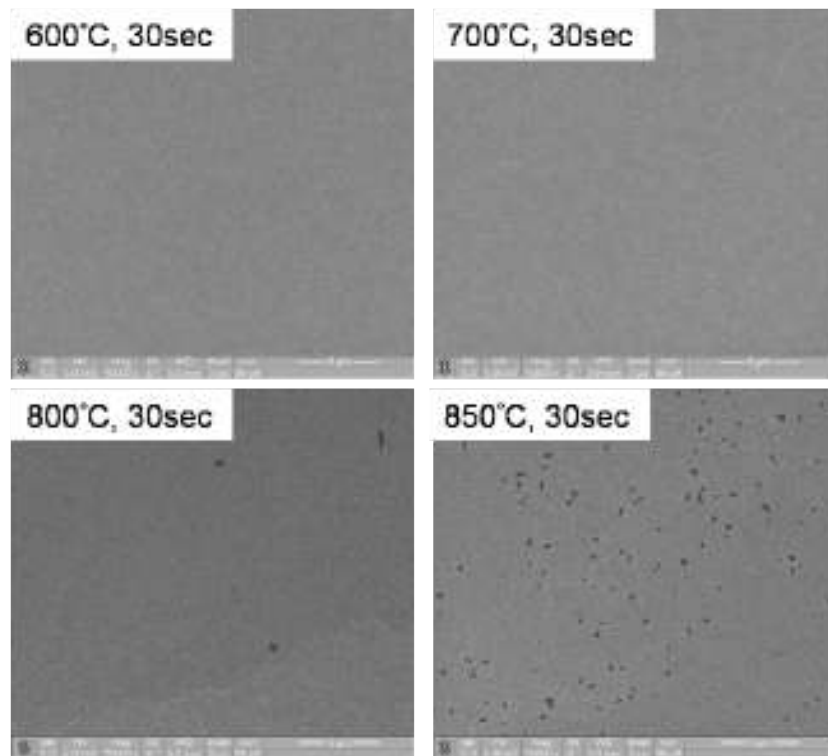
Fig.2-3.　SEM micrographs of the CIA samples with a dose of 1×10^{15} cm^{-2} at 40 keV. Nickel silicide film agglomerates at 800 °C.
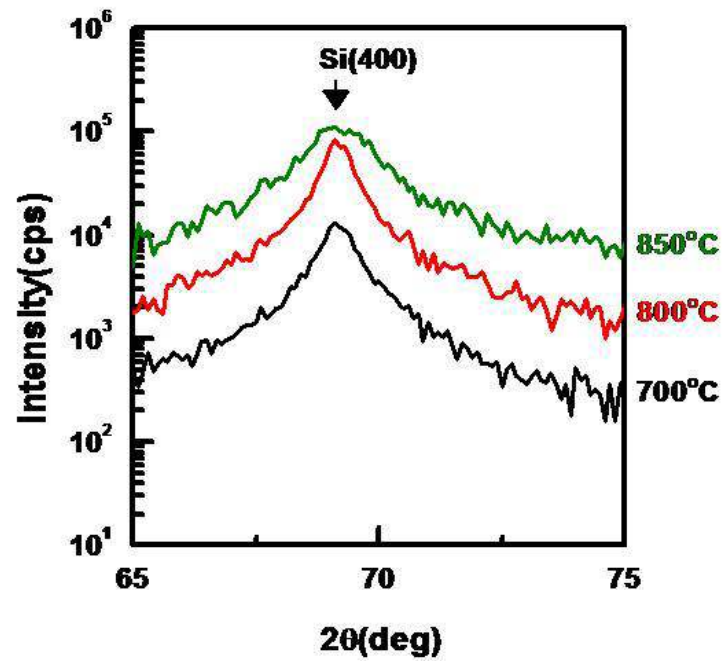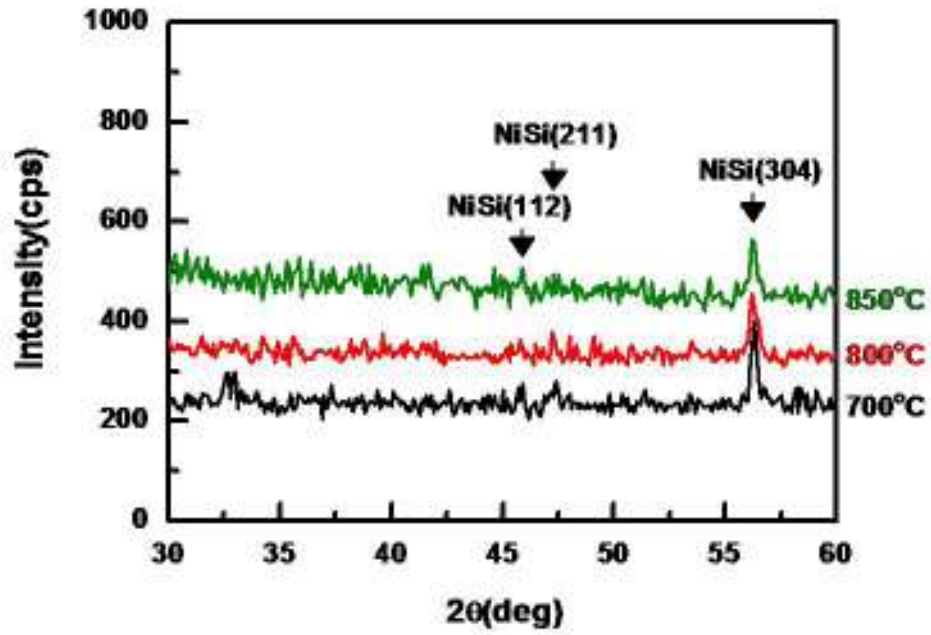
Fig.2-4. XRD spectra of the CIA samples with a dose of 5×10^{15} cm^{-2} at 40 keV. Phase transformation does not occur even at 850 °C.

Fig.2-5. SEM micrographs of the CIA samples with a dose of 5×10^{15} cm^{-2} at 40 keV. No pin-holes can be observed which indicates nickel silicide film is still continuous.

Fig.2-6.   Sheet resistance of the w/o CIA samples and the reference samples as a function of annealing temperature.

Fig.2-7.   XRD spectra of the w/o CIA samples with a dose of 5×10^{15} cm^{-2} at 30 keV. Phase transformation occurs at 850 °C.

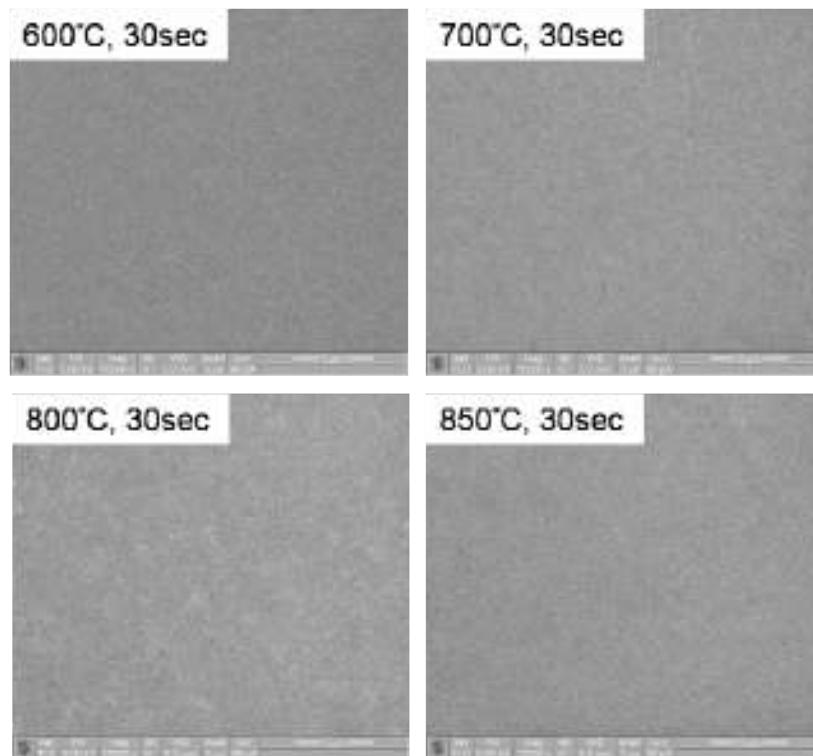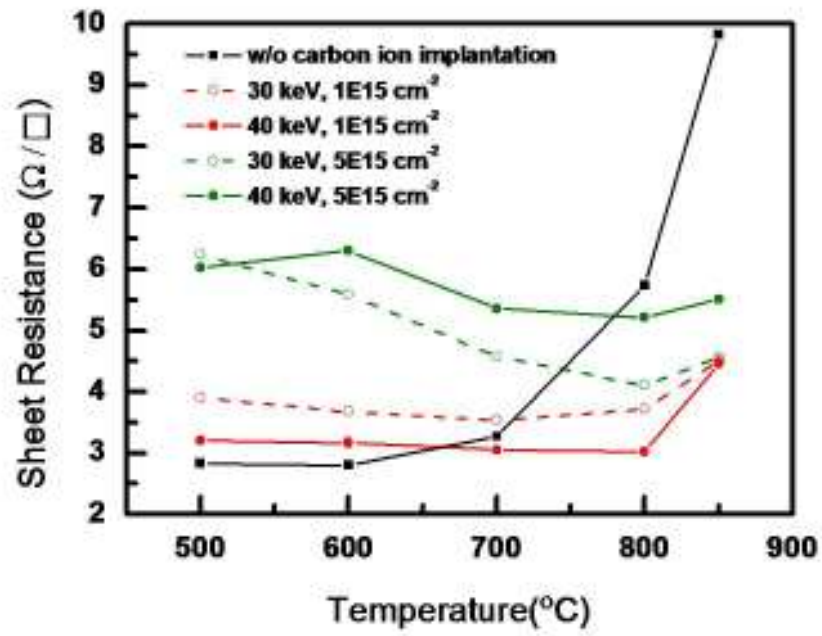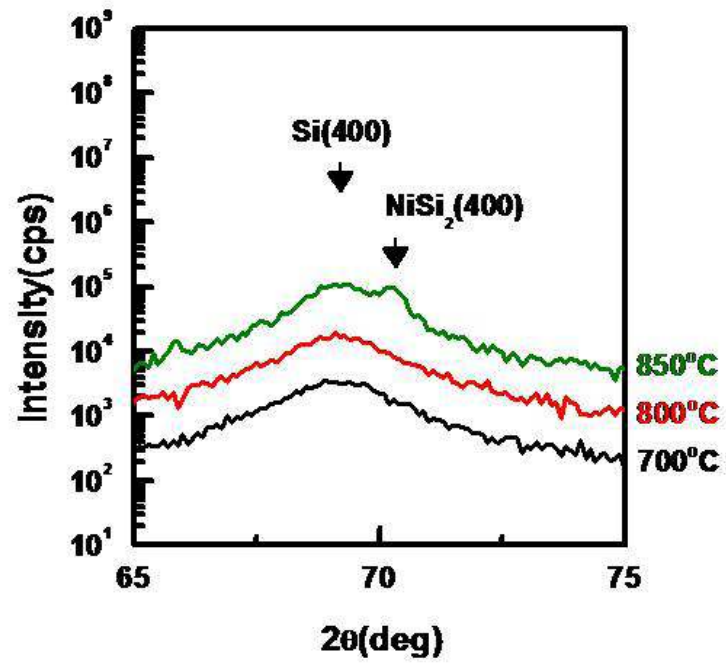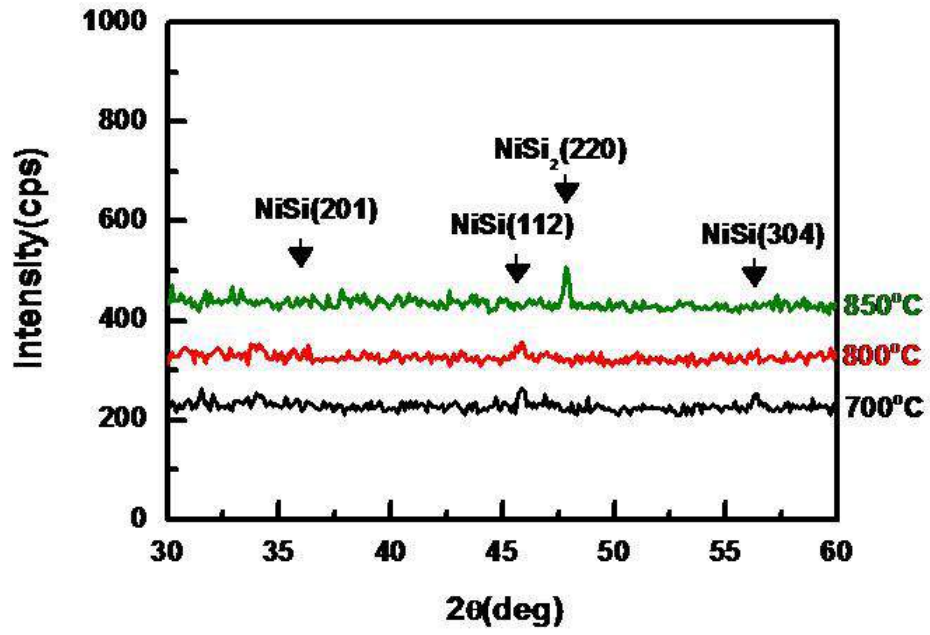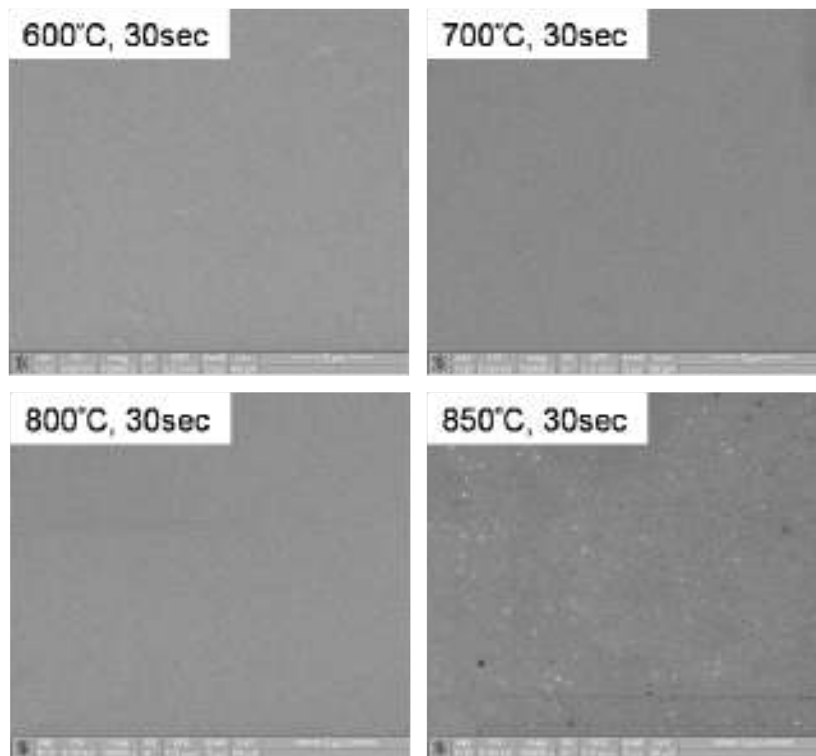Fig.2-8.　SEM micrographs for w/o CIA samples with a dose of 5×10^{15} cm^{-2} at 30 keV. Nickel silicide film agglomerates at 850 °C.

Chapter 3

Impact of Carbon Ion Implantation on the Thermal Stability of Nickel Silicide Contacted Shallow Junction

3.1 Introduction

Nickel monosilicide (NiSi) has been extensively investigated and used as a source/drain (S/D) contact material for a long time. NiSi has several advantages including low resistivity, low contact resistivity, a low-temperature process, less Si consumption during silicide formation, no narrow-line effect, and no bridging failure [1]. However, the main issue of NiSi film is its thermal stability at high temperatures. It is well known that NiSi film agglomerates to form small broken holes and then discontinuous islands at 700 °C, and the NiSi phase transforms into $NiSi_2$ phase at 700-750 °C. These two factors cause an increase in the sheet resistance (R_s) of the Ni-silicide film. Moreover, with the continuous scaling down of complementary metal-oxide-semiconductor (CMOS) devices, ultra shallow S/D junctions are becoming increasingly important in order to suppress the short-channel effect (SCE). The decrease in junction depth requires a decrease in NiSi film thickness, which has a strong effect on its thermal stability. Consequently, several methods of raising the thermal stability of NiSi film have been published [2-7]. These methods involve ion implantation (I/I) utilizing F or N_2 ions before NiSi formation, the deposition of Ti or Pt as a capping layer or an interposing layer, and the deposition of a $Ni_{1-x}Ti_x$ or $Ni_{1-x}Pt_x$ alloy.

Recently, Zaima et $al.$ reported that a p^+ $Si_{0.996}C_{0.004}$ epitaxial layer grown by low-pressure chemical vapor deposition (LPCVD) can effectively raise the thermal stability of NiSi film [8], and similar results were also reported by Nakatsuka et $al.$ [9]. The mechanism of suppressing the agglomeration and phase transformation of NiSi film is that C atoms segregate to the NiSi grain boundaries and NiSi/Si interface to modify the grain boundary and interfacial energy due to the low solid solubility of C atoms in NiSi [10].   Two common methods have been used to include C atoms within a Si substrate. One is $Si_{1-x}C_x$ epitaxial growth directly on a Si substrate [8, 10], and the other is C I/I into a Si wafer surface followed by thermal annealing [9, 11-12]. As a result of the extremely low solid solubility of C atoms in Si, the $Si_{1-x}C_x$ epitaxial process cannot easily achieve a higher substitutional C concentration than 1% (x>1%) [13]. In this chapter, we focus on C I/I technology. This

process is simpler than the epitaxy process and is compatible with the standard CMOS process flow. Moreover, it has been demonstrated that a $Si_{1-x}C_x$ S/D can produce tensile strain in the channel region, increasing the electron mobility and drive current of n-type metal-oxide-semiconductor field-effect transistors (NMOSFETs) [14-15]. Thus, C I/I technology is feasible for integration with n^+/p shallow junctions in the future.

The impact of the C I/I process on n^+/p shallow junction current-voltage (I-V) characteristics has not been studied in detail. In this chapter, we demonstrate and discuss the trade-off between the thermal stability of NiSi film and the n^+/p shallow junction I-V characteristics. Some methods of fabricating NiSi-contact n^+/p shallow junctions with both good thermal stability and excellent I-V characteristics are proposed.

3.2 Experiments

The starting material used in this study was boron-doped (100) 6-in.-diameter Si prime wafer with a resistivity of 2-7 Ω cm. After typical local-oxidation-of-silicon (LOCOS) isolation, a 70-nm-thick screen oxide layer was thermally grown. Next, C ions were implanted through the screen oxide at 40 keV to a dose of $1x10^{15}$ or $5x10^{15}$ cm^{-2}. The projected range of C ions is 58 nm under the Si surface. Then C I/I defects were eliminated by rapid thermal annealing (RTA) at 1100 °C for 30 s. Samples without C I/I were also prepared as reference. After etching the screen oxide by diluted HF (DHF) solution, arsenic (As) ions were implanted to a dose of $5x10^{15}$ cm^{-2} at 35 or 85 keV followed by a 1050 °C spike annealing process. The lower As I/I energy of 35 keV results in more dopants within the Ni-silicide film and a shallower junction depth. After removing the native oxide by DHF solution, a 25-nm-thick Ni layer and a 5-nm-thick TiN capping layer were continuously deposited by a sputtering system followed by a two-step annealing process to form NiSi [16]. The first step was performed at 300 °C for 60 min. After that, the TiN capping layer and the unreacted Ni were selectively removed by a mixture of H_2O_2:H_2SO_4=1:3. The second annealing step was performed at a temperature of 500-800 °C for 30 s in order to study the NiSi thermal stability. Finally, a 500-nm-thick Al layer was deposited on the wafer backside surface by a sputtering system to complete the fabrication of the n^+/p shallow junctions. Blanket samples without a LOCOS isolation structure were also fabricated for the purpose of material analysis. The main process flow of n^+/p shallow junctions is illustrated in Fig. 1. The notation used to identify different samples along with their fabrication conditions are summarized in Table I.

The four-point probe technique was used to measure the sheet resistance (R_s) of all

samples with blanket Ni-silicide films. X-ray diffraction (XRD) was adopted to distinguish the NiSi phase from the $NiSi_2$ phase. Scanning electron microscopy (SEM) was used to inspect the surface morphology of the Ni-silicide. The I-V characteristics of the n^+/p shallow junctions were measured by an Agilent 4156C precision semiconductor parameter analyzer.

3.3 Results and Discussion

A. Thermal stability

Figure 2 shows the measured R_s values as a function of silicide formation temperature with As I/I energy at 35 keV. The samples with the higher C I/I dose of $5x10^{15}$ cm^{-2} (C5As35) have slightly higher R_s values at a lower silicide formation temperature ($\leqq 700$ °C) due to the larger number of C atoms within the Ni-silicide film. Figures 3-5 display SEM images of the C0As35, C1As35, and C5As35 samples, respectively. The R_s values of the C0As35 samples increase from 700 °C because of NiSi film agglomeration. Many broken holes in the NiSi film can be seen in Fig. 3(b). On the other hand, few holes can be observed at 750 °C in the C1As35 samples, as shown in Fig. 4(c), and a continuous Ni-silicide film without any holes is obtained even at 800 °C in the C5As35 samples as shown in Fig. 5(d). Hence, it is confirmed that sufficient C atoms can effectively suppress the agglomeration of Ni-silicide film.

To understand the reason for the increased R_s values of the C1As35 samples at 750 °C and the C5As35 samples at 800 °C, XRD analysis was used to identify the Ni-silicide phase. The XRD spectra of C1As35 and C5As35 samples are shown in Figs. 6(a) and 6(b), respectively. In Fig. 6(a), it is observed that the $NiSi_2(400)$ phase appears at 750 °C in the C1As35 samples, and the NiSi(121) phase coexists in the Ni-silicide film at the same time. Furthermore, the NiSi(121) phase disappears and only the $NiSi_2(400)$ phase can be detected at 800 °C. In the C5As35 samples, the $NiSi_2(400)$ phase does not occur until 800 °C as shown in Fig. 6(b). According to these observations, it is clear that increasing the C I/I dose to $5x10^{15}$ cm^{-2} can retard the phase transformation of NiSi film. In summary, performing the C I/I process with a higher C dose of $5x10^{15}$ cm^{-2} is a feasible method for enhancing the thermal stability of NiSi film even if As dopants exist.

Figure 7 shows the measured R_s values as a function of silicide formation temperature with As I/I energy at 85 keV, and the corresponding SEM images and XRD spectra are shown in Figs. 8 and 9, respectively. The information revealed from these figures is similar to that discussed previously. Moreover, the phase transformation temperature of the C0As85 samples is 750 °C while that of the C0As35 samples is 700 °C. On the basis of the experimental

results of Ahmet *et al.* [17], we consider that the higher As I/I energy results in fewer As dopants within the NiSi film. Thus, the phase transformation temperature of the C0As85 samples is 50 °C higher than that of the C0As35 samples.

The agglomeration temperature and phase transformation temperature of all samples are summarized in Table II. It is clear that C I/I with a dose of 1×10^{15} cm^{-2} can raise the agglomeration and phase transformation temperatures of Ni-silicide film to 750 °C. By increasing the C I/I dose to 5×10^{15} cm^{-2}, the phase transformation temperature of Ni-silicide film can be further raised to 800 °C, and the agglomeration temperature becomes higher than 800 °C. The C I/I process successfully enhances the thermal stability of Ni-silicide film by at least 100 °C.

B. Junction characteristics

Figure 10 shows the I-V characteristics of the Ni-silicide-contact n$^+$/p shallow junction with As I/I energy at 35 keV. The junction area is 6.25×10^{-4} cm^2. Both the C1As35 and C5As35 samples exhibit the lowest leakage current at the silicide formation temperature of 500 °C. The lowest leakage value is approximately 10 nA/cm^2 at a reverse bias of 3 V, and this value is close to that of the junction without silicide. For the C0As35 and C1As35 samples, the leakage current increases with increasing silicide formation temperature. However, the samples with a C I/I dose of 5×10^{15} cm^{-2} exhibit very different reverse leakage current behavior. For the C5As35 samples, when the silicide formation temperature increases to 600 °C, the leakage current abruptly increases by 3 orders of magnitude. Then the leakage current decreases as the silicide formation temperature increases to 700 and 750 °C, but increases again as the silicide formation temperature increases to 800 °C. Figures 11 and 12 show statistics of the junction leakage current at a reverse bias of 3 V for the Ni-silicide-contact n$^+$/p shallow junctions with As I/I at 35 and 85 keV, respectively. The silicide formation temperature dependences of the junction leakage current described above are confirmed to be universal behavior. The same leakage current dependence on the silicide formation temperature and C I/I dose can also be found at an As I/I energy of 85 keV as shown in Fig. 12.

Three mechanisms are considered to have an effect on the junction leakage current. The first one is the agglomeration of the Ni-silicide film. Agglomeration causes an increase in interface roughness at the Ni-silicide/Si contact, and the junction leakage current may increase owing to structural damage. The second is the diffusion of Ni atoms. The many defects

produced by the high-dose I/I process form the diffusion path. Ni atoms can rapidly diffuse via these defects during silicide formation. As Ni atoms diffuse toward the junction depletion region and form deep levels, the junction leakage current increases. The third is the phase transformation from the NiSi phase to the NiSi$_2$ phase. When the phase transformation occurs, the thickness of the silicide film becomes double that of the NiSi film. Thus, the Ni-silicide/Si interface becomes closer to the junction depletion region. Agglomeration can easily damage the junction depletion region, and more Ni atoms arrive at the junction depletion region to contribute to the junction leakage current. Agglomeration and the phase transformation occur at a high silicide formation temperature and depend on the silicide formation temperature and C I/I dose. In addition to the silicide formation temperature, the effect of the diffusion of Ni atoms is also related to the number of I/I defects, which depends on the C I/I dose.

For the reasons mentioned above, the deeper junction has fewer Ni atoms within the junction depletion region. Moreover, the agglomeration and phase transformation also have less impact on the deeper junction. Hence, by comparing Figs. 11 and 12, it can be seen that the leakage current at an As I/I energy of 85 keV is much lower than that of 35 keV at a high silicide formation temperature.

When the C I/I dose is zero or equal to 1×10^{15} cm^{-2}, the number of defects is not large enough to form a long diffusion path for Ni atoms. Hence, the agglomeration and phase transformation dominate the junction leakage current mechanism, and the junction leakage current increases with silicide formation temperature. Because the C1As35 and C1As85 samples have better thermal stability of the Ni-silicide film, both samples exhibit a lower leakage current than the C0As35 and C0As85 samples with silicide formation temperatures of 700 and 750 °C .

On the other hand, when the C I/I dose increases to 5×10^{15} cm^{-2}, it generates many remnant defects, and Ni atoms can diffuse very rapidly via these defects. Therefore, the diffusion of Ni atoms dominates the junction leakage current mechanism. The leakage currents of the C5As35 and C5As85 samples are similar to that of the C0As35 sample at 500 °C, as can be observed by comparing Figs. 11 and 12. This indicates that most of the defects generated by a high C I/I dose were annihilated by RTA at 1100 °C for 30 s. Figures 13(a) and 13(b) show the SIMS depth profiles of C, As, and Ni atoms of the C5As85 and C0As85 samples with the silicide formation temperature at 600 °C, respectively. The different surface NiSi thicknesses of these two samples is due to the thickness variation of the as-deposited Ni films. Hence, all of the depth profiles were measured from the NiSi/Si interface, which is

defined as the intersection of the Ni and As depth profiles. Rucker *etal.* reported that substitutional C atoms can enhance As dopants diffusion, but the diffusion enhancement effect ends when most of the C atoms precipitate [18]. In the case of our C5As85 samples, C atoms were incorporated by ion implantation, and this process produced a large number of Si interstitials. It is well known that C atoms can trap Si interstitials to eliminate secondary defects during high-temperature annealing [19]. Hence, C atoms combine with Si interstitials and precipitate to form immobile clusters during high-temperature annealing. Compared with the epitaxial Si:C layer in Rucker *et al.*'s experiment, most of the C atoms are not located at substitutional sites in our C5As85 samples. Therefore, no As diffusion enhancement is observed upon comparing Fig. 13(a) with Fig. 13(b). It is observed that the Ni depth profile of the C5As85 sample has an apparent hump whose position coincides with the peak of the C depth profile. The distance between As and Ni atom depth profiles measured at an As atom concentration of 1×10^{18} cm^{-3} is indicated in Figs. 13(a) and 13(b). The Ni distribution of the C5As85 sample is about 15 nm closer to the n^{+}/p junction than that of the C0As85 sample. This implies that the C5As85 sample has more Ni atoms within the junction depletion region owing to the dissolution and diffusion of Ni atoms toward the junction depletion region along the many defects induced by C I/I with a dose of 5×10^{15} cm^{-2} during silicide formation. This explains why the C5As35 and C5As85 samples unexpectedly exhibit the highest leakage current at 600 °C. We consider that it can generate more and more vacancies injecting into Si substrate during Ni-silicide formation at a higher temperature [20]. These vacancies can combine and remove some residual defects, so that fewer Ni atoms can diffuse into the junction depletion region. Therefore, the junction leakage current decreases as the silicide formation temperature increases to 700 and 750 °C. Finally, the increase in the leakage current again at 800 °C is a result of the agglomeration and phase transformation of the Ni-silicide film.

To suppress the diffusion of nickel atoms, we propose two solutions. One method is to ensure that the carbon distribution is shallower than the junction depletion region by introducing a lower carbon ion implantation energy. Thus, a higher concentration of carbon atoms near the Si substrate surface can be obtained. We predict that this will further enhance the thermal stability of the nickel silicide film. Furthermore, defects are far away from the junction, thus reducing the leakage current. The other method is to eliminate the defects as completely as possible. Raising the thermal budget of RTA or developing other annealing processes to eliminate these defects will be researched in the future.

3.4 Conclusions

We have investigated the impact of carbon ion implantation on the thermal stability of nickel silicide. Although carbon atoms exist within nickel silicide, may increase the sheet resistance at low silicide-formation temperature ($\leqq 700$ °C) due to C segregation at grain boundary, the increased sheet resistance value is only slightly larger than that of the reference sample without C^+ implantation. For the CIA samples, the increased of sheet resistance value is smaller than 1 $\Omega/\square$. Sufficient carbon atoms, a dose of 5×10^{15} cm^{-2}, can effectively suppress the agglomeration and phase transformation. For the CIA samples with a dose of 5×10^{15} cm^{-2} at 40 keV, agglomeration and phase transformation indeed can be suppressed completely even at 850 °C. Hence as the silicide-formation temperature exceeds 700 °C, samples with C^+ implantation have lower Rs values than the reference samples. The thermal stability of nickel silicide can be improved by as high as 150 °C with the optimum C^+ implantation condition of 5×10^{15} cm^{-2} at 40 keV.

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Table.3-1. Summary of results of the agglomeration and phase transformation temperature of all samples.

Spilt condition		Agglomeration	Phase transition
30keV, 1E15 cm^{-2}	CIA	800 °C	800 °C
	w/o CIA	800 °C	800 °C
40keV, 1E15 cm^{-2}	CIA	800 °C	800 °C
	w/o CIA	800 °C	800 °C
30keV, 5E15 cm^{-2}	CIA	850 °C	850 °C
	w/o CIA	850 °C	850 °C
40keV, 5E15 cm^{-2}	CIA	>850 °C	850 °C
	w/o CIA	850 °C	>850 °C

Table.3-2. Summary of results of agglomeration and phase transformation temperatures of all samples.

Sample ID	Agglomeration temperature (°C)	Phase transition temperature (°C)
C5As35	> 800	800
C1As35	750	750
C0As35	700	700
C5As85	> 800	800
C1As85	750	750
C0As85	700	750

(a) screen oxide
FOX | FOX
P-type Substrate
• LOCOS isolation
• screen oxide : 70 nm

(b) C⁺
FOX | FOX
P-type Substrate
• C$^+$ I/I : 40 keV / 5x10^{15} cm^{-2}
• RTA : 1100 ^{o}C / 30 sec

(c) As⁺
FOX | FOX
P-type Substrate
• As$^+$ I/I : 35 or 85 keV / 5x10^{15} cm^{-2}
• Spike RTA : 1050 ^{o}C

(d) Ni silicide
FOX | FOX
Al | P-type Substrate
• 2-step Ni silicide formation
• backside Al deposition : 500 nm
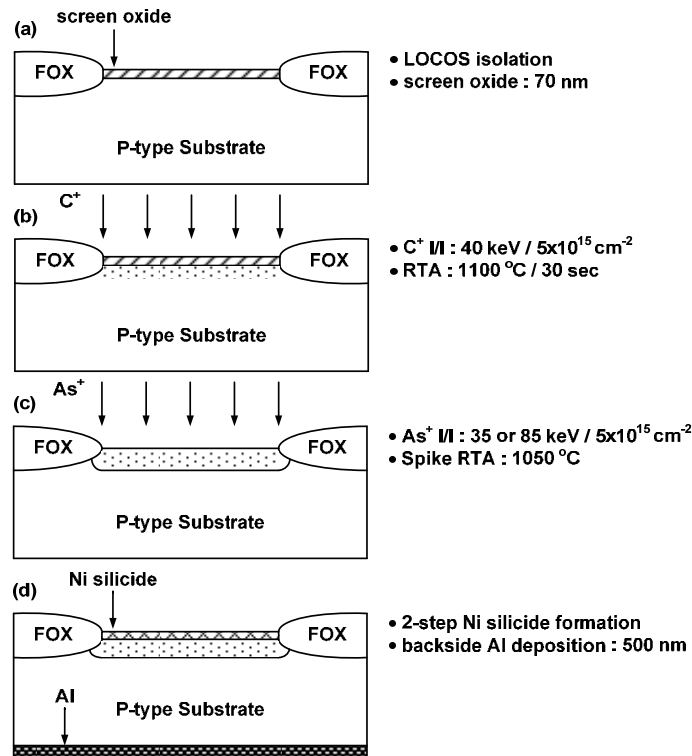
Fig.3-1 Main process flow of the n$^+$/p shallow junction: (a) after LOCOS isolation and screen oxide growth, (b) after carbon ion implantation and annealing, (c) after arsenic ion implantation and activation, and (d) the final structure.
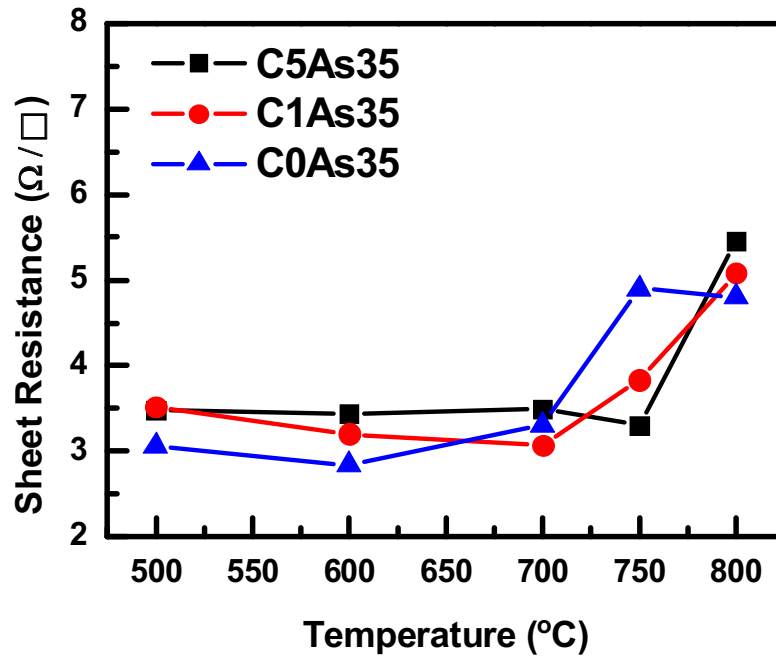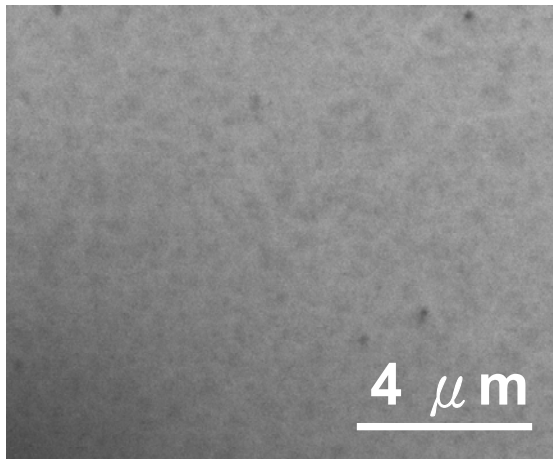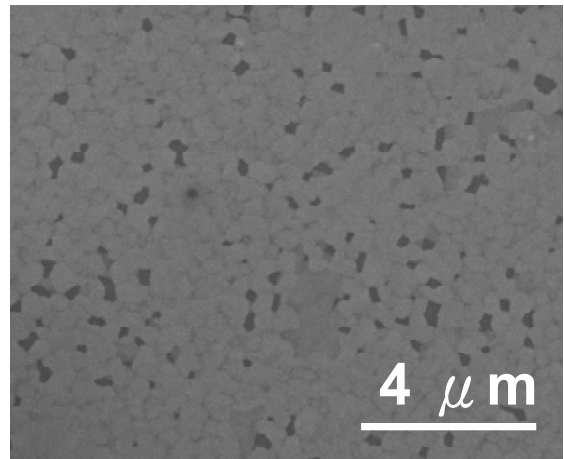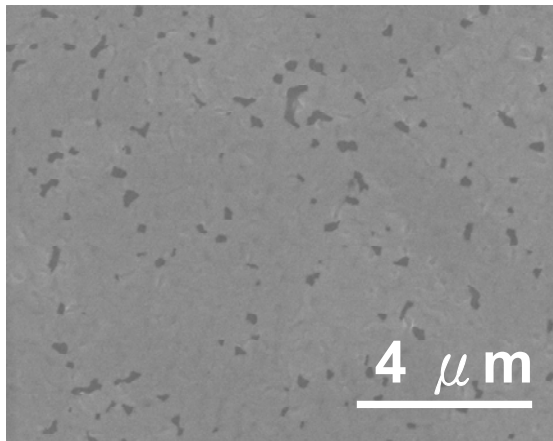

Fig.3-2 Sheet resistance values as a function of silicide formation temperature with As I/I energy at 35 keV and different C I/I doses.
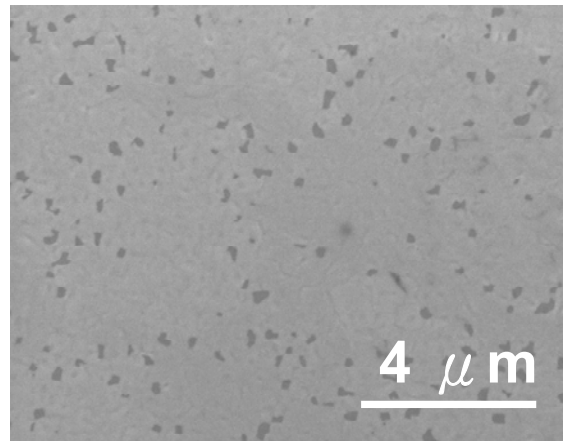
(a) 600 ℃   (b) 700 ℃
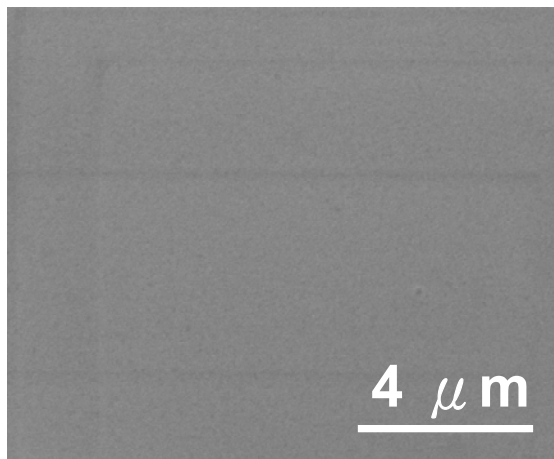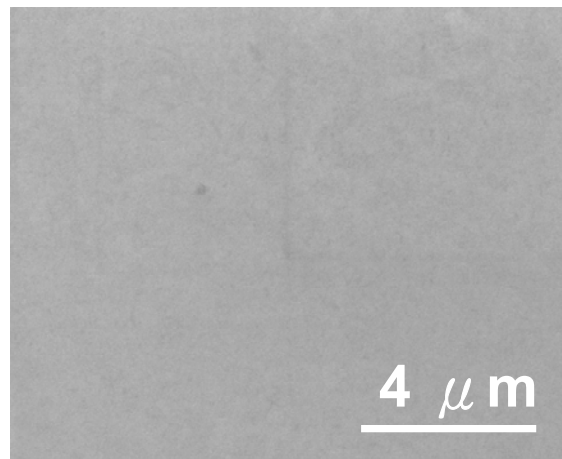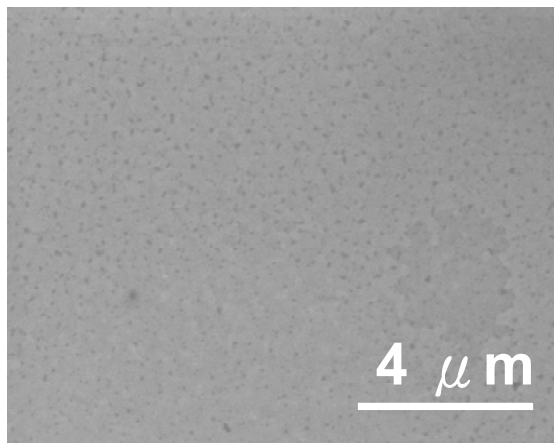
(c) 750 ℃   (d) 800 ℃

Fig.3-3 SEM images of the C0As35 samples with different silicide formation temperatures: (a) 600 °C, (b) 700 °C, (c) 750 °C, and (d) 800 °C. Several holes are generated within the Ni-silicide film at 700 °C, causing an increase in sheet resistance.

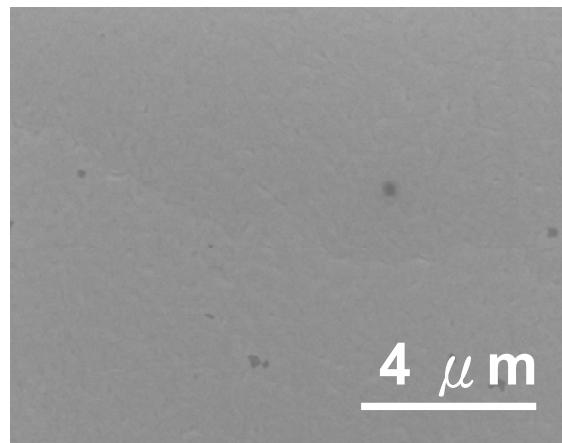**(a) 600 ℃**

(b) 700 ℃

(c) 750 ℃

(d) 800 ℃

Fig.3-4 SEM images of the C1As35 samples with different silicide formation temperatures: (a) 600 °C, (b) 700 °C, (c) 750 °C, and (d) 800 °C. Only a few small holes can be observed at 750 °C.

(a) 600 ˚C

(b) 700 ˚C

(c) 750 ˚C

(d) 800 ˚C

Fig.3-5 SEM images of the C5As35 samples with different silicide formation temperatures: (a) 600 °C, (b) 700 °C, (c) 750 °C, and (d) 800 °C. No holes can be observed, and the Ni-silicide film retains an intact structure.
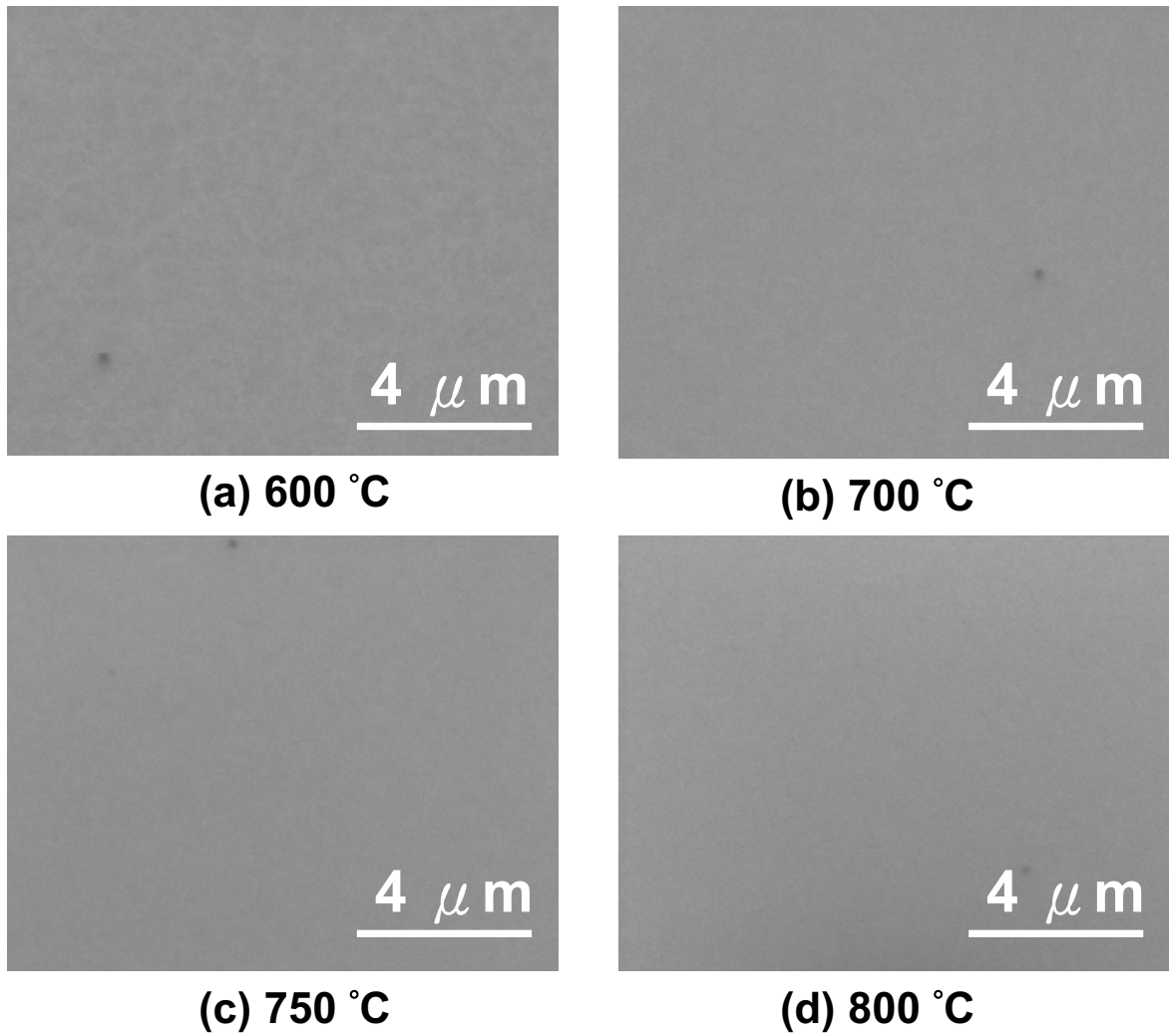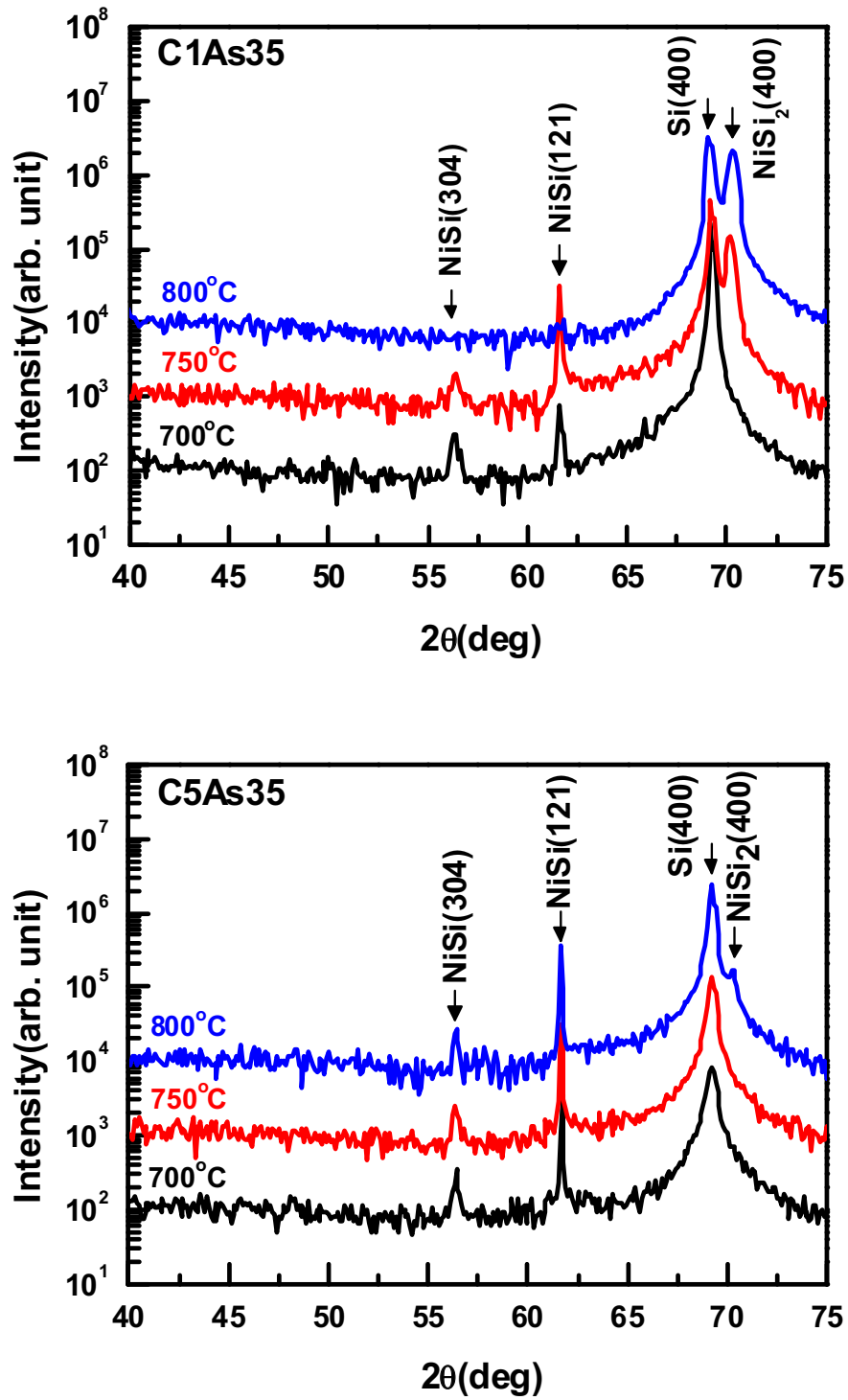
Fig.3-6 XRD spectra of the (a) C1As35 samples and (b) C5As35 samples. The NiSi$_2$ phase appears to cause an increase in the sheet resistance at 750 °C in the C1As35 samples and at 800 °C in the C5As35 samples.
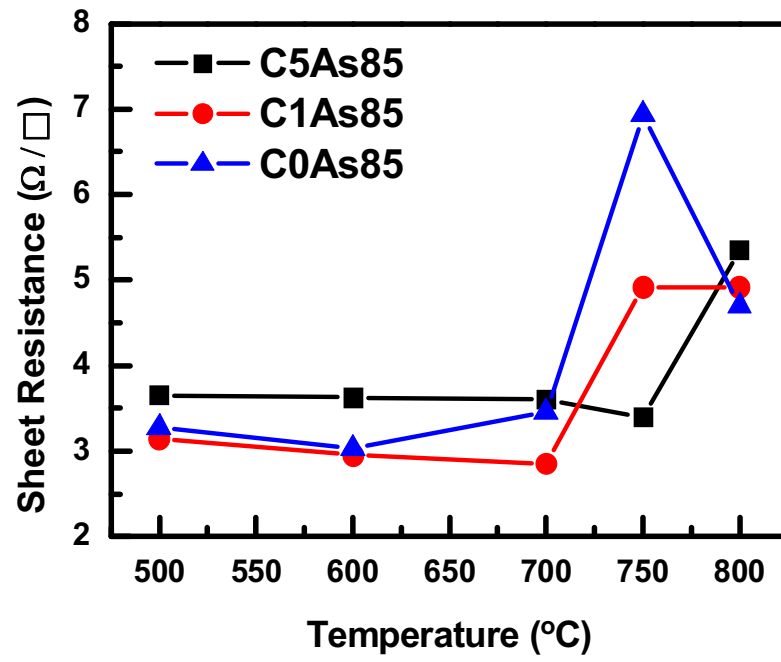
Fig.3-7 Sheet resistance values as a function of silicide formation temperature with As I/I energy at 85 keV and different C I/I doses.
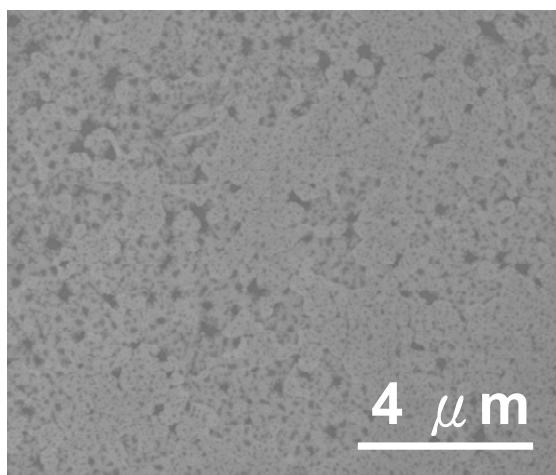
(a) C0As85 @ 700 ˚C
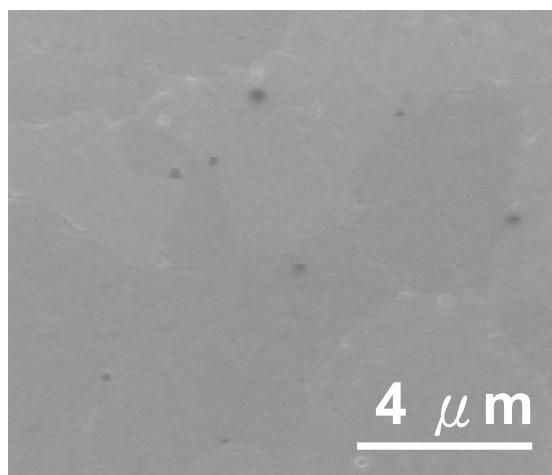
(b) C1As85 @ 750 ˚C
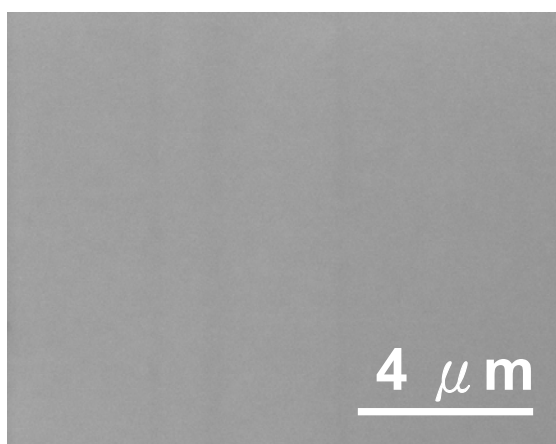
(c) C5As85 @ 750 ˚C
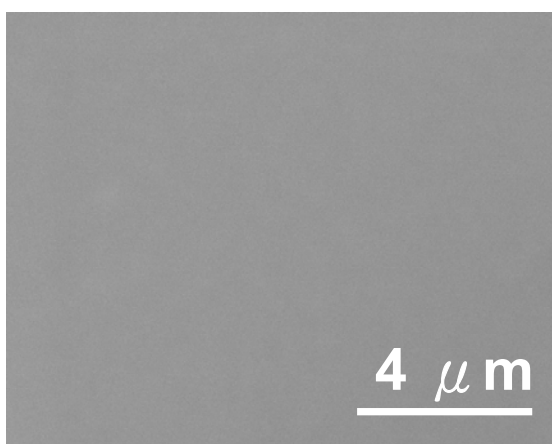
(d) C5As85 @ 800 ˚C

Fig.3-8 SEM images at agglomeration temperature with As I/I energy at 85 keV and various C I/I doses: (a) C0As85 at 700 °C, (b) C1As85 at 750 °C, (c) C5As85 at 750 °C, and (d) C5As85 at 800 °C.
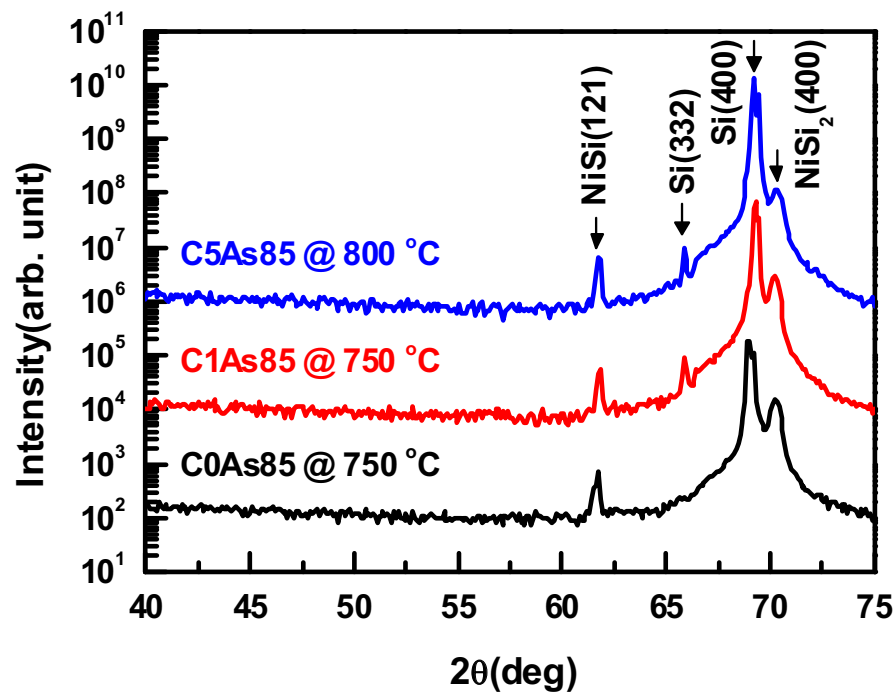
Fig.3-9 XRD spectra at phase transformation temperature with As I/I energy at 85 keV and various C I/I doses
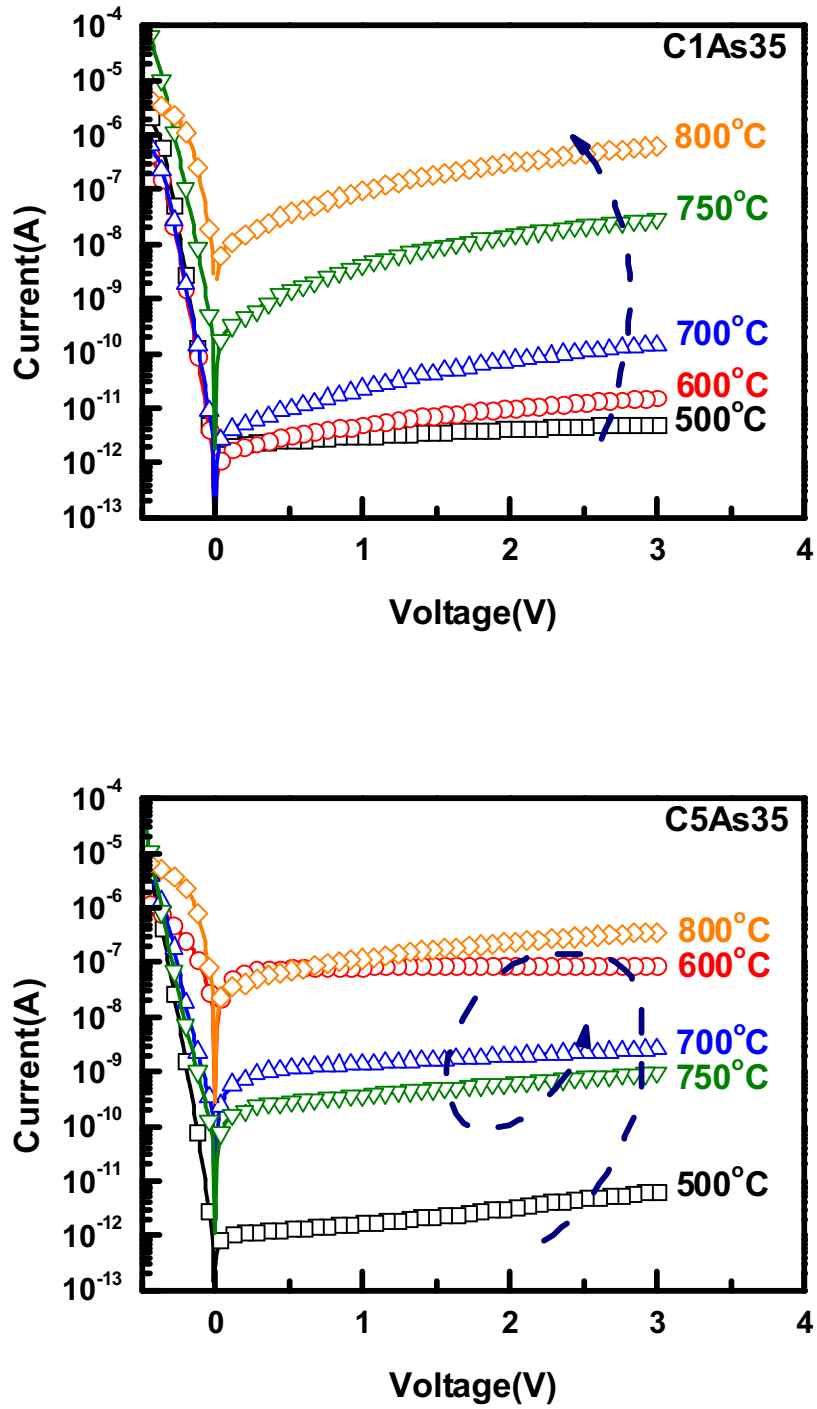
Fig.3-10　Silicide formation temperature dependences of leakage current characteristics of Ni-silicide-contact n^+/p shallow junction with As I/I energy at 35 keV: (a) C1As35 samples and (b) C5As35 samples.
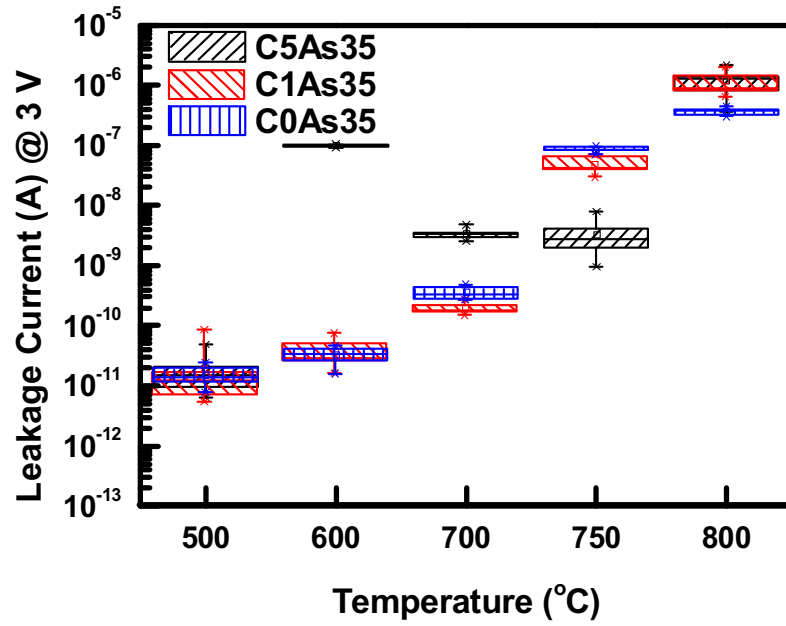
Fig.3-11 Statistics of the reverse-bias junction leakage current at 3 V for the Ni-silicide-contact n^{+}/p shallow junctions with As I/I at 35 keV.
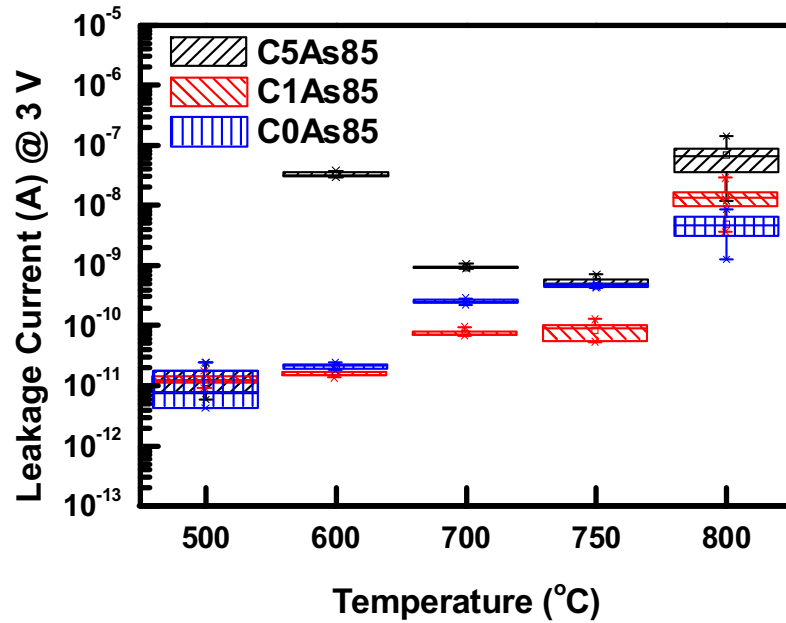
Fig.3-12 Statistics of the reverse-bias junction leakage current at 3 V for the Ni-silicide-contact n^{+}/p shallow junctions with As I/I at 85 keV.

Fig.3-13 SIMS depth profiles of C, Ni, and As of the (a) C5As85 and (b) C0As85 samples with silicide formation temperature at 600 °C.

Chapter 4

Si-C Formation by Low Temperature Carbon Ion Implantation

4.1 Introduction

Low temperature ion implantation process is performed by putting wafer on a low temperature chuck to make the wafer temperature low. Low temperature wafer contains less thermal energy, thus the self annealing effect during implantation process can be reduced. In this way, the surface amorphous layer created by low temperature ion implantation will have better quality than that created by ion implantation at room temperature or higher temperature. High quality amorphous layer can improve the crystalline quality of substrate after annealing, and is beneficial for Si-C forming.

In this chapter, we use low temperature ion implantation to implant carbon ions. The basic characteristic of low temperature carbon ion implanted silicon substrate is examined. Different experimental conditions are investigated to find the best condition for Si-C forming.

4.2 Experiments

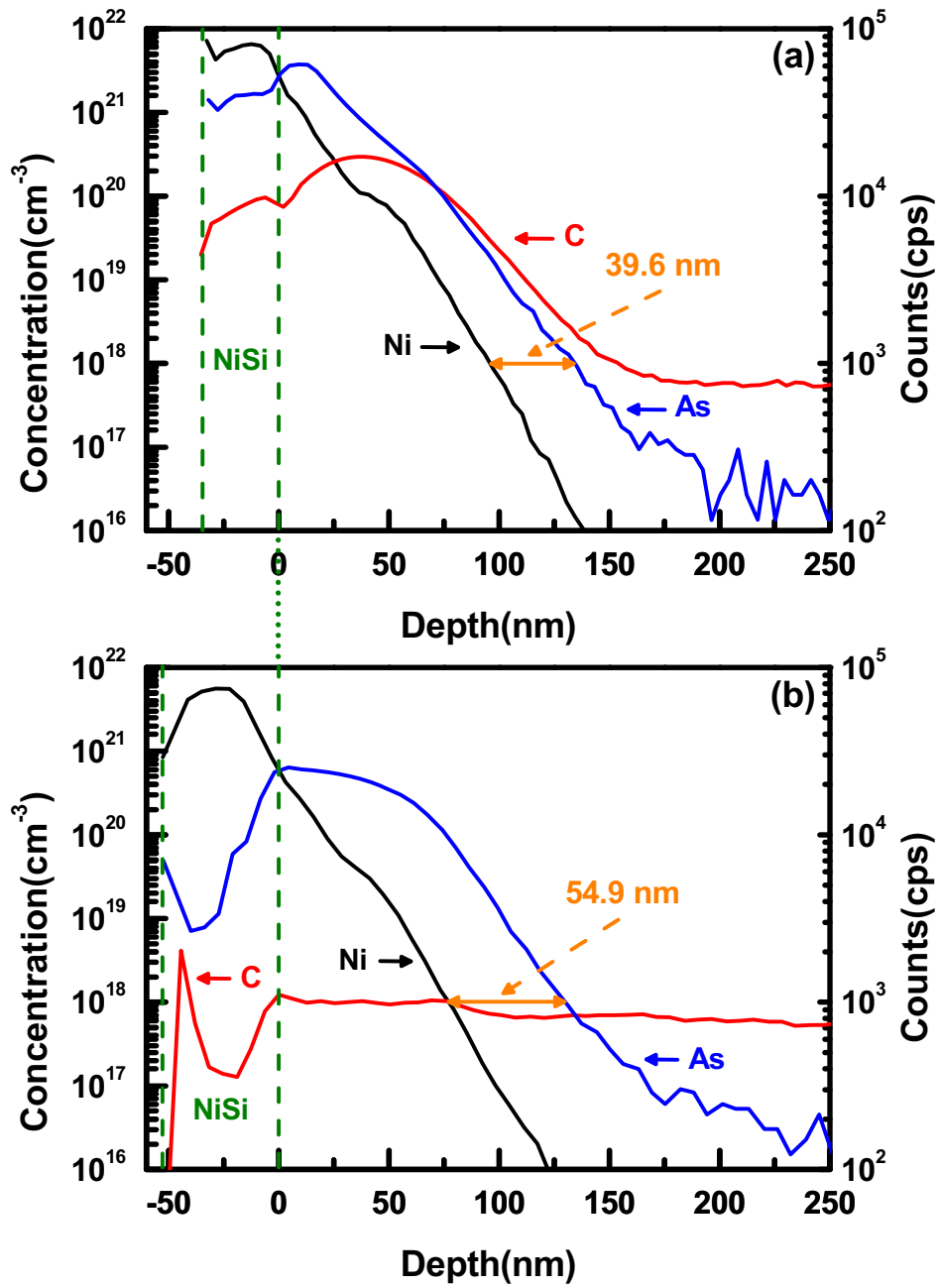### A. Low Temperature Ion Implantation

The low temperature ion implanter used in this chapter is model iPulsar produced by Advance Ion Beam Technology Co. (AIBT). The allowed implantation energy range is 100 eV – 40 keV and the dose range is 1×10^{13} to 5×10^{16} ions/cm^2. Tilt angle is from 0˚ to 45˚ and the twist angle is from 0˚ to 360˚. Since the implanter is designed for 12-inch wafer process, we use a 12-inch wafer as wafer holder, and attach 6-inch wafer on it, then put the holder on the chuck to perform ion implantation.

The iPulsar system contains one focused ion beam 2D mechanical scan system and one uniform strip shape ion beam 1D mechanical scan system, can provide various kind of implantation, especially low energy ion implantation. The cold wafer e-chuck in the iPulsar system is a special equipment, and is one of the major differences compare to conventional ion implanters. During the process, the chiller is flowed through the e-chuck and makes the chuck temperature low, the lowest temperature that e-chuck could achieve is -20 °C. The backside gas flow between the wafer backside and chuck is controlled to conduct the heat.

Low temperature e-chuck can lower the temperature of wafer, and can provide several process benefits.

B. Substitutional Carbon Density Sample

Six-inch-diameter p-type (100) silicon wafers with nominal resistivity of 15~25 Ω-cm were used as substrates. The low temperature ion implantation was performed at chuck temperature of 5°C or -15°C. The implant energy is at 3 keV, 5 keV, 7 keV, and 9 keV. The implantation dose is controlled to $2\sim5\times10^{15}$ cm^{-2}. The implantation conditions of samples are labeled in the form of energy/dose. For the samples implanted at 5℃ chuck temperature the implantation conditions are 3 keV/5×10^{15} cm^{-2}、5 keV/5×10^{15} cm^{-2} and 7 keV/5×10^{15} cm^{-2}. For the samples implanted at -15°C chuck temperature, the implantation conditions are 7 keV/5×10^{15} cm^{-2}、7 keV/8×10^{15} cm^{-2}、9 keV/5×10^{15} cm^{-2} and 3 keV/2×10^{15} cm^{-2}+ 5 keV/3×10^{15} cm^{-2}+ 7 keV/3×10^{15} cm^{-2}. Then all the samples accepted additional phosphorous ion implantation at 17 keV to a dose of 5×10^{15} cm^{-2}. After phosphorus ion implantation, the samples were cut into small pieces and two steps of annealing process were performed for SiC formation. In the first step, samples were annealed in N$_2$ ambient by a rapid thermal annealing (RTA) system at temperatures ranging from 650 °C to 850 °C for 90 to 180 secs. In the second step, some of the samples were annealed in N$_2$ ambient by a RTA system at temperature of 1000°C for 1sec second. Some samples were annealed by a pulse laser annealing (PLA) system. A 248nm KrF excimer laser was used as laser source, the laser energy is 350 mJ/cm^2, the pulse duration is around 25 ns/shot and the number of shots ranges from 5 to 20.

The same process steps were also performed on the CPIII samples to evaluate the substitutional carbon density of the CPIII process. The carbon ion implant condition is 3K5M and the annealing temperature is 650°C and 750°C for 120 secs.

C. Material Analysis

Several Material Analysis techniques include XRD、SEM、SIMS and TEM were used in our experiment. XRD analysis has two main purposes in this experiment. The first one is to find out the nickel silicide phase transformation temperature. The second purpose of XRD is to calculate the number of substitutional carbon by using the rocking curve method proposed by P. C. Kelires in 1997 [1]. This model can calculate the atomic percentage of the

substitutional carbon in Si matrix (C_{sub}) by the lattice constant difference (Δd) obtained from the XRD rocking curve. The detail is introduces in the next paragraph. First, the lattice constant difference Δd between Si and $Si_{1-x}C_x$ could be obtained by the XRD rocking curve result. The lattice constant of $Si_{1-x}C_x$ on the growth direction $a_\perp$ can be calculated by

$$a_\perp = a_{Si} + \Delta d \ (a_{Si} = 5.431A)$$

After obtained the value of $a_\perp$, the value of relaxed lattice parameter a_{rel} can be calculated by

$$a_{rel} = \left[(a_\perp - a_\parallel) \div \left(1 + 2\frac{C_{12}}{C_{11}}\right)\right] + a_\parallel$$

Finally the value x of $Si_{1-x}C_x$ can be extracted by solving the following Equation

$$a_{rel} = a_{Si} - 2.439x + 0.5705x^2$$

Scanning Electron Microscope (SEM) is used to inspect the surface morphology of the carbon implanted nickel silicide samples after annealing at different conditions. The surface continuity and the level of agglomeration can be observed by SEM inspection. Secondary Ion Mass Spectrometry (SIMS) is used to analysis the depth profiles of carbon and phosphorus atoms in samples after ion implantation and annealing. Transmission Electron Microscopy (TEM) is used to observe the microstructure of samples. It can help to figure out the thickness of amorphous layer and the level of amorphization.

For electrical measurement, the sheet resistances of all blanket samples were measured by four point probe.

4.3 Basic Material Analysis

We performed SIMS and TEM on the sample with carbon implanted at 7 keV and a dose of 5×10^{15} cm^{-2}. The chuck temperature was -15℃ during ion implantation. After carbon implantation, additional phosphorous ion implantation at 17 keV to a dose of 5×10^{15} cm^{-2} was performed. Both the as-implanted sample and the samples annealed at 750°C for 120 sec were analyzed. Fig.4-1 shows the SIMS depth profiles of carbon and phosphorus atoms of the as-implanted sample. It is observed that most of carbon atoms are located at the region between 25nm to 30nm from the surface. And the phosphorous atoms are located at the region between 18nm to 30nm from the surface. Fig.4-2 shows the SIMS depth profiles of carbon and phosphorus of the 750°C annealed sample. The carbon profile is nearly the same with that of the as-implanted sample. In Fig.4-3 we compare the phosphorous depth profiles of annealed sample to the as-implanted sample. After annealing, the concentrations of phosphorous in the region between 25nm to 43nm and between 49nm to 78nm significantly

decreases and the concentrations of phosphorous in the region between 16nm to 24nm and between 44nm to 48nm increases evidently. In the deeper region of the silicon substrate, the number of phosphorous increased for less than one order.

The change of depth profiles indicates that phosphorous atoms diffuse from the original location toward the shallower region of the silicon substrate. The concentration of phosphorous in the tail region didn't increase significantly, which means the phosphorous diffusion to the substrate is not affected by carbon. B. J. Pawlak et al. reported that the implanted carbon in the silicon substrate can catch Si_i (interstitial silicon) to form Si-C cluster and reduce the number of Si_i [2]. As the number of Si_i decreases, the interstitial assisted transient enhanced diffusion (TED) will be suppressed and the depth of dopant diffused to the substrate will be reduced. We can also find that the concentration of phosphorous in the original carbon rich region significantly decreases after annealing, and the phosphorous distribution is shallower than the as-implanted distribution. This observation can be explained by a model which is similar to that proposed by B. J. Pawlak. In typical case, the Si_{ii} distributed near the Si surface will diffuse toward to Si surface because the free Si surface acts efficient Si_i sink, while the Si_i distributed deeper than the project range (R_p) of the implanted ions will diffuse toward the Si substrate because of the concentration gradient. With carbon ion implantation, some of the Si_i in the carbon rich region tends to diffuse toward the bulk will be caught by carbon. The Si_i assisted TED on phosphorus would be suppressed. Therefore, the depth of phosphorus becomes shallower. In the region between Si surface and the R_p of phosphorus, the concentration of Si_i does not affected by carbon effectively. The upward diffused Si stream results in the increase of phosphorus near Si surface. This characteristic might be applied to ultra shallow junction fabrication, is one of the benefit of carbon ion implantation process.

Fig.4-4 shows the TEM image of 7 keV/5×10^{15} cm^{-2} low temperature (5°C) carbon implanted sample. We can observe that the surface amorphous layer thickness is about 49nm to 50nm and is near totally amorphous. The boundary of amorphous layer and silicon substrate is clear but not very smooth. Fig-4.5 is the TEM image of 7 keV/5×10^{15} cm^{-2} low temperature (-15°C) carbon implanted sample. We can find its amorphous layer thickness is 49 nm to 50 nm which is very similar to the 5°C implanted sample. The amorphous layer is totally amorphous, and the boundary of amorphous layer and silicon substrate is complete and smooth, it means the level of amorphous is higher than the amorphous layer of 5°C implanted sample but the difference is not very significant. The TEM image of 7 keV/5×10^{15} cm^{-2} low

temperature (-15°C) carbon implanted sample after annealing at 750°C for 120 sec is showed in Fig.4-6. We can observe that the amorphous layer thickness reduced to about 22nm.after annealing, and the layer between amorphous layer and the 49nm deep region were re-crystallized. The result indicates that during the annealing process, surface amorphous layer were re-crystallized and formed SiC from the bottom of amorphous layer. As the re-crystallized layer extended to the R_p of phosphorous implant which is about 22nm deep from the surface, it stops re-crystallization because the project range defect of phosphorous revealed. We can also clearly see that there are two defect layers, one is project range defect of phosphorous on the boundary of amorphous layer and re-crystallized layer and is about 22 nm to 23 nm deep. The other one is secondary defect at the boundary of re-crystallized layer and silicon substrate, and is about 49 nm to 50 nm deep. This is match with the phosphorous profile peak we observed in the SIMS result, which indicates that after annealing phosphorous in the carbon-rich region would diffused with the Si_i, and trapped by the two defect layer.

4.4 Si-C Formation

In this section, we discuss the Si-C formation on the low temperature carbon ion implanted silicon substrate. Both implantation conditions and annealing conditions are discussed. The Si-C formation results are also compared with those of the CPIII sample.

A. Effect of Implantation Condition

At first, we control the samples with the same annealing condition and then discuss the effect of ion implantation conditions including energy, dose, and chuck temperature on Si-C forming.

A-1. Effect of Implantation Energy

We perform carbon implantation at chuck temperature 5°C and implantation energy from 3 keV to 7 keV, and at chuck temperature -15°C and implantation energy at 7 keV and 9 keV. The 5°C samples were annealed in N_2 ambient at 700 °C for 120sec, and the -15 °C samples were annealed in N_2 ambient at 750 °C for 120 sec to form Si-C.

From the XRD rocking curve results shown in Fig.4-7, we find that the differences in angle between Si and Si-C peaks increase from 0.125 to 0.185 as the implantation energy increases from 3 keV to 5 keV. When the implantation energy increases to 7 keV, the difference further increases to 0.28. After calculation using the Kelires model [1], the atomic

percentage of the C_{sub} (substitutional carbon) is only 0.501% at 3 keV and as the energy increases to 5 keV, the C_{sub} increases to 0.743%. The C_{sub} increases to 0.973% as the implantation energy further increases to 7 keV. From these results we can see that the C_{sub} increases as the implantation energy increases. In Fig.4-8 we compare the results of the 7 keV and 9 keV samples, the C_{sub} increases from 1.027% to 1.047 %. This difference is not significant.

The reason for the above results might be due to the difference in amorphous layer created by different implantation energies. In the research of K. Sekar et al., they found that the C_{sub} will increase as the surface amorphous layer is thicker or the amorphous level is higher [3]. When energy increases from 3 keV to 7 keV, the amorphous layer thickness becomes thicker and level of amorphous becomes higher, so the C_{sub} increases obviously. But when the energy increases from 7keV to 9keV, since the surface is nearly totally amorphous when the energy is 7 keV, the amorphous layers created at 7 keV and 9 keV don't have evident difference, therefore, the C_{sub} don't have much difference.

A-2. Effect of Implantation Dose

To study the implantation dose effect, we fixed the carbon implantation temperature at 5°C and implantation energy at 7 keV while the dose were controlled to 5×10^{15} cm^{-2} and 8×10^{15} cm^{-2}. The samples were annealed in N_2 ambient at 750°C for 120 sec.

From the XRD rocking curves shown in Fig.4-9, it is found that the C_{sub} slightly increases from 1.037% to 1.127% when the dose increases from 5×10^{15} cm^{-2} to 8×10^{15} cm^{-2}. But the Si-C peak of the 8×10^{15} cm^{-2} sample is broader and the peak intensity is lower than that of the 5×10^{15} cm^{-2} sample. The differences in the Si-C peaks indicate the crystalline quality of the Si-C is better in the 5×10^{15} cm^{-2} sample. The Si reference peak of the 8×10^{15} cm^{-2} sample is also broader than that of the 5×10^{15} cm^{-2} sample, that means there are more interstitial carbons in the 8×10^{15} cm^{-2} sample. Comparing the R_s (sheet resistance) values, the value of the 8×10^{15} cm^{-2} sample is 391.7 $\Omega/\square$ and the value of the 5×10^{15} cm^{-2} sample is 258 $\Omega/\square$. The significantly higher R_s value of the 8×10^{15} cm^{-2} sample supports the poor crystalline quality of this sample.

Since the solid state solubility of carbon in silicon is very low [4], most of the implanted carbons are at interstitial sites. When carbon dose increases from 5×10^{15} cm^{-2} to 8×10^{15} cm^{-2}, the amount of carbon incorporated into the interstitial site increases significantly. These interstitial carbons will form interstitial carbon defects [5] and increases the R_s value, the two

effects are detrimental to S/D engineering. In summary, higher carbon dose can slightly increase the C_{sub}. But considering the negative effects brought by the large amount of interstitial carbons, carbon dose should not be higher than 5×10^{15} cm^{-2}.

A-3. Effect of Chuck Temperature

The effect of chuck temperature at 5°C and -15°C is examined. The implantation condition fixed at 7 keV to a dose of 5×10^{15} cm^{-2}. The samples were annealed in N$_2$ ambient at 750 °C for 120 sec.

Fig.4-10 shows the XRD rocking curves. It is observed that when the chuck temperature decreases from 5°C to -15°C, the C_{sub} only slightly increased from 1.027% to 1.046%. From the TEM image shown in Fig.4-4 and Fig.4-5, we can observe that the amorphous layer on the surface of 5°C carbon implanted sample and on the surface of -15°C carbon implanted sample are very similar. The amorphous layer thickness and level of amorphization does not have significant difference.

This phenomenon may be due to two reasons. The first one is that as the chuck temperature is 5°C, the Si surface after implantation process has been almost totally amorphized, so as the chuck temperature decreases to -15°C, the characteristic of surface amorphous layer would not change significantly. The second reason is that the 6-inch wafer wasn't directly contact to the chuck, but attached on a 12-inch holder during the implantation process. The mentioned temperature of either 5°C or -15°C are measured on the chuck, but after heat conduction through the holder, we could not control the temperature of the wafer surface precisely. The actual temperature difference on sample may be less than the difference on chuck in practical. So the surface amorphous layer created at 5°C and -15°C chuck temperatures are similar, and the C_{sub} after annealing are similar, too.

From the TEM image of 5 °C and -15 °C sample in Fig.4-4、Fig.4-5, we can confirm our explanation in the previous paragraph. The surface amorphous layer thickness is very similar with a value of 49 nm to 50 nm. Compare the roughness of boundary between amorphous layer and silicon substrate, we can find the boundary of -15 °C sample is smoother and clearer than 5 °C, that means the level of amorphous is higher. For that reason, the C_{sub} density of -15 °C sample after annealing is higher than 5 °C sample.

B. Effect of Annealing Condition

In this sub-section, the effect of annealing conditions including one-step annealing,

two-step annealing, and annealing temperature will be discussed.

B-1. First Step Annealing Temperature

The ion implantation condition used to study the effect of annealing temperature is chuck temperature 5 °C, implantation energy 7 keV, and implantation dose 5×10^{15} cm^{-2}. The samples were then annealed in N_2 ambient by RTA at 650 °C to 850 °C for 120 sec.

It has been listed in Table 4.1 that the R_s value decreases as the first step annealing temperature increases. The XRD rocking curves shown in Fig.4-11 indicate that the C_{sub} increases from 0.88% to 0.973% as the first step annealing temperature increases from 650°C to 700°C, and the stronger Si-C peak intensity on the 700°C sample indicates better crystalline quality. As the annealing temperature increases from 700°C to 750°C, the C_{sub} does not increase again but the Si-C peak intensity on the 750°C annealed sample is higher than that of the 700°C annealed sample. This result indicates that although the density of substitutional carbon does not increase but the crystalline quality can be improved as the annealing temperature increases to 750°C. When the annealing temperature further increases to 800°C, the Si-C peak nearly merges with the silicon reference peak. This means the density of substitutional carbon is very low. Increasing the annealing temperature to 850°C, the Si-C peak totally disappears, and the Si peak broadens. It means that there is nearly no substitutional carbon and the number of interstitial carbon increases dramatically.

During the thermal annealing process, the thermal energy provided by the annealing process affects the implanted carbons in two mechanisms [3]. The first one is to make the interstitial carbons incorporate into the substitutional site. The second one is to make the substitutional carbons diffuse into the interstitial site. When the annealing temperature is under 750°C, the first mechanism dominates in the process. For that reason, as temperature increased from 650°C to 750°C, the C_{sub} density increased and the crystalline quality became better. But after the temperature is increased to 800°C or higher, the second mechanism starts to dominate, although some of the interstitial carbons diffuse into the substitutional site, but more carbons are tend to diffuse into the interstitial site. That makes the C_{sub} density deceased as temperature increased to 800°C or higher, and the number of interstitial carbon increased at the same time. The highest solid state solubility of carbon in silicon is at the temperature of the melting point of silicon, which is $3.5 \pm 0.4 \times 10^{17}$ cm^{-3}, it is only about 7×10^{-4}% which is very low [6]. Most of the implanted carbons were on interstitial site before annealing. During the SPE annealing process, the carbons were driven into substitutional site and reach

supersatuation state by the thermal budget provided by annealing process. But if the thermal budget is too much, the sample will become thermal equilibrium again, the substitutional carbons in super-saturation state would driven to the interstitial site and the number of C_{sub} would decreased to solid solubility, which is a very small number.

In summary, at 650 °C to 750 °C, the C_{sub} increases as temperature increases and the crystalline quality will also be improved. As the annealing temperature increases to 800 °C or higher, the C_{sub} would decrease with the increase of temperature. Thus, 750 °C would be the most suitable first step annealing temperature within the implantation conditions studied in this chapter.

B-2. First Step Annealing Time

The carbon implantation condition used to study the effect of annealing time is chuck temperature -15 °C implantation energy at 7 keV, and implantation dose to 5×10^{15} cm^{-2}. The samples were annealed in N_2 ambient by RTA at 750 °C for 90 sec to 180 sec.

According to the experimental results listed in Table 4-2, the R_s value decreases as the first step annealing time increases. Fig.4-12 shows the XRD rocking curves, it reveals that for the 90 sec and 120 sec annealing times, the C_{sub} both about 1.04%. The Si-C peak intensity of the 120 sec sample is higher than that of the 90 sec sample. As the annealing time further increases to 150 sec, the C_{sub} does not increase, but slightly decreases to 1.01%. For the 180 sec sample, the C_{sub} further decreases to 0.992%.

The sheet resistance decreases as the annealing time increases because the higher thermal budget provided by the longer annealing time can activate more dopants and lower the sheet resistance. The C_{sub} are almost the same when the annealing time is 90sec and 120 sec. This implies that the solid-phase epitaxial growth has completed in 90 sec so that as the annealing time increases to 120 sec, the C_{sub} does not increases significantly. Additional thermal budget can repair residual defects produced by implantation process, so the crystalline quality can be further improved. When the annealing time increases to beyond 150 sec, the additional thermal budget cannot increase the C_{sub} but make some substitutional carbons diffuse into the interstitial site.

In summary, as the first step annealing temperature is 750 °C, the annealing for 90 sec to 120 sec can produce the highest C_{sub}. And the 120 sec annealing can make crystalline quality better. As annealing time exceeds 120 sec, the C_{sub} starts to decrease. According to these results, 120 sec is the best first step annealing time.

B-3. Second Step Annealing Condition

In order to further increase the C_{sub}, the feasibility of high temperature second step annealing is examined. In this experiment, carbon implantation was performed at chuck temperature -15°C and implantation energy 7 keV. The samples were annealed in N_2 ambient by RTA at 750 °C for 120 sec as the first step annealing. Two kinds of second step annealing were performed on different samples. The first one is annealed in the N_2 ambient by RTA at 1000°C for 1 sec in N_2 ambient. The second one is PLA at 350mj/cm^2 with 5 shots.

From the sheet resistance values listed in Table.4-2 and Table.4-3, after 1000 °C /1 sec second step annealing, the sheet resistance deceases significantly. In the case of using PLA for the second step annealing, the sheet resistance does not change by the 5 to 20 shots of PLA process. According to the XRD spectra shown in Fig.4-13, after the 1000°C /1sec second step annealing, the Si-C peak totally disappears, which indicates no substitutional carbon. Fig.4-14 shows the XRD rocking curves of the PLA sample with 5 shots of laser pulse. It is calculated that after PLA, the C_{sub} doesn't decrease but slightly increase from 1.046% to 1.091%.

The result can be explained by the following reason. By monitoring the temperature curve of 1000 °C /1 sec second step anneal, we find the sample was annealed at temperature higher than 900℃ for about 7 sec to 8 sec. Although the high temperature increases the carbon solid state solubility, the further thermal budget will drive the carbon atoms out of the substitutional sites. In the case of PLA, the laser pulse can melt the silicon surface. SiC formed in the SPE process will not melt due to its high melting point, and other carbons will incorporate into substitutional site to increase the C_{sub} density [7]. That's because the pulse duration is very short (25ns), after 5 shots of laser pulse, the effective annealing time is less than 125 ns, there's no further thermal budget to drive the substitutional carbon out of the substitutional site. In the research of K. Sekar et al., they find mili-second flash anneal can increase C_{sub} density, too [8]. So we speculate that the annealing time of second step anneal should not be longer than milli second.

In summary, suitable second step anneal can help to increase C_{sub}. But the annealing time should not be longer than milli-second. Otherwise, the further thermal energy will drive the carbon atoms out of the substitutional site. PLA or Flash annealing is the ideal choice for the second step annealing technique.

C. Comparison of Si-C Forming by PIII and Low Temperature Implantation

In this last subsection, we compare the Si-C formation results by the low temperature carbon implantation technique with the results by the CPIII technique. For the low temperature carbon implantation technique, the sample with chuck temperature at 5°C, carbon implantation energy 3 keV, and the dose to 5×10^{15} cm^{-2} is selected. For the CPIII technique, the sample with 3 keV/5 minutes CPIII process is selected. Both samples were annealed in N_2 ambient by RTA at 650 °C for 120 sec. we choose the annealing condition because in the previous chapter we find annealing temperature at 650 °C can create significant SiC peak in XRD, with temperature higher than 750 °C, the SiC peak disappear. So we choose 650 °C as annealing temperature in this comparison.

Fig.4-15 shows the XRD rocking curves, it is observed that the low temperature carbon implantation sample exhibits significantly larger difference in the positions of Si and Si-C peaks. . After calculation by the Kelires model, the C_{sub} of the low temperature carbon implantation sample is 0.654% and that of the CPIII sample is only 0.301%. The Si-C peak intensity of the low temperature carbon ion implantation sample is also higher than that of the CPIII sample.

These differences between the two ion implantation methods are related to the surface amorphous layer created during the implantation process. The CPIII technique uses CH_4 as the carbon ion source, it provides monomer carbon ion. The mass of the monomer carbon ion is light so it is not easy to produce good quality amorphous layer on the Si surface at room temperature or higher without high implantation dose. The low temperature carbon implantation technique uses low temperature chuck in the process, the low chuck temperature can reduce the self-annealing effect of silicon wafer and create better quality amorphous layer on the surface. Furthermore, the cleanliness of the low temperature ion implantation equipment is much better than the CPIII equipment. The low temperature implanter is a production tool for 12" process and is installed in cleanroom while the CPIII equipment is an academic tool and is installed in general laboratory. The other species except C and H may be also implanted into the Si substrate and will deteriorate the re-crystallization of the amorphous layer. Therefore, the low temperature ion implantation technique can result in higher atomic percentage of the substitutional carbon.

4.5 Conclusions

Low temperature carbon ion implantation can create good quality amorphous layer on the surface with low energy. From the TEM image we can find carbon implantation at 7 keV

with a dose of 5×10^{15} cm^{-2} and chuck temperature at -15 °C can create about 49nm thick high quality amorphous layer. After annealing at 750 °C for 120 sec, we find the phosphorous will diffuse out from the carbon-rich region and the phosphorous profile will be shallower compare to as-implanted sample. That's because the Si_i in the carbon-rich region will diffuse to the shallower or deeper region of silicon substrate. The Si_i diffuse to the deeper region will be trap by Si-C clusters and reduce the interstitial-assisted diffusion, and the Si_i diffuse to the shallower region will make phosphorous diffuse with it and make the profile shallower. As low temperature carbon implantation applied to phosphorous doped NiSi/Si structure, we find it could not improve NiSi thermal stability, that's because phosphorous atom will change the interfacial energy between nickel silicide and silicon. As low temperature carbon implantation applied to Si-C forming, we find as the implant energy is under 7keV, C_{sub} density will increase as energy increase, that's because higher energy can produce thicker amorphous layer with higher quality. The surface is near totally amorphous when implant energy is 7keV, so higher energy could not make significant C_{sub} density difference. As carbon dose increased from 5×10^{15} cm^{-2} to 8×10^{15} cm^{-2}, the C_{sub} density did not increase significantly, that's because the surface is totally amorphous when dose is 5×10^{15} cm^{-2}, so higher dose won't make significant difference on surface amorphous layer. The solid state solubility of carbon in silicon is very low even under supersatuation state, most of the implanted carbon is interstitial, too much carbon dose could not increase C_{sub} density effectively but will increase the number of interstitial carbon and make the crystalline quality worse. Annealing at 750°C for 120 sec was found to be the best first step annealing condition in our experiment, more thermal budget will make the silicon substrate back to thermal equilibrium and decrease the C_{sub} density. Second step annealing temperature should be higher than first step to increase the C_{sub} density in super-satuation state, and the duration time should be less than 1sec. If the duration time is too long, too much thermal budget will decrease the C_{sub} density. PLA for 5 shots at energy 350mj/cm^2 can increase C_{sub} density from 1.046% to 1.091%, it indicates that PLA is a promising process to perform second step Si-C formation annealing. Finally, we find low temperature carbon ion implantation can produce higher C_{sub} density after Si-C formation compare to CPIII, that's because low temperature carbon ion implantation can produce thicker surface amorphous layer with high quality.

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Table 4-1.　The sheet resistance value of carbon implanted silicon substrate after Si-C formation（Ⅰ）

	650°C 120secs	700°C 120secs	750°C 120secs	800°C 120secs	850°C 120secs
3keV (5°C) 5×10^{15} cm^{-2}	139.5	134.7			
5keV (5°C) 5×10^{15} cm^{-2}	185.5	177.9			
7keV (5°C) 5×10^{15} cm^{-2}	292	270.5	258	238	173
7keV(-15°C) 5×10^{15} cm^{-2}			255		
7keV(-15°C) 8×10^{15} cm^{-2}			391		
9keV(-15°C) 5×10^{15} cm^{-2}			327		

Table 4-2.　The sheet resistance value of carbon implanted silicon substrate after Si-C formation（Ⅱ）

	750°C 90secs	750°C 120secs	750°C 150secs	750°C 180secs	750°C 120secs + 1000°C 1secs
7keV(-15°C) 5×10^{15} cm^{-2}	267	255	247	241	125
7keV(-15°C) 8×10^{15} cm^{-2}		391			213
9keV(-15°C) 5×10^{15} cm^{-2}		327			132

Table 4-3. The sheet resistance value of carbon implanted silicon substrate after Si-C formation (Ⅲ)

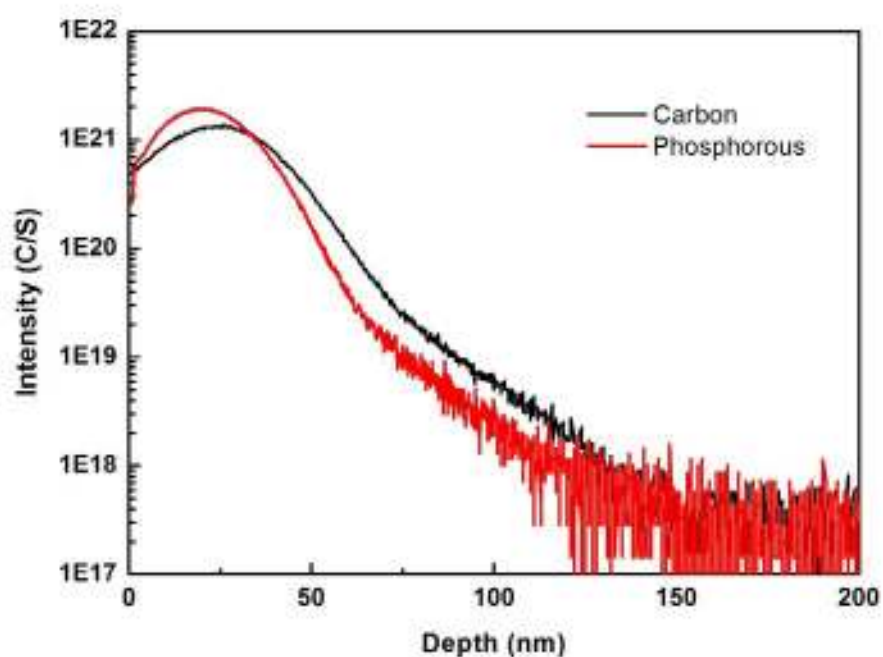|	750°C 120secs	750°C 120secs + 350mj 5shots	750°C 120secs + 350mj 10shots	750°C 120secs + 350mj 15shots	750°C 120secs + 350mj 20shots
7keV(-15°C) 5×10^{15} cm^{-2}	255	254	248	244	242

Fig.4-1   SIMS depth profile after 7keV/-15°C /5×10^{15} cm^{-2} low temperature carbon   ion implantation (as-implanted)
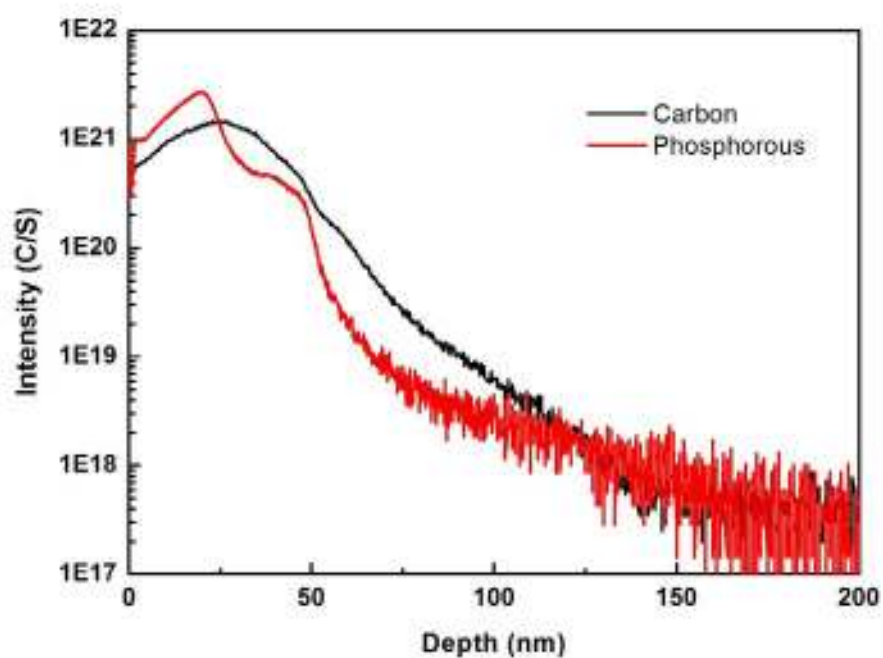

Fig.4-2   SIMS depth profile after 7keV/-15°C /5×10^{15} cm^{-2} low temperature carbon ion implantation (750°C /120secs annealed).
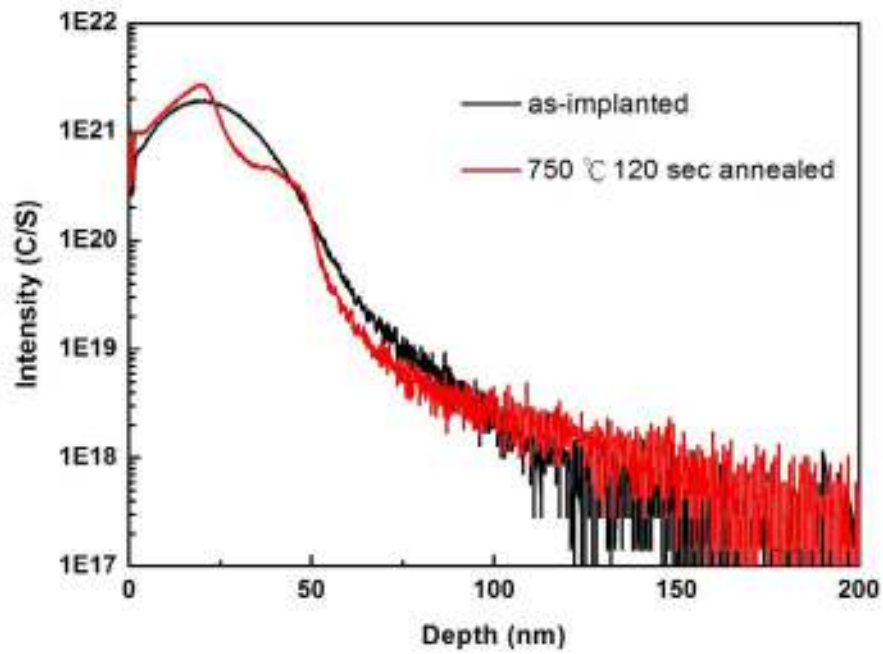
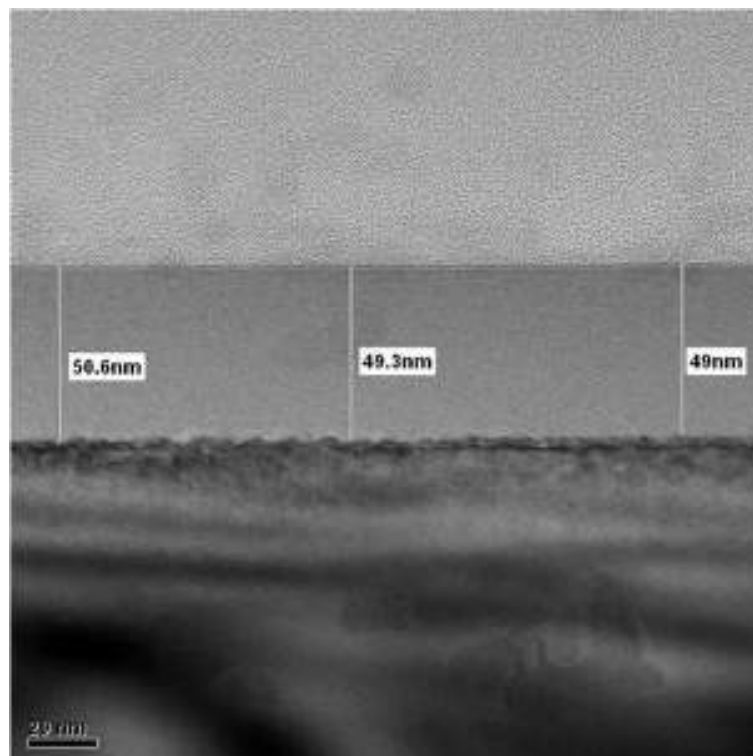Fig.4-3   SIMS depth profile of phosphorous before and after 750°C /120secs annealing

Fig.4-4   The TEM image of 7keV/5×10^{15} cm^{-2} low temperature (5°C) carbon implanted sample.

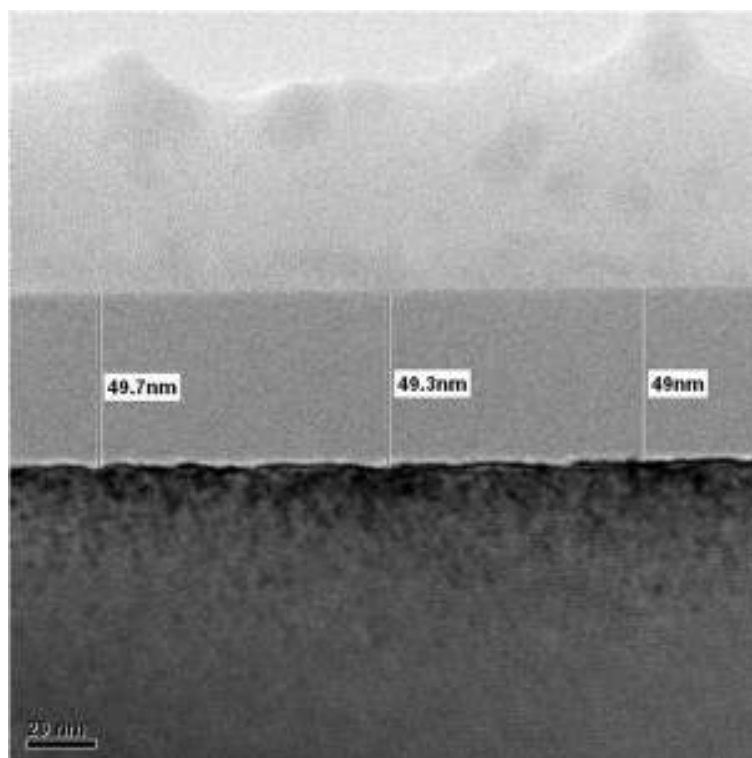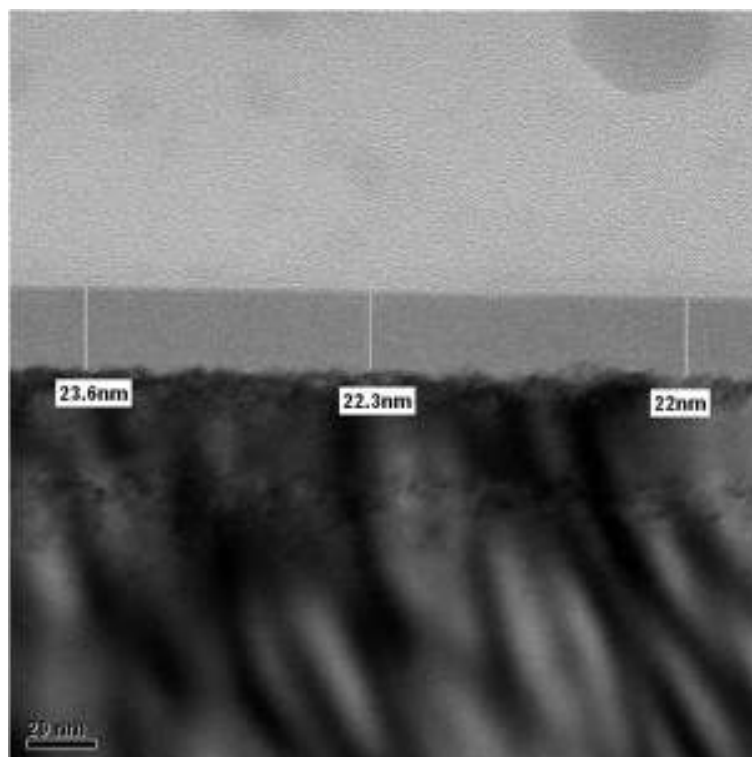Fig.4-5   The TEM image of 7keV/5×10^{15} cm^{-2} low temperature (-15°C) carbon implanted
sample

Fig.4-6   The TEM image of 7keV/5×10^{15} cm^{-2} low temperature (-15°C) carbon implanted
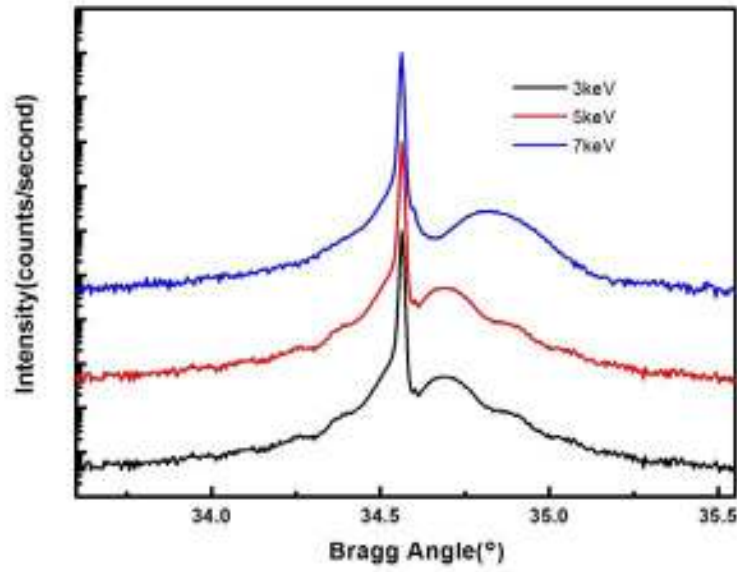sample after annealing at 750℃ for 120 sec

Fig.4-7   The XRD rocking curve patterns of low temperature carbon implant samples, with 5°C chuck temperature at a dose of 5×10^{15} cm^{-2} . The implant energy ranged from 3keV to 7keV. The samples were annealed with temperature 700°C for 120secs.
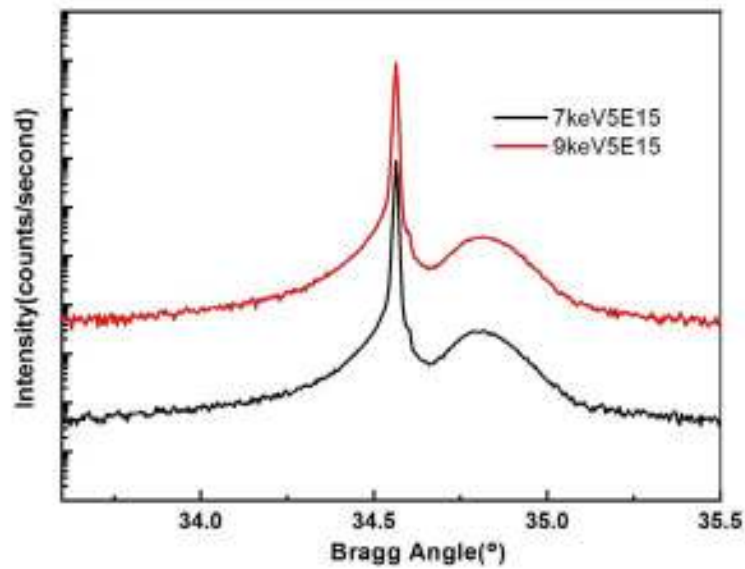

Fig.4-8   The XRD rocking curve patterns of low temperature carbon implant samples, with -15°C chuck temperature at a dose of 5×10^{15} cm^{-2} . The implant energy ranged from 7keV to 9keV. The samples were annealed with temperature 750°C for 120secs.
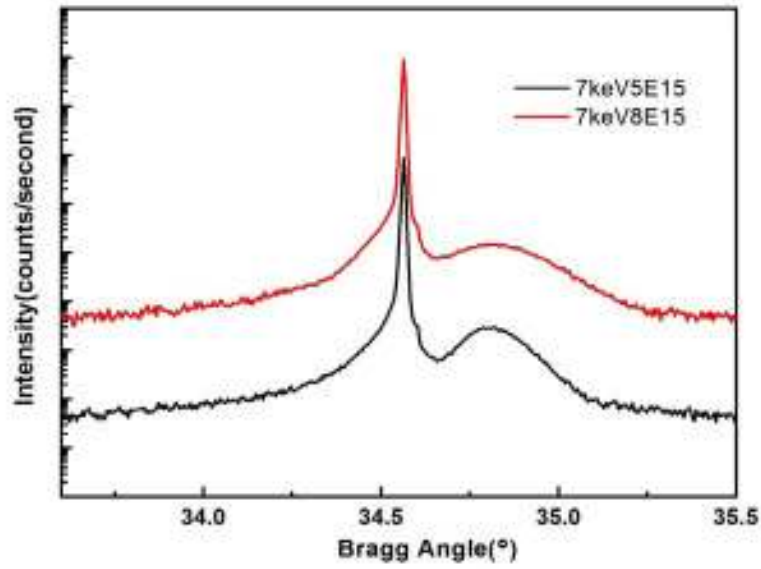
Fig.4-9   The XRD rocking curve patterns of low temperature carbon implant samples, with -15°C chuck temperature and 7keV implant energy. The dose was 5×10^{15} cm^{-2} and 8×10^{15} cm^{-2}. The samples were annealed with temperature 750°C for 120secs.

Fig.4-10   The XRD rocking curve patterns of low temperature carbon implant samples, with 7keV implant energy at a dose of 5×10^{15} cm^{-2}. Chuck temperature is 5°C and -15°C.The samples were annealed with temperature 750°C for 120secs.

Fig.4-11   The XRD rocking curve patterns of low temperature carbon implant samples, with 7keV implant energy at a dose of 5×10^{15} cm^{-2}. Chuck temperature is 5°C. The samples were annealed with temperature 650°C to 850°C for 120secs.
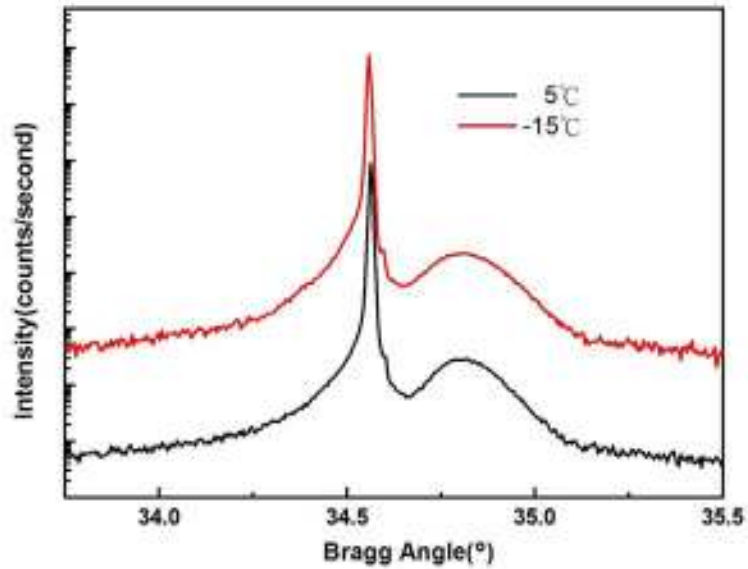

Fig.4-12   The XRD rocking curve patterns of low temperature carbon implant samples, with 7keV implant energy at a dose of 5×10^{15} cm^{-2}. Chuck temperature is -15°C. The samples were annealed with temperature 750°C for 90secs to 180secs.
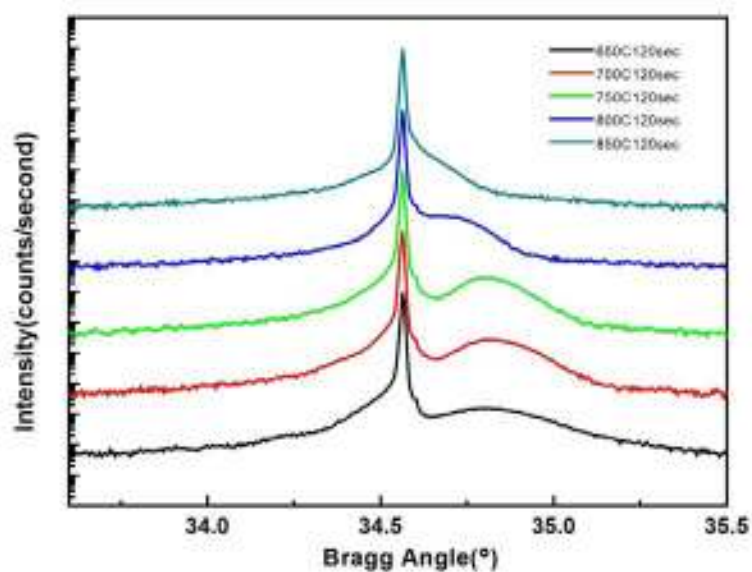
Fig.4-13   The XRD rocking curve patterns of low temperature carbon implant samples, with 7keV implant energy at a dose of 5×10^{15} cm^{-2}. Chuck temperature was 5°C. The samples were annealed with first step temperature annealing 750°C for 120secs, and one of the sample were performed 1000°C second step annealing for 1 second.
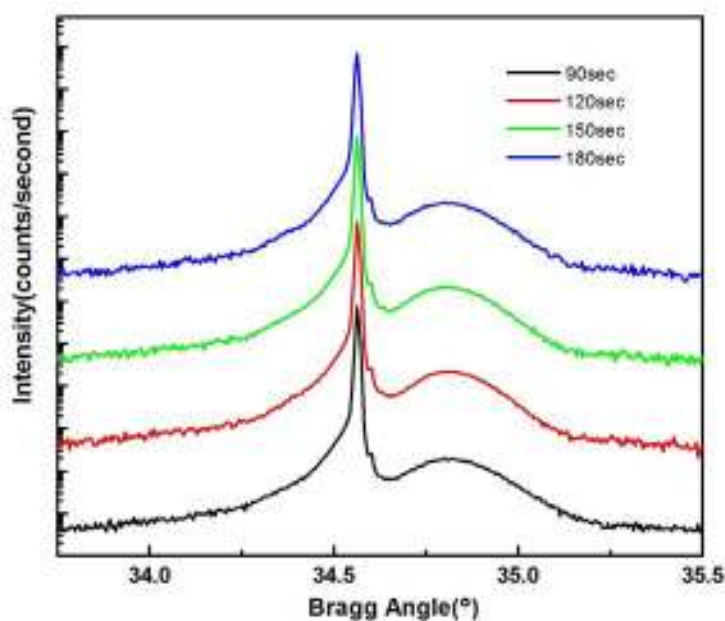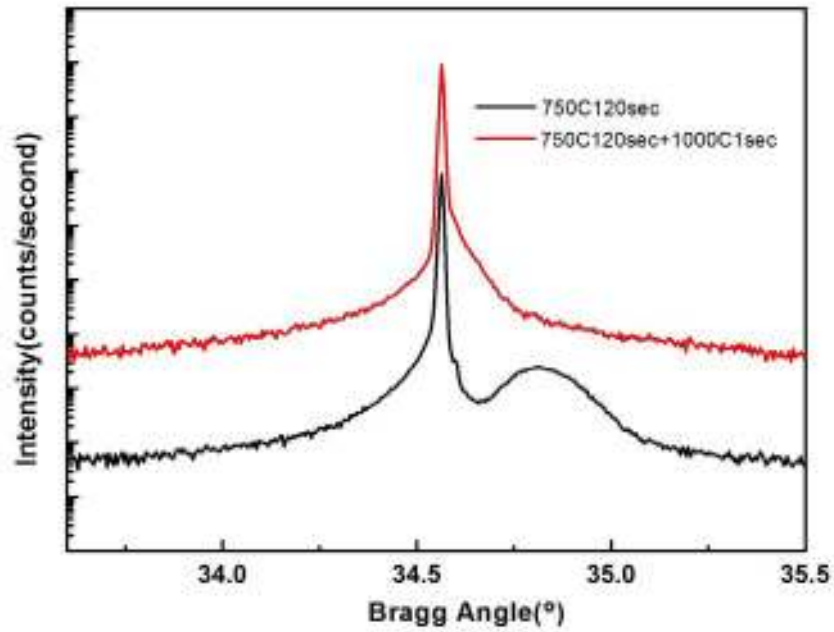
Fig.4-14　The XRD rocking curve patterns of low temperature carbon implant samples, with 7keV implant energy at a dose of 5×10^{15} cm^{-2}. Chuck temperature was 5°C. The samples were annealed with first step temperature annealing 750°C for 120secs, and one of the sample were performed PLA second step anneal at energy 350mj/cm^2, number of shots is 5.
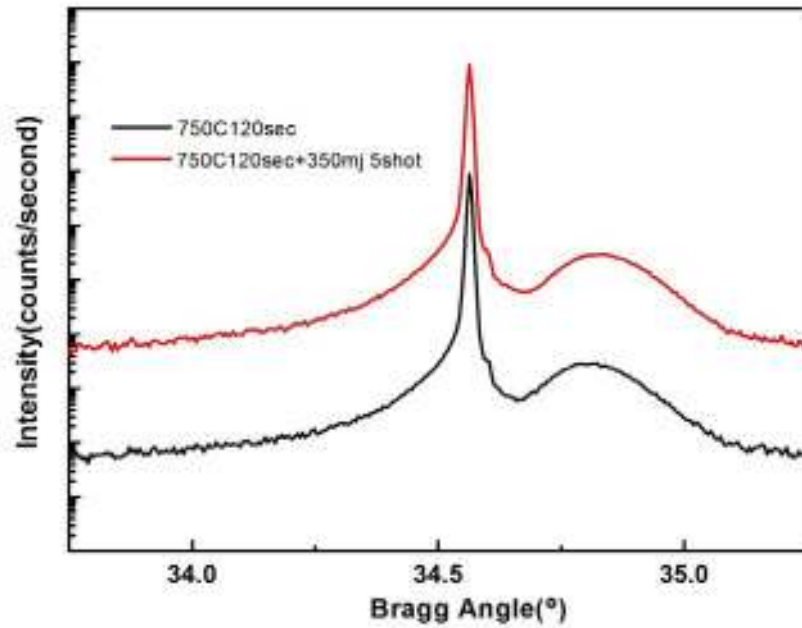
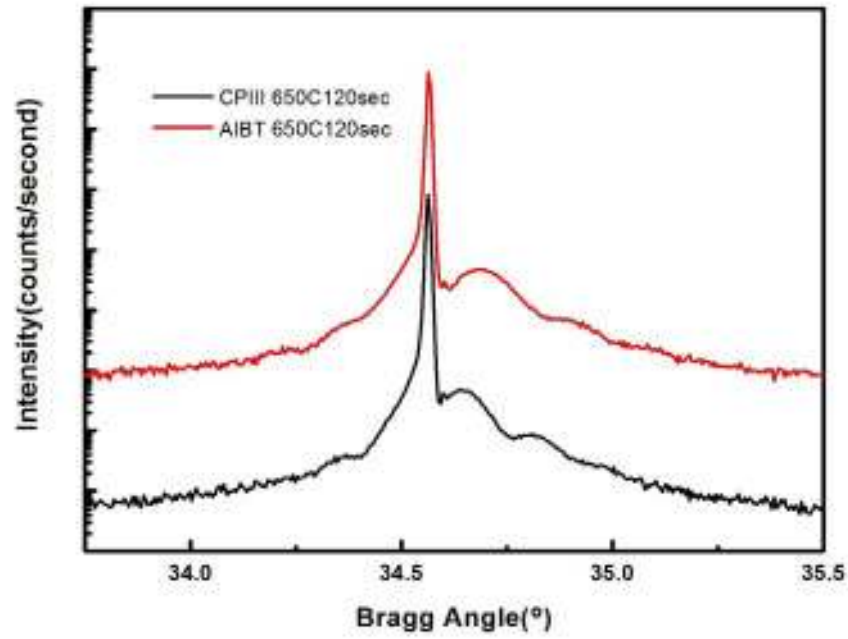Fig.4-15   The XRD rocking curve patterns of low temperature carbon implant sample
(3keV/5×10^{15} cm^{-2}/5°C) and CPIII sample (3keV/5min). The samples were
annealed with temperature 650°C for 120secs.

Chapter 5

Gate-All-Around Poly-Si Nano Wire Thin-Film Transistor

5.1 Introduction

Polycrystalline-silicon thin film transistors (poly-Si TFTs) have been studied for several decades. In the past, large-grain poly-Si TFTs are extensively researched by different recrystallization technologies including excimer laser annealing (ELA) [1-2] and metal induced lateral crystallization (MILC) [3-4] instead of conventional solid phase crystallization (SPC) [5]. Large-grain poly-Si TFTs with low grain boundary defects can enhance the carrier mobility and suppress leakage current. Furthermore, it is well known that the NH3 plasma treatment process is able to reduce grain boundary defects, and effectively improve the device characteristics of poly-Si TFTs [6].

Recently, various nano wire (NW) poly-Si TFTs with different multi-gate structures were proposed by many researchers [7-10]. The main advantage of these device structures is suppressing the short channel effect (SCE) by increasing the control ability of the gate electrode. However, the physical gate length (LG) of most of the published TFTs is not short (LG $\geqq$ 1 μm). Moreover, it has been suggested that poly-Si TFTs could be applied in the three-dimensional integrated circuit (3D-IC) technology to relax the scaling down issues [11], so the physical gate length scaling of poly-Si TFTs should be achieved simultaneously for high layout efficiency as logic devices. Therefore, the device characteristics of NW poly-Si TFTs with ultra short gate length must be investigated.

Although the NW poly-Si TFT with L_G = 20 nm and omega-shaped gate electrode has been reported, their transfer characteristics shows poor switch performance [7]. In this chapter, we successfully fabricated the smallest gate-all-around (GAA) NW poly-Si TFT with recorded physical gate length of 30 nm for the first time. Excellent electrical characteristics after NH_3 plasma treatment are obtained. These results indicate the possibility of applying the GAA NW poly-Si TFTs in 3D-IC technology.

5.2 Experiments

Fig.5-1 shows the main fabrication process and the schematic diagram of the GAA poly-Si NW TFT integrated with the modified Schottky barrier (MSB) source/drain (S/D) [12]. The detail process flow is described below. First, a 150-nm-thick SiO_2 was thermally

grown on a p-type Si substrate. Then, an 18-nm-thick amorphous Si film was deposited by a low pressure chemical vapor deposition (LPCVD) system as the channel layer. The amorphous Si film was recrystallized to poly-Si film during a SPC annealing at 600 ^{o}C for 24 hr. The active region of poly-Si NW was defined by electron beam lithography (EBL) and reactive ion etching (RIE). The narrowest poly-Si NW width (W_{NW}) is 35 nm as shown in Fig. 5-2(a). The average grain size of the poly-Si channel inspected by plan-view transmission electron microscope (TEM) is about 55 nm as shown the inset in Fig. 5-2(a).

A simple process was used to fabricate the GAA structure. The wet oxide, whose length, width, and depth is 1 μm, 1μm, and 70 nm, under the poly-Si NW was removed by EBL and wet etching. Hence, the poly-Si NW was suspended from the wet oxide. Next, after the standard RCA cleaning process, a 25-nm-thick tetra-ethoxy-silane (TEOS) gate oxide and a 200-nm-thick in-situ phosphorus-doped poly-Si gate were sequentially deposited followed by a rapid thermal annealing (RTA) at 1000 ^{o}C for 10 sec. Fig. 5-2(a) shows that the poly-Si NW channel was completely surrounded by TEOS gate oxide and poly-Si gate, and the darker area under the poly-Si NW contains grains of poly-Si gate with different orientations. The final poly-Si active layer thickness (T_{Si}) was reduced to 8 nm owing to the several cleaning steps. The cross-sectional area of the narrowest NW is 35 nm x 8 nm. After poly-Si gate patterning, a 20-nm-thick TEOS SiO_2 and a 20-nm-thick Si_3N_4 were deposited and etched to form a double spacer. To reduce the serious series resistance of the poly-Si NW's S/D region, the low-temperature process of MSB Ni-silicide S/D was used for our GAA NW poly-Si TFTs. After removing the remnant TEOS SiO_2 and/or native SiO_2 on S/D and gate regions by dilute HF (DHF) solutions, the composite Ni(6 nm)/TiN(10 nm) films was continuously deposited by a physical vapor deposition (PVD) system. The two-step silicidation process was employed to form Ni-silicide [12]. Phosphorus ions were implanted into Ni-silicide at 10 keV with a dose of 5×10^{15} cm^{-2}, then a furnace annealing at 600 ^{o}C for 30 min was performed to form N^{+} S/D extension. After recording the fresh current-voltage characteristics, a NH$_3$ plasma treatment at 300 ^{o}C for 5 min was performed to passivate the grain boundary defects. Fig. 5-2(b) displays the cross-sectional TEM micrograph along the channel direction. The shortest physical gate length is 30 nm. The plan-view channel area of the smallest GAA NW poly-Si TFT is smaller than the average poly-Si grain size, so there are few grain boundaries in the ultra scaling channel region. Therefore, the smallest GAA NW poly-Si TFT with NH$_3$ plasma treatment can be considered as the single-crystal-like logic device.

5.3 Results and Discussion

The cross-sectional TEM images of the device with L_G/W_{SN}= 30 nm/35 nm are shown in Fig.5-2(a) and 5-2(b). The poly-Si thickness (T_{SN}) has been reduced to 8 nm during the sequential cleaning processes. This structure can be treated as a planar fin structure. Figures 5-3 and 5-4 show the transfer characteristics and output characteristics of the device with L_G/W_{SN}= 30 nm/35 nm, respectively. Due to the GAA fin structure, the short channel effect can be well controlled. The mobility after correcting S/D resistance is about 25 cm^2/V-s, which is higher than most of the TFTs fabricated by SPC technique. The driving current (I_{ON}) exceeds 100 $\mu A/\mu m$ at V_G=10V and V_D=1V, which is also higher than most of the published results. The I_{ON}/I_{OFF} ratio is higher than 10^5.

Figure 5-5 ~ Figure 5-7 show the average values of threshold voltage (VTH), drain-induced-barrier-lowering (DIBL), and I_{ON} of the devices with fixed W_{SN}= 35 nm and various LG, respectively. The V_{TH} is defined as the V_G at which I_D= W_{EFF}/L_Gx10nA, where W_{EFF}= 2x(W_{SN}+ T_{SN}). Each average value is calculated from fifteen devices with the same dimension. No VTH roll-off phenomenon occurs. The V_{TH} even increases while L_G is equal to or smaller than 80 nm. The average DIBL value as L_G= 30 nm is only 69 % larger than that as L_G= 200 nm. The I_{ON} saturates as L_G is equal to or smaller than 80 nm owing to S/D series resistance. The average I_{ON} as L_G= 30 nm is 106 $\mu A/\mu m$ while the highest I_{ON} is 129 $\mu A/\mu m$.

Figure 5-8 ~ Figure 5-10 show the average values of V_{TH}, DIBL, and I_{ON} of the devices with fixed L_G= 30nm and various W_{SN}, respectively. The V_{TH} value depends on the volume and defect density of the NW. Hence, the narrower W_{SN} results in the lower V_{TH} value. Besides, gate stacks can tightly control the channel potential via narrower W_{SN} so that the DIBL values decrease with WSN. The ION continuously increases with the decrease of W_{SN} because the volume inversion increases the electron mobility although narrower W_{SN} has larger S/D resistance.

After employing a NH_3 plasma treatment process to passivate the grain boundary defects of the poly-Si NW channel and poly-Si gate/TEOS gate oxide interface states, the transfer characteristics of the NH_3-passivated GAA NW poly-Si TFT are drastically improved and has excellent performance compared to that of the non-NH_3-passivated GAA NW poly-Si TFT as shown in Fig.5-11. The V_{TH}, S.S., and DIBL values decrease to 0.97 V, 224 mV/Dec., and 0.895 V/V, respectively. Before the NH_3 plasma treatment process, grain boundary barriers close to the drain electrode can be reduced more effectively as V_{DS} increases. Therefore, the DIBL effect is apparent. After the NH_3 plasma treatment process, the grain boundary barriers are lowered. The transport of electrons becomes dominated by the source-to-channel barrier, and the drain electric field has less influence on the source-to-channel barrier lowering owing

to the GAA structure. Therefore, the DIBL effect can be improved. The I_{ON}/I_{OFF} current ratio is raised to 5×10^7 at $V_{DS} = 1V$. We believed that the V_{TH}, S.S., DIBL, and I_{ON} values could be further improved by scaling equivalent oxide thickness (EOT) to get better gate controllability.

Figure 5-12 shows the typical output characteristics of the NH_3-passivated GAA NW poly-Si TFT with $L_G = 30$ nm, $W_{NW} = 35$ nm, and $T_{Si} = 8$ nm. The key parameters of our GAA NW poly-Si TFT and some state-of-the-art TFTs [7-10] are summarized in the table inserted in Fig. 4. The linear relationship between I_{DS} and V_{DS} when the NH_3-passivated GAA NW poly-Si TFT is biased in the linear region indicates that the MSB S/D has been successfully fabricated. The normalized driving current (I_{DS}/W_{EFF}) at $V_{GS}-V_{TH} = 5$ V and V_{DS} = 1 V is 187 µA/µm ($W_{EFF} = 2$ x ($W_{NW} + T_{Si}$)). If normalized to the drawn channel width, the driving current can be as high as 459 µA/µm. As we compared our device characteristics with state-of-the-art TFTs listed in references [7-10], our device shows the best driving current value due to the ultra short L_G and fully silicided S/D.

The gate dopant activation process at 1000 ^{o}C for 10 sec can be replaced by 600 ^{o}C for 12 hr to avoid thermal budget issue in the 3D-IC application. We consider the device can still be retained because the rather thick EOT of the GAA NW poly-Si TFTs.

5.4 Conclusions

The record smallest poly-Si NW TFT with GAA structure is demonstrated for the first time. The tight GAA and NW structure enhances the gate potential controllability effectively. Therefore, excellent short channel and narrow width behaviors can be obtained. It is demonstrated that the V_{TH}, DIBL, and I_{ON} can be further improved by scaling the gate oxide thickness and by NH_3 plasma treatment for defects passivation. These results reveal the possibility of 3D ICs.

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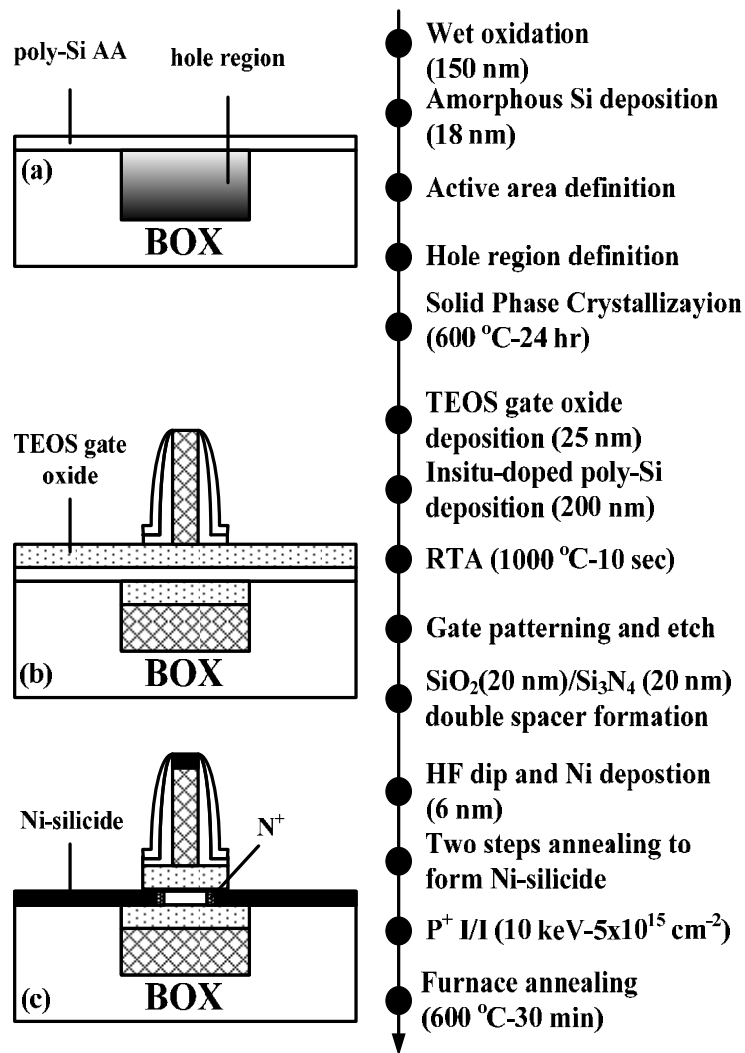
poly-Si AA   hole region

(a)

BOX

Wet oxidation
(150 nm)

Amorphous Si deposition
(18 nm)

Active area definition

Hole region definition

Solid Phase Crystallizayion
($600\,^{o}C$-24 hr)

TEOS gate
oxide

(b)   BOX

TEOS gate oxide
deposition (25 nm)

Insitu-doped poly-Si
deposition (200 nm)

RTA ($1000\,^{o}C$-10 sec)

Gate patterning and etch

SiO_2(20 nm)/Si_3N_4 (20 nm)
double spacer formation

Ni-silicide N^+

(c)   BOX

HF dip and Ni depostion
(6 nm)

Two steps annealing to
form Ni-silicide

P^+ I/I (10 keV-$5x10^{15}$ cm^{-2})

Furnace annealing
($600\,^{o}C$-30 min)

Fig.5-1. Process flow and schematic structure of   the GAA poly-Si NW TFT: (a) after active layer and hole region definition, (b) after gate oxide/n^+-poly gate continuously deposition and composite spacer formation, (c) after modified Schottky barrier S/D formation.
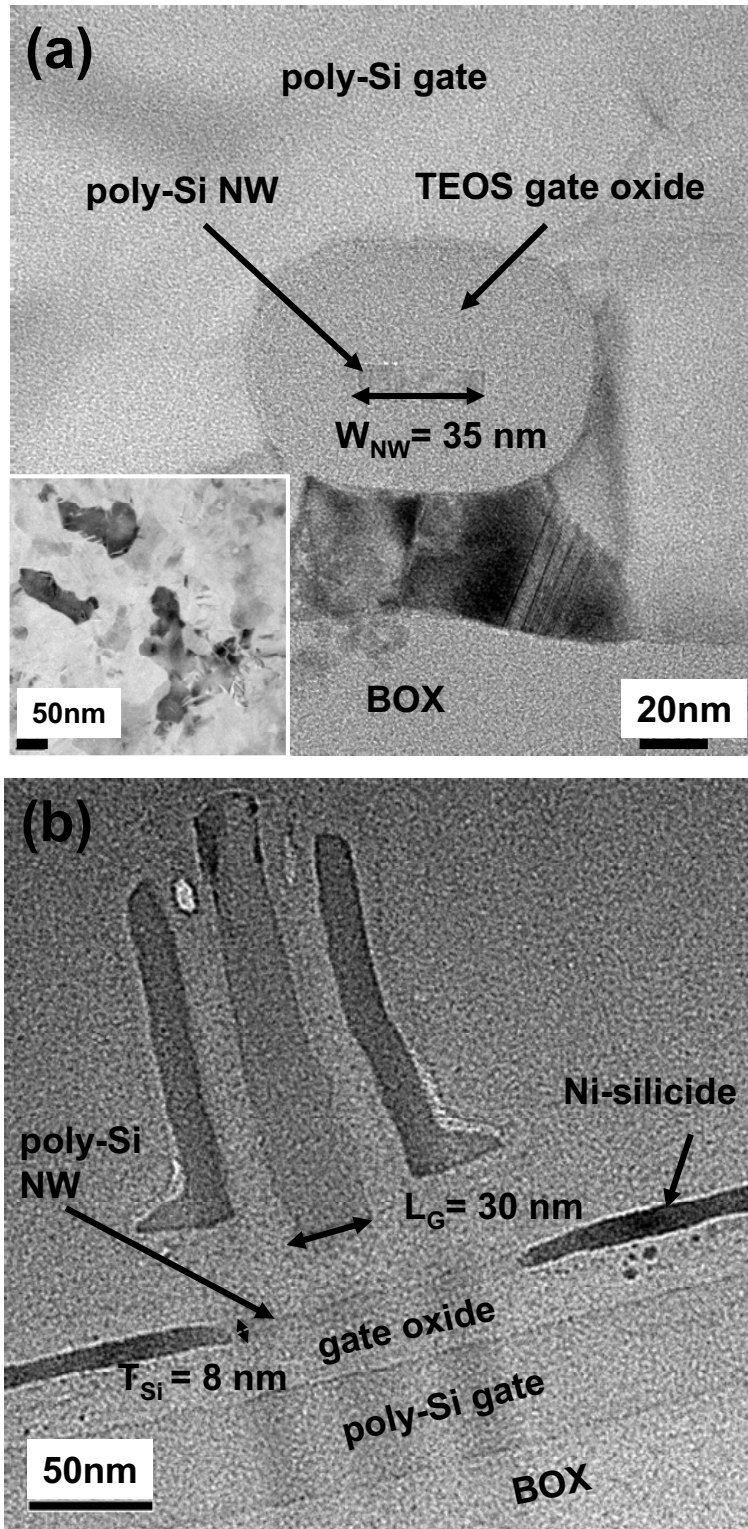
Fig.5-2. (a) Cross-sectional TEM image of the GAA NW poly-Si TFT along gate direction with L_G/W_{SN} = 200 nm/35 nm. The inset displays the plan-view TEM image of the 8-nm-thick poly-Si channel. (b) Cross-sectional TEM image of the GAA NW poly-Si TFT along channel direction with L_G/W_{SN} = 30 nm/35 nm.

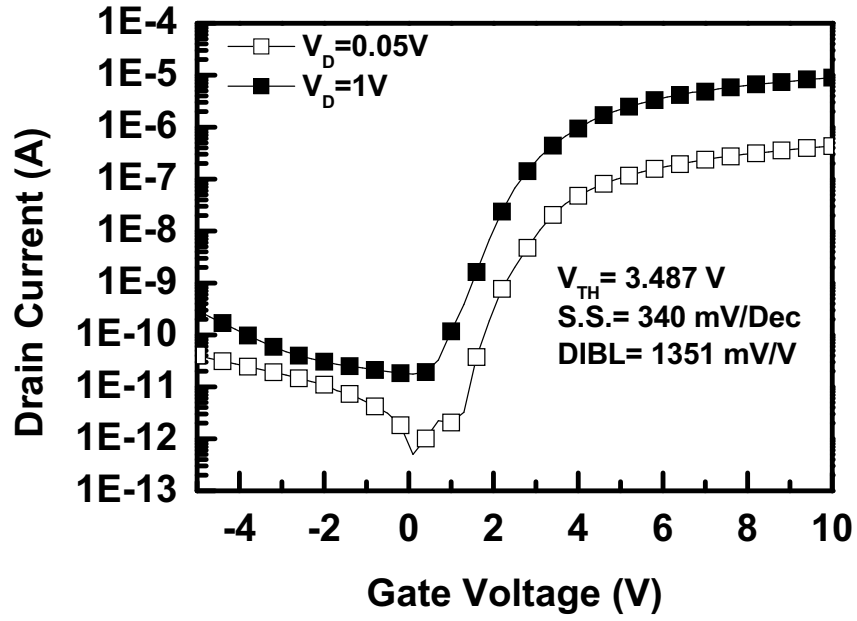Fig.5-3. Typical transfer chrarcteristics of the GAA poly-Si NW TFT with L_G/W_{SN}= 30 nm/35 nm.
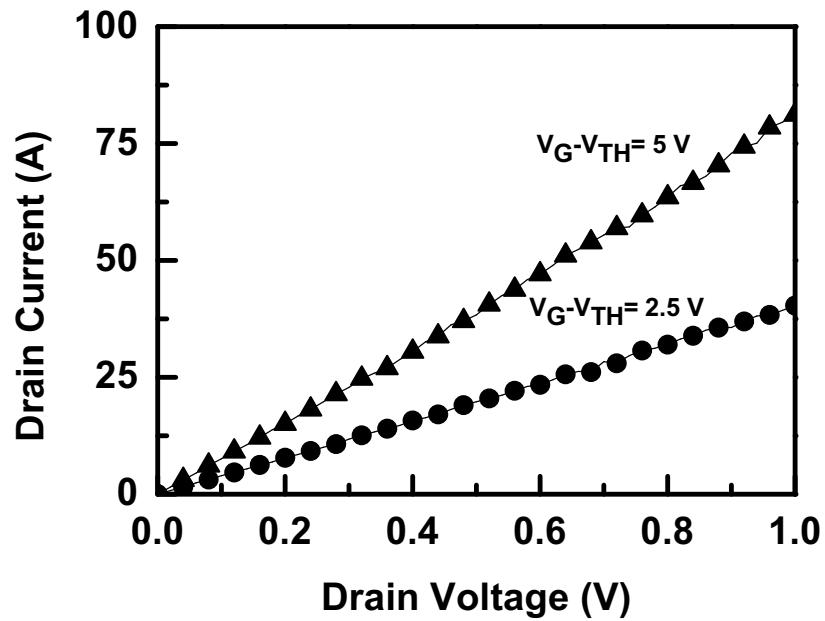

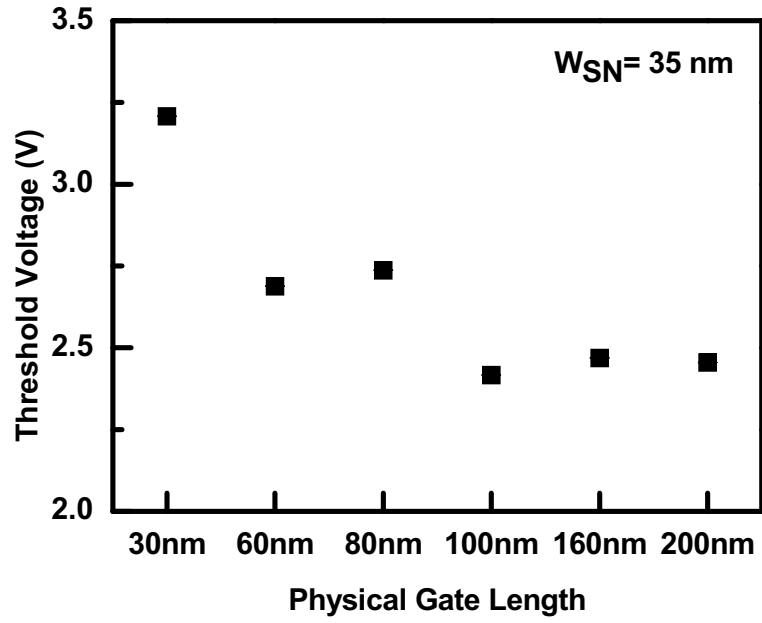Fig.5-4. Typical output chrarcteristics of the GAA poly-Si NW TFT with L_G/W_{SN}= 30 nm/35 nm.

Fig.5-5. Average values of V_{TH} of the devices with fixed $W_{SN}= 35$ nm and various L_G.

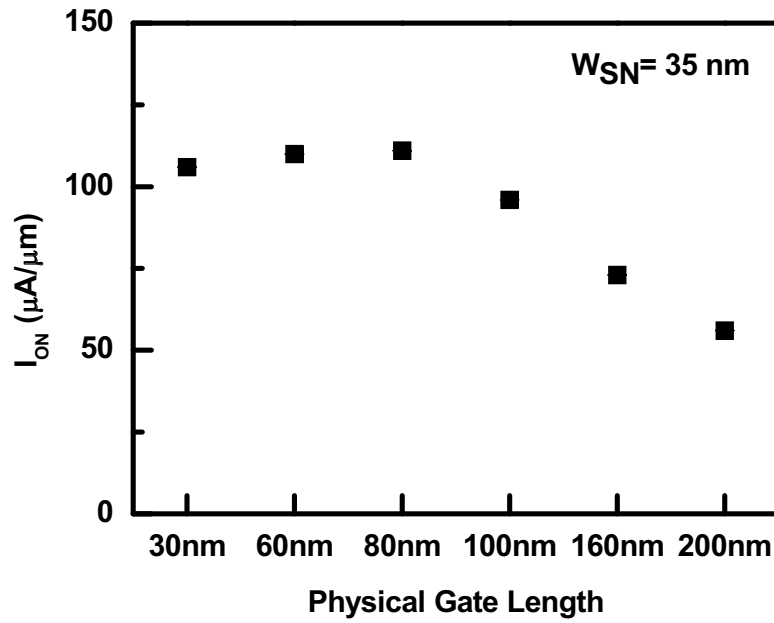
Fig.5-6. Average values of I_{ON} of the devices with fixed $W_{SN}= 35$ nm and various L_G.
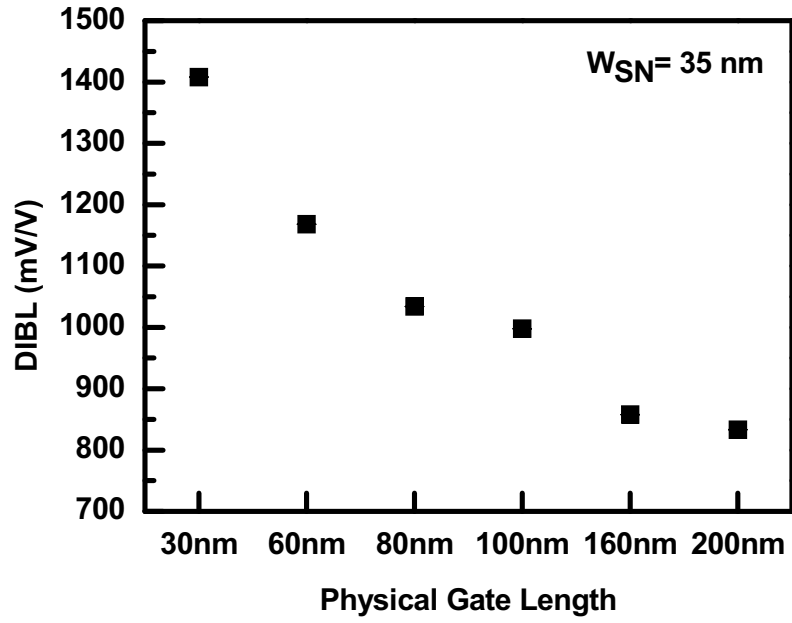
Fig.5-7. Average values of DIBL of the devices with fixed W_{SN}= 35 nm and various L_G.
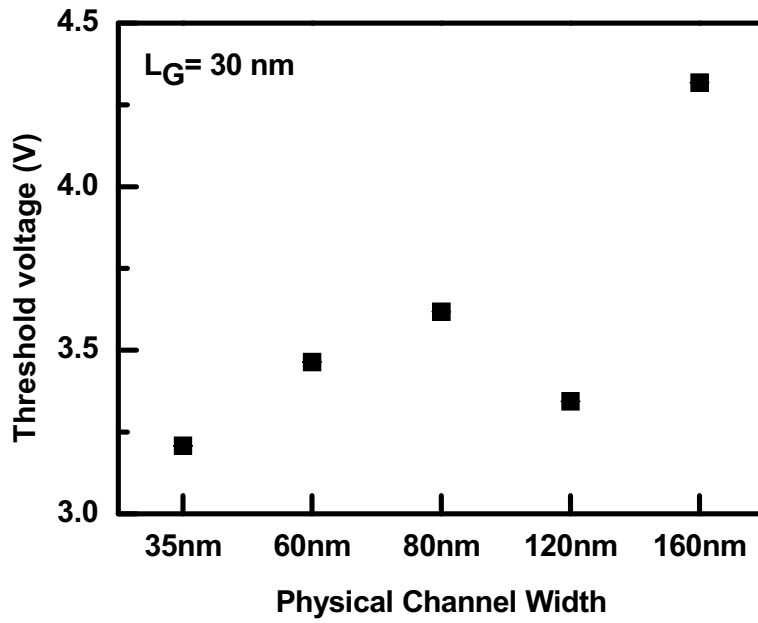

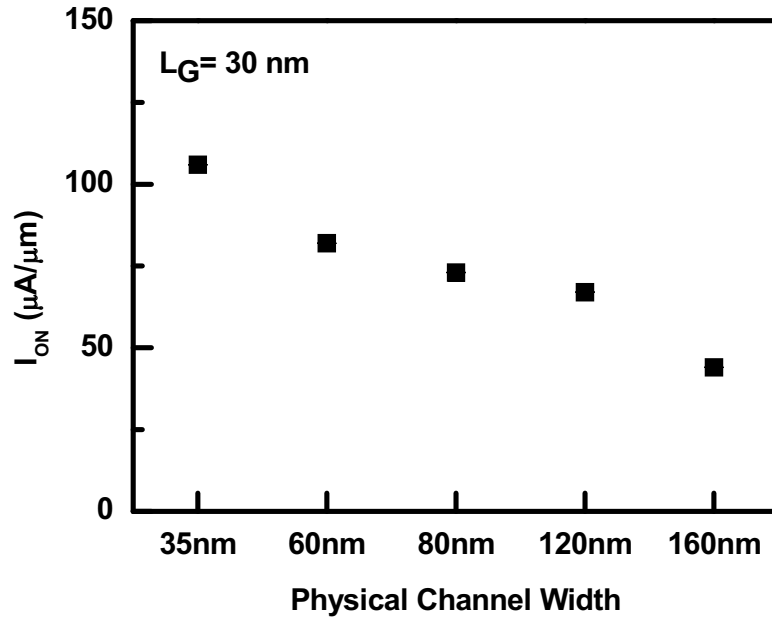Fig.5-8. Average values of V_{TH} of the devices with fixed L_G= 30 nm and various W_{SN}.

Fig.5-9. Average values of I_{ON} of the devices with fixed $L_G= 30$ nm and various W_{SN}.
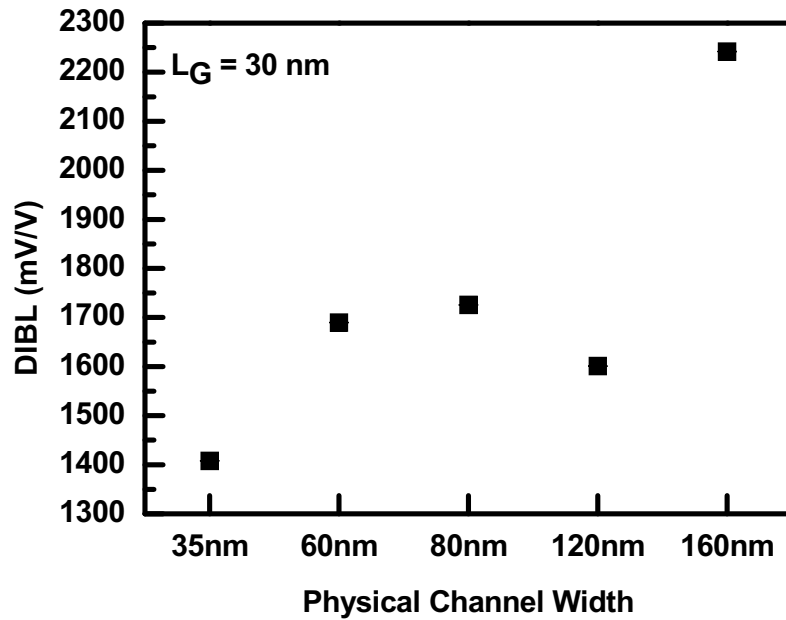
Fig.5-10. Average values of DIBL of the devices with fixed $L_G= 30$ nm and various W_{SN}.
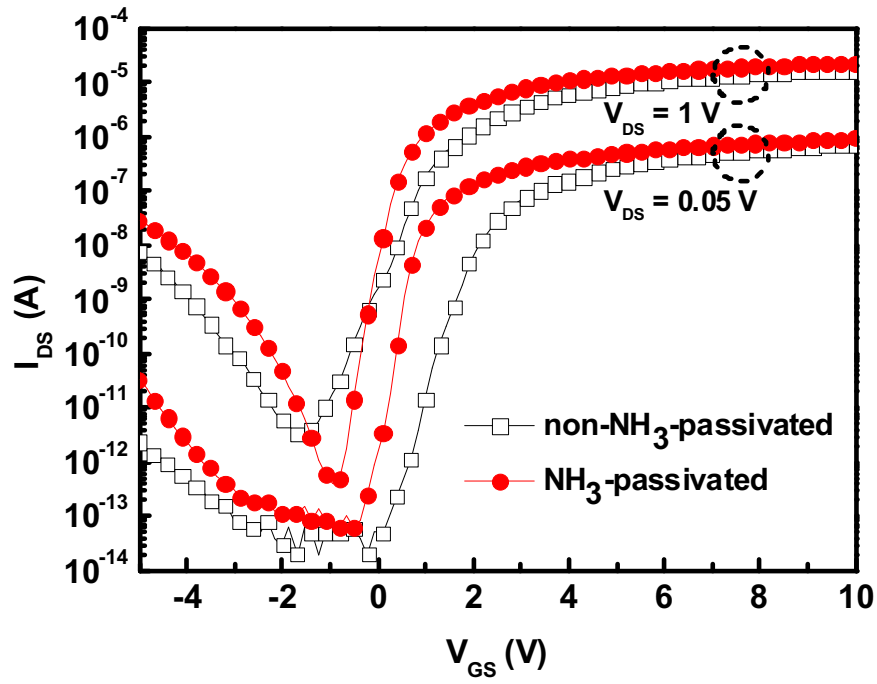
Fig.5-11. Transfer characteristics of the non-NH₃-passivated and NH₃-passivated GAA NW poly-Si TFT with L_G = 30 nm, W_{NW} = 35 nm, and T_{Si} = 8 nm, respectively.

Key parameters	This work	[7]	[8]	[9]	[10]
L_G (µm)	0.03	0.1	0.4	1	2
V_{TH} (V)	0.97	NA	-0.7	1.41	-0.38
S.S. (mV/Dec.)	224	79	100	360	114
DIBL (mV/V)	895	78	10	60	13
I_{ON} (µA/µm)	187	40	145	26	68

Fig.5-12. Output characteristics of the NH₃-passivated GAA NW poly-Si TFT with L_G = 30 nm, W_{NW} = 35 nm, and T_{Si} = 8 nm, respectively. The inset table compares the key parameters of our GAA NW poly-Si TFT with that of references [7-10].

Chapter 6

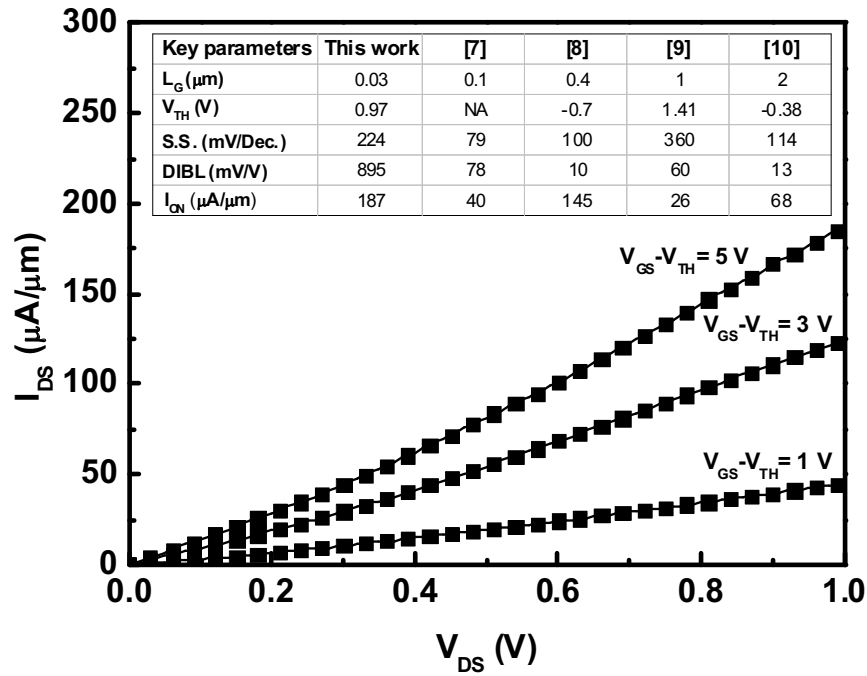# High Performance Poly-Si Nano Wire Thin Film Transistors using the HfO$_2$ Gate Dielectric

6.1 Introduction

Polycrystalline-silicon thin film transistors (poly-Si TFTs) are extensively applied in the active-matrix liquid crystal display (AMLCD) at present. For high-level applications in the future, such as the peripheral integrated circuits (IC) of the system-on-panel (SOP) and three-dimensional (3D) IC, the high driving capability is necessary for the poly-Si TFTs. However, the normalized driving current of the most published poly-Si TFTs are still smaller than 100 μA/μm [1-2]. Therefore, it is very important to improve the driving capability of the poly-Si TFTs. Most research on the silicon-on-insulator (SOI) MOSFETs with the ultra-thin body (UTB) has shown excellent electrical characteristics [3-4], so the concept of the UTB could be easily extended to the poly-Si TFTs. Furthermore, several studies also indicate reducing the channel thickness of the poly-Si TFTs can also achieve larger driving current, lower leakage current, steeper subthreshold swing, and lower threshold voltage [5-6].

One issue of the ultra-thin poly-Si channel thickness is the degradation of its film quality. After the solid phase crystallization (SPC) process, the thinner poly-Si film consists of the smaller grain size and thus higher grain boundary trap density [5]. Therefore, the channel thickness of the published SPC poly-Si TFTs is just thinned to 20 nm [7]. The other issue of the poly-Si TFTs with the ultra-thin channel thickness is the large parasitic resistance at the source/drain (S/D) regions. Both of these issues degrade the driving capability of the poly-Si TFTs. In recent years, the poly-Si TFTs with various high-κ gate dielectrics, such as hafnium dioxide (HfO$_2$) and praseodymium oxide (Pr$_2$O$_3$), have been proposed to reduce the EOT [9-11] but the gate electrodes they used are close to planar structures.

On the basis of our previous work described in the previous chapter [8], we focus on the scaling of the equivalent oxide thickness (EOT) by using the high-κ gate dielectric in this chapter. The electrical characteristics of the poly-Si nanowire (NW) TFTs with the ultra short L$_G$ are investigated. The HfO$_2$ gate dielectric and the novel omega-shaped (Ω) gate structure are both employed to improve the gate-to-channel controllability and suppress the short

channel effect (SCE). And, the S/D parasitic resistance effect is improved by using Ni-silicide metal S/D.

6.2 Experiments

The detailed process flow of the SPC poly-Si NW TFTs combined with the HfO_2 gate dielectric is described below. This device is called device A. First, a 150-nm-thick silicon dioxide (SiO_2) was thermally grown on a p-type Si substrate. Next, a 20-nm-thick un-doped amorphous-Si film was deposited by a low pressure chemical vapor deposition (LPCVD) system as the channel layer. The average grain size of the amorphous-Si film was enlarged to about 55 nm after the SPC annealing in nitrogen (N_2) ambient at 600 ^{o}C for 24 hr. Then, the channel thickness of the poly-Si film was thinned to 10 nm by repetitions of the wet piranha ($H_2SO_4:H_2O_2 = 3:1$) oxidation and the dilute hydrofluoric acid (DHF) etching. The active area was patterned by electron-beam lithography (EBL) and reactive ion etching (RIE) on the poly-Si layer.

After the standard RCA cleaning process, a metal-organic CVD (MOCVD) system was used to deposit a 10-nm-thick HfO_2 gate dielectric (T_{HfO2} = 10 nm) at 500 ^{o}C. A 200-nm-thick un-doped amorphous-Si film was sequentially deposited by a LPCVD system and etched to define the gate pattern, and the omega-shaped gate structure was formed owing to the recessed and undercut etching of the buried SiO_2 by several cleaning steps. Then, a double spacer consisting of a 20-nm-thick tetra-ethoxy-silane (TEOS) SiO_2 and a 20-nm-thick silicon nitride (Si_3N_4) was formed by a plasma enhanced CVD (PECVD) system and RIE. Phosphorous ions were implanted into the amorphous-Si gate electrode at 60 keV to a dose of $5x10^{15}$ cm^{-2}. This ion implantation process also amorphorize the HfO_2 gate dielectric at the S/D regions so that it can be removed easier. After removing the HfO_2 layer by an isopropyl alcohol (IPA):HF mixture [12], the implanted dopants in the gate electrode were activated in N_2 ambient at 600 ^{o}C for 12 hr. To reduce the S/D parasitic resistance, the Ni-silicide metal S/D was fabricated by a low-temperature process. An 8-nm-thick Ni film was evaporated by electron-beam evaporation. Next, a two-step silicidation process was employed to form the Ni-silicide metal S/D [13]. Phosphorus ion implantation was used to dope the Ni-silicide metal S/D at 10 keV to a dose of $5x10^{15}$ cm^{-2}, then a furnace annealing at 600 ^{o}C for 30 min was performed to form the N^+ S/D extension region. Finally, some devices underwent a sintering process in forming gas (95 % N_2 and 5 % hydrogen (H_2)) at 400 ^{o}C for 30 min. Figure 1 shows the device structure inspected by the transmission electron microscope (TEM).

The L_G and the ultra-thin poly-Si channel thickness (T_{Si}) are 40 nm and 10 nm, respectively. The fully Ni-silicided S/D was successfully fabricated. The narrowest poly-Si NW channel width (W_G) observed by the scanning electron microscope (SEM) is 20 nm, as shown in the inset of Fig.6-1.

For comparison, the other two devices named device B and device C were also fabricated by using the process flow described in reference [8] and [14], respectively. The active layer thickness and the gate dielectric thickness of all devices are listed in Fig.6-2.

6.3 Results and Discussion

To investigate the intrinsic gate-to-channel controllability without the influence of the SCE, the transfer characteristics of three non-sintered long-channel devices with L_G = 5 μm and W_G = 10 μm are compared in Fig.6-2. The linear region threshold voltage (V_{TH}) is defined as the gate voltage (V_{GS}) at which the drain current (I_{DS}) equals to (W_G/L_G) x 10 nA at V_{DS} = 0.05 V. The drain-induced-barrier-lowering (DIBL) value is calculated from the difference in V_{TH} at V_{DS}=0.05V and 0.5V. The device key parameters including the V_{TH}, subthreshold swing (S.S.), and DIBL values are extracted and shown in the inserted table in the Fig.6-2. By comparing the device key parameters of the device B to those of the device C, it is observed that the scaling of the T_{Si} and T_{ox} can effectively improve the gate-to-channel controllability. The grain boundary trap density (N_t) is measured by Levinson's method [15]. For device B with ultra-thin T_{Si} of 8 nm, the N_t value is 5.266×10^{12} cm^{-2}, and is comparable to that of SPC poly-Si TFTs with the thicker T_{Si} [16]. Moreover, the off current of the device B is smaller than that of the device C owing to the thinner T_{Si}. As the TEOS SiO_2 gate dielectric is replaced by the HfO_2 gate dielectric to further reduce the equivalent oxide thickness (EOT), the device A exhibits the best transfer characteristics among these three devices. The S.S. and DIBL values can be further improved to 606 mV/dec and 2.283 V/V, respectively, but the gate-induced-drain-leakage (GIDL) effect is more apparent in the off-state as the result of the stronger electric filed between the gate electrode and the drain electrode.

Figure 6-3 shows the non-sintered and sintered transfer characteristics of the poly-Si NW TFTs combined with the HfO_2 gate dielectric, and its L_G/W_G is equal to 90 nm/20 nm, respectively. Before the sintering process, the V_{TH}, S.S., and DIBL values are 2.561 V, 253 mV/dec., and 0.459 V/V, respectively. It is indicated that the SCE can be greatly suppressed by the structure of the HfO_2 gate dielectric, the ultra-thin poly-Si NW, and the omega-shaped gate structure. After utilizing the 400 °C forming gas sintering process to passivate the grain

boundary defects and the poly-Si/interfacial oxide interface states, the V_{TH}, S.S., and DIBL values decrease to 1.162 V, 113 mV/Dec., and 0.254 V/V, respectively. The extremely high on/off current ratio of 2.52×10^7 is obtained at V_{DS} = 1 V. It has been reported that H_2 in the HfO_2 gate dielectric can form H^+ state to contribute the positive fixed charges [17], so it results in the negative V_{TH} shift after the sintering process.

Figure 6-4 shows the transfer and output characteristics of the poly-Si NW TFTs combined with the HfO_2 gate dielectric after the sintering process. The L_G/W_G is equal to 40 nm/20 nm, respectively. The V_{TH}, S.S., and DIBL values are -0.413 V, 248 mV/Dec., and 0.760 V/V, respectively. From the output characteristics, the driving current normalized to the W_G (I_{DS}/W_G) at V_{GS}-V_{TH} = 3 V and V_{DS} = 1 V is as high as 549 µA/µm, and exceeds the record value published in reference [8] with the even lower V_{GS}-V_{TH} value of 3 V. The on/off current ratio is 3.19×10^6 at V_{DS} = 0.05 V. This ratio is not very high because the thinner EOT results in higher GIDL current, but it is an acceptable value especially for TFTs. The field-effect mobility extracted from the maximum transconductance method is 7.04 cm^2/V-s because the SPC method was employed in this chapter.

6.4 Conclusions

The smallest poly-Si NW TFTs combined with the HfO_2 gate dielectric is demonstrated for the first time. The SCE is well controlled owing to the structure of the HfO_2 gate dielectric, the ultra-thin poly-Si NW, and the omega-shaped gate structure. The gate controllability could be further enhanced by scaling the equivalent oxide thickness. Moreover, the S/D parasitic resistance can be reduced by the Ni-silicide metal S/D. Therefore, the high performance poly-Si NW TFTs, especially for the ultra-high driving capability of 549 µA/µm, can be achieved without using the metal-induced lateral crystallization (MILC) and the excimer laser annealing (ELA) technology.

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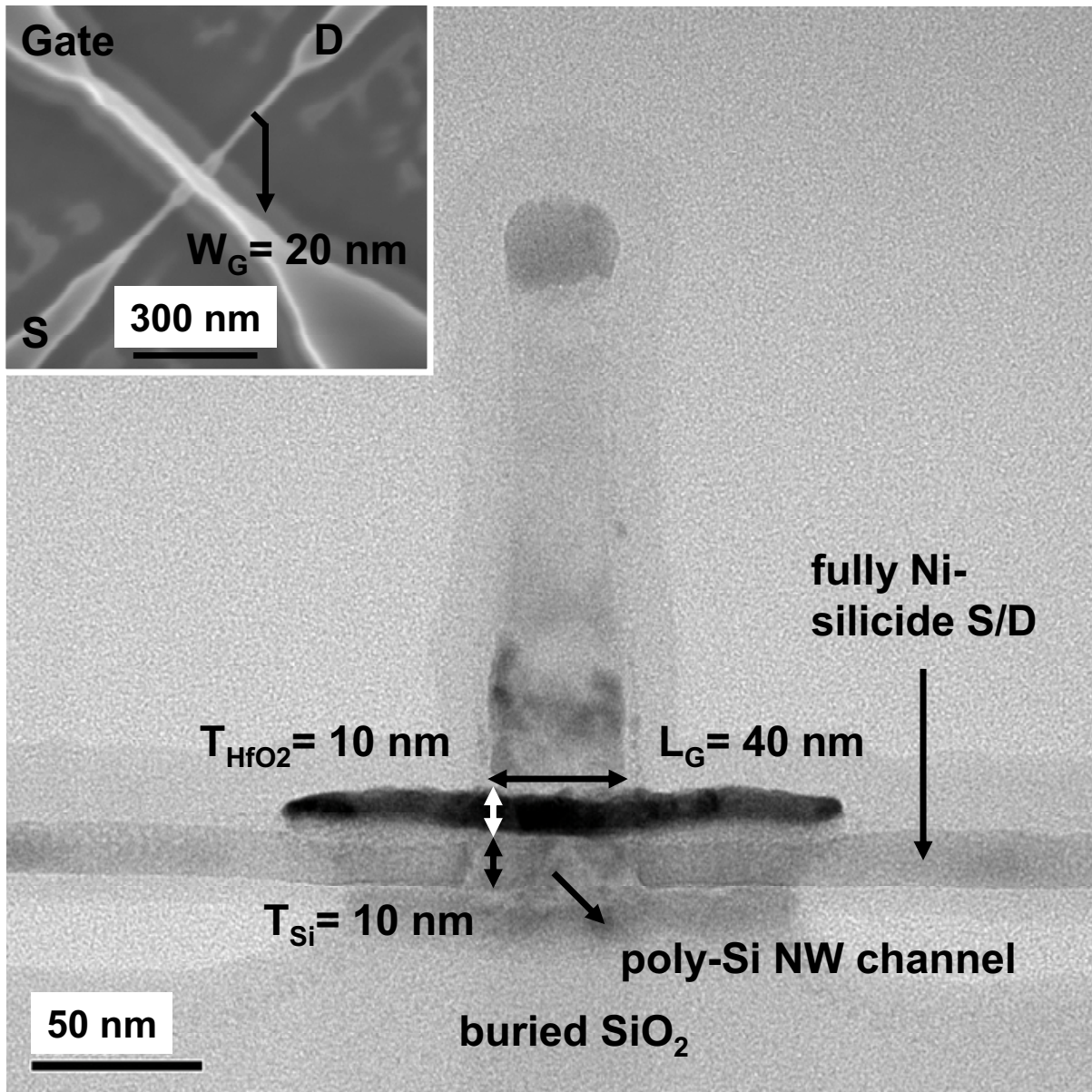
Fig.6-1. The cross-sectional TEM image of the poly-Si NW TFT combined with the HfO$_2$ gate dielectric with L$_G$/W$_G$ = 40 nm/20 nm. The inset shows the bird's-eye view of the SEM image.
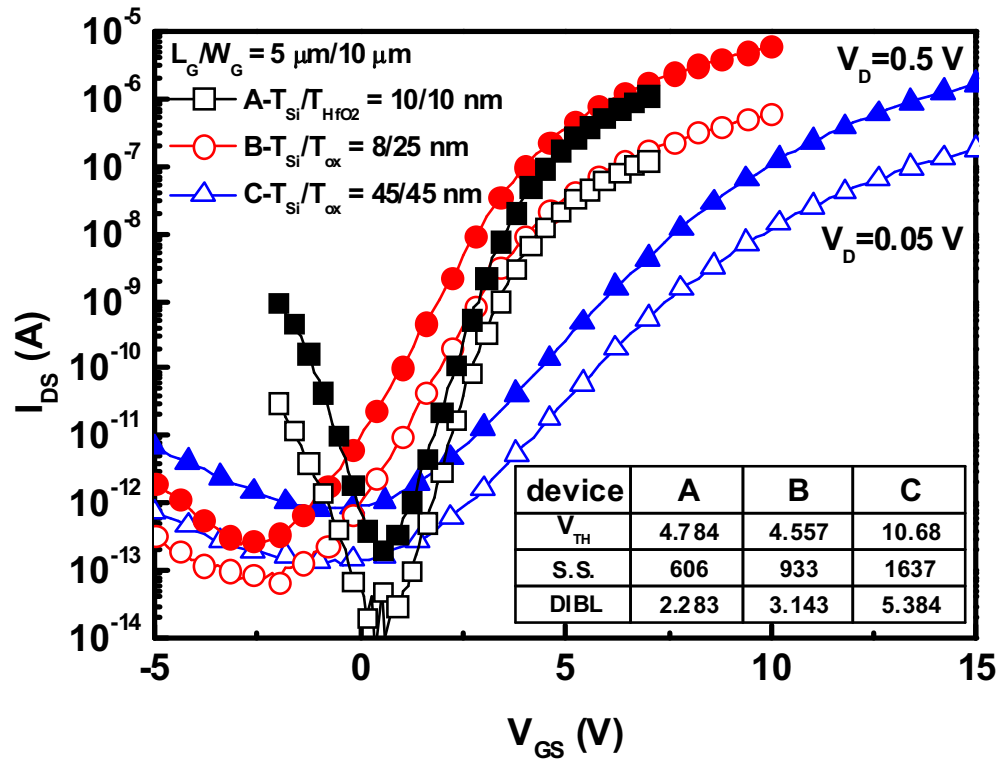
Fig.6-2. A comparison of the typical non-sintered transfer characteristics of the device A, device B, and device C with $L_G/W_G = 5 \mu m/10 \mu m$.
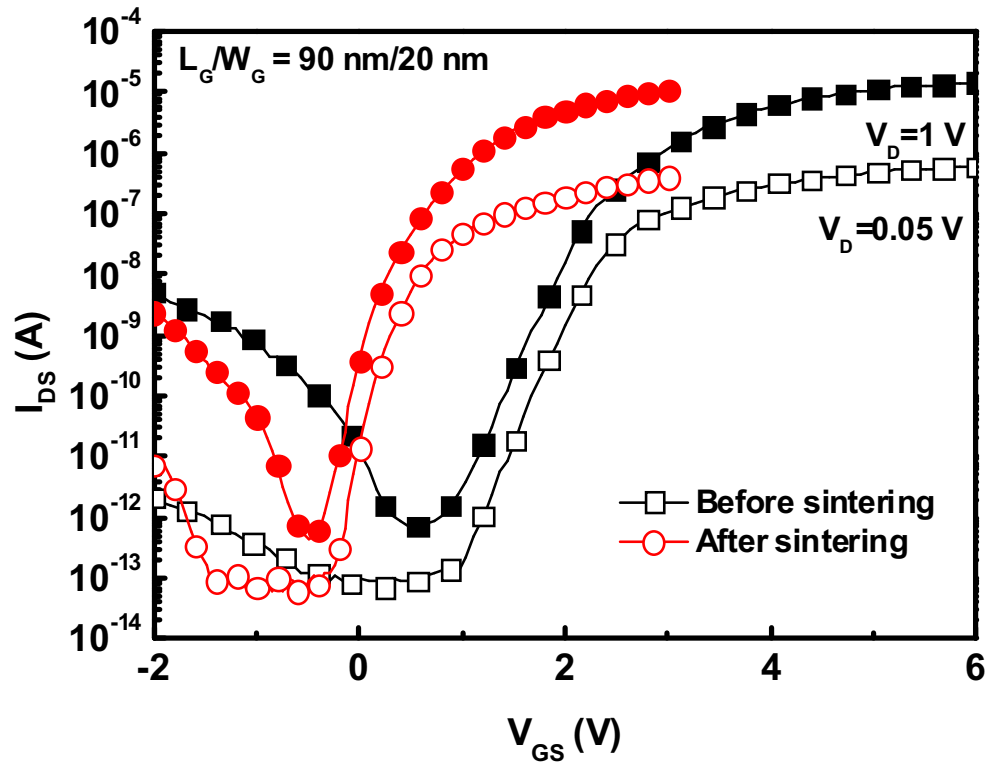
Fig.6-3. The non-sintered and sintered transfer characteristics of poly-Si NW TFTs combined with HfO$_2$ gate dielectric, and its L$_G$/W$_G$ = 90 nm/20 nm.
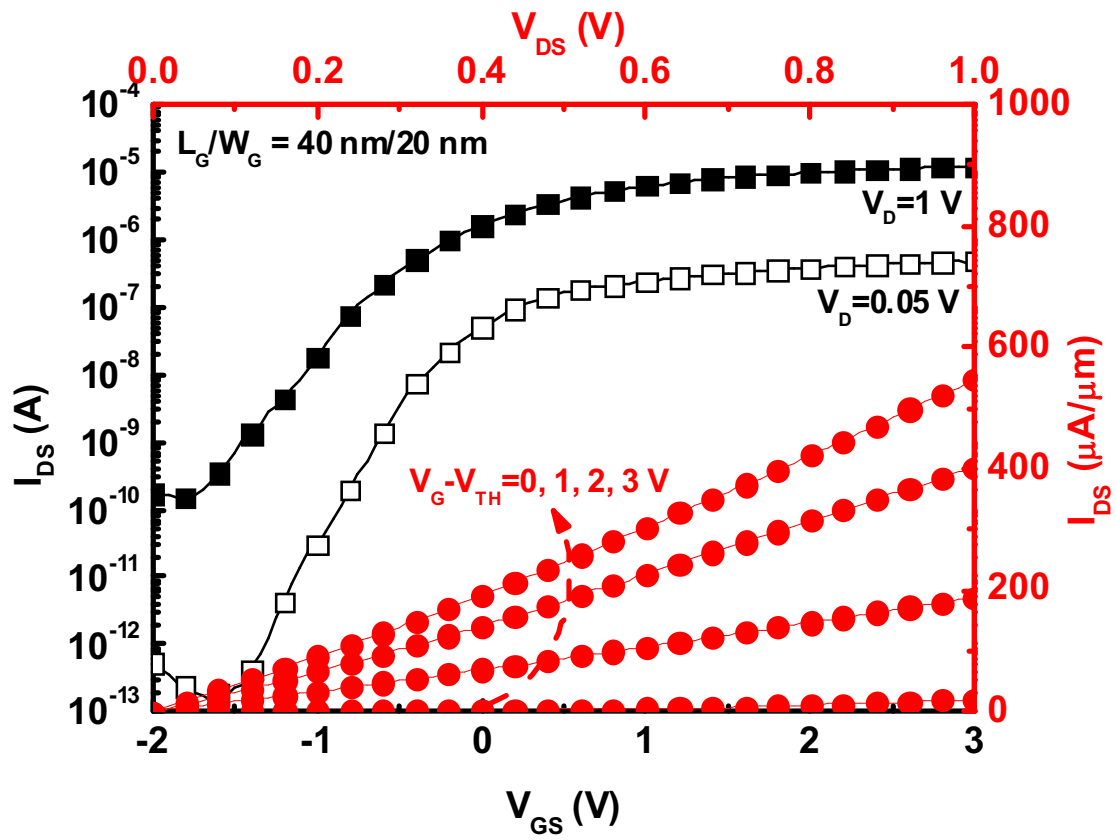
Fig.6-4. The typical sintered transfer and output characteristics of poly-Si NW TFTs combined with HfO$_2$ gate dielectric, and their L$_G$/W$_G$ = 40 nm/20 nm.

成果自評

　　此三年期計畫本計畫主要目標是開發高性能的全包覆閘極(GAA，Gate All Around)元件，並對 GAA 元件的傳導與可靠度進行分析。為製作 GAA 元件，必須先開發矽奈米線製作技術，以及奈米線接面、奈米線金屬矽化物等技術，並希望整合碳摻雜技術，以改善 NiSi 熱穩定性，且藉助 Si-C 產生的應力提高載子遷移率。原計畫目標是希望以微影蝕刻製程製作出直徑小於 10nm 的矽奈米線，但是受限於機台性能，整合電子束微影、光阻消減、電漿蝕刻等製程，僅能獲得 20nm 左右的奈米線。加上製程變異極大，探摻雜對奈米線電晶體的影響，被製程變異所掩蓋，無法觀測。因此計畫成果分成兩大部分，第一部分是碳摻雜技術以及對 NiSi 的影響；第二部分是全包覆式薄膜電晶體技術。

　　在碳摻雜技術方面，我們採用電漿浸潤技術、一般離子佈植技術、低能量/低溫離子佈植技術三種。過低的電漿浸潤能量會造成碳膜沈積，無法形成 NiSi，必須避免。三種技術的碳摻雜劑量達到 1×10^{15} cm^{-2} 以上，都可以提高 NiSi 的熱穩定性達攝氏 50-100 度，但是如果同時有高劑量的 As, P, B 等摻雜，碳摻雜的作用則不明顯。低能量離子佈植技術可以形成品質最好的非晶矽層，搭配快速退火+雷射退火，可以得到最高的替代性碳濃度。即使經過高溫退火，碳摻雜仍會增加矽基板的缺陷密度，Ni 可能藉由這些缺陷快速擴散，因此碳植入深度和接面深度必須適當搭配，以免接面漏電流增加。高劑量的碳摻雜可以微幅降低 NiSi/n-Si 的蕭基位障高度約 30meV，幅度不大，對於接觸電阻影響很小。

　　在全包覆式電晶體部分，因為直徑無法微縮到 10nm 以下，對於單晶矽電晶體而言，不具有優勢，故將重點轉移到多晶矽薄膜電晶體，整合各項模組技術，製作出通道長度 18nm，厚度 8nm 的世界最小的薄膜電晶體。進一步搭配高介電常數介電質，將驅動電流推進到 500uA/um 以上，接近單晶矽電晶體，創下多晶矽薄膜電晶體的最大電流紀錄。

　　總言之，計畫執行細部雖因內部因素及國際潮流而小有修正，但尚在原始規劃的全包覆式電晶體以及碳摻雜技術的主軸下進行。目前已發表兩篇 SCI 期刊論文、五篇研討會論文，一篇期刊論文在審查中，另有一篇期刊論文、一篇研討會論文在撰寫中。已取得的數據，估計至少可以再發表 2-3 篇 SCI 期刊論文。本計畫已經培育兩名博士、四名碩士，另一名博士班研究生應可在一年取得學位。不論在學術成果或是人才培育方面，均有良好成效。

Appendix : Publication List

SCI Journal Paper:

[1]. <u>Bing-Yue Tsui</u> and Chen-Ming Lee, "An Investigation on the Thermal Stability of Nickel Silicide and Shallow Junction Electrical Characteristics with Carbon Ion Implantation," Jap. Journal of Applied Physics, vol.49, No.4, pp.04DA04-1~04DA04-6, 2010.

[2]. Chen-Ming Lee and <u>Bing-Yue Tsui</u>, "A High Performance 30 nm Gate-All-Around Poly-Si Nano Wire Thin Film Transistor with NH_3 Plasma Treatment," IEEE Electron Device Lett., vol.31, No.7, pp.683-685, 2010.

[3]. Chen-Ming Lee and Bing-Yue Tsui, "High Performance Poly-Si Nano Wire Thin Film Transistors using the HfO_2 Gate Dielectric," submitted to the IEEE Electron Device Lett.

Conference Paper:

[1] Chen-Ming Lee, <u>Bing-Yue Tsui</u>, and Guang-Li Luo, "Improvement of Nickel Silicide Thermal Stability by Carbon Ion Implantation," in Proc. of the 15th Symposium on Nano Device Technology, p.26, 2008.

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