60 GHz Broadband MS-to-CPW Hot-Via Flip Chip Interconnects

Wei-Cheng Wu, Li-Han Hsu, Edward Yi Chang, *Senior Member, IEEE*, Camilla Kärnfelt, *Member, IEEE*, Herbert Zirath, *Member, IEEE*, J. Piotr Starski, *Senior Member, IEEE*, and Yun-Chi Wu

***Abstract*—In this letter, the microstrip-to-coplanar waveguide (MS-to-CPW) hot-via flip chip interconnect has been experimentally demonstrated to have broadband performance from dc to 67 GHz. The interconnect structures with the hot-via transitions were first designed and optimized by using the electromagnetic simulation tool. Three types of designs were investigated in this letter. The interconnect structures were then fabricated and radio frequency (RF) tested up to 67 GHz. The optimized interconnect structure with the compensation design demonstrated excellent RF characteristics with the insertion loss less than 0.5 dB and the return loss below 18 dB over a very broad bandwidth from dc to 67 GHz. This is to our knowledge the best result reported for this frequency range.**

***Index Terms*—Coplanar waveguide (CPW), finite ground coplanar (FGC) waveguide, flip chip, hot-via, interconnect, microstrip (MS).**

I. Introduction

FLIP chip interconnect has been proven to be a low-cost alternative with superior performance in all aspects over other interconnect schemes for high frequency applications. Flip chip architecture is more compatible with the coplanar chip designs. However, most existing chip designs are of microstrip (MS) type, which is of particular importance for power applications [1]. Thus, a modified architecture so-called "hot-via" [1] or "direct backside interconnect technology (DBIT)" [2] was proposed as the alternative of the flip-chip procedures, which showed the compatibility with the microstrip designs.

Hot-via transition adds three more advantages for the flip chip approach. First, detuning effect due to chip flipping is eliminated. Second, the chip can be optically inspected after bonding [1]. The third advantage is that it enables the chip to be surface mountable [chip scale packaging (CSP)] directly to the motherboard to achieve the goals of the easy assembly and cost reduction [3].

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W. C. Wu is with the Department of Materials Science and Engineering, National Chiao Tung University, Hsinchu 300, Taiwan, R.O.C. and also with Microwave Electronics Laboratory, Department of Microtechnology and Nanoscience, MC2, Chalmers University of Technology, Göteborg SE-412 96, Sweden (e-mail: edc@mail.nctu.edu.tw; williamwu.mse90g@nctu.edu.tw).

L. H. Hsu, E. Y. Chang, and Y. C. Wu are with the Department of Materials Science and Engineering, National Chiao Tung University, Hsinchu 300, Taiwan, R.O.C. (e-mail: edc@mail.nctu.edu.tw).

C. Kärnfelt, H. Zirath, and J. P. Starski are with the Microwave Electronics Laboratory, Department of Microtechnology and Nanoscience, MC2, Chalmers University of Technology, Göteborg SE-412 96, Sweden.

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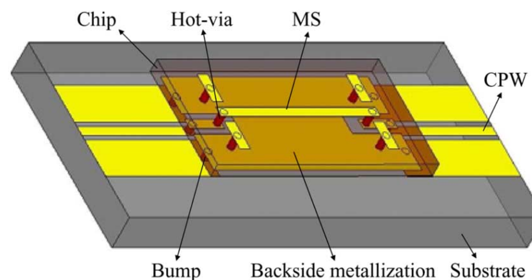

Fig. 1. Hot-via flip chip interconnect structure of this work.

In the literature, [1] reported a frequency range of 32 to 42 GHz with the return loss below 15 dB. [2] demonstrated a interconnect performance from dc to 20 GHz with the return loss below 15 dB. In [3] and [4], the results showed the return loss below 15 dB from dc to 25 GHz. To date, the hot-via approach with the broadband performance over 40 GHz has not been experimentally proved and reported.

In this letter, three types of micorstrip-to-coplanar waveguide (MS-to-CPW) flip chip interconnect structures were fabricated in-house with the modified backside process steps and were radio frequency (RF) characterized up to 67 GHz. Fig. 1 shows the MS-to-CPW hot-via flip chip interconnect structure of this work. The interconnect performance of the structures with and without the ground pads and vias were compared. The compensated interconnect structure showed excellent performance with the insertion loss within 0.5 dB and the return loss below 18 dB from dc to 67 GHz, where the transitions of the hot-vias and bumps only accounted for 0.23 dB loss. With the experimentally demonstrated data, this study further extends the hot-via approach for the microstrip monolithic microwave integrated circuits (MMICs) packaging to 60 GHz and above.

II. Design and Fabrication

The design and optimization of the hot-via flip chip interconnects were performed using the simulation tool HFSS for the 3-D electromagnetic field analysis.

Fig. 2 shows the schematics of the three different demonstrated interconnect structures in this study with each parameter defined and optimized, designated as Designs I, II, and III. The material of the substrate was Al_2O_3, and the material of the chip was GaAs; the thicknesses of the substrate (h_s) and chip (h_c) were 254 μm and 100 μm, respectively. The conductor metal was 3 μm Au. The microstrip (signal width, $s = 76$ μm) on the chip and CPW ($s = 76$ μm, $g_s = 38$ μm) on the substrate

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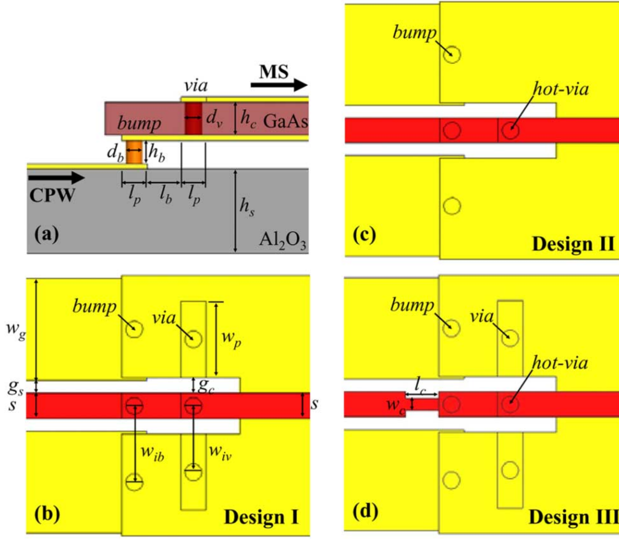

Fig. 2. Three demonstrated MS-to-CPW hot-via flip chip interconnect transition structures. (a) Side-view. (b) Top-view of the structure Design I with each parameter defined and optimized. (c) Top-view of Design II. (d) Top-view of Design III.

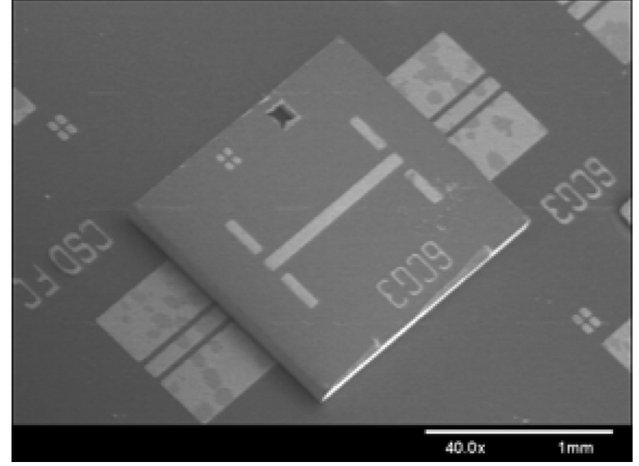

Fig. 3. SEM image of the fabricated MS-to-CPW hot-via interconnect structure.

were with the characteristic impedances (Z_0) equal to 50 Ω. The total length of the MS-to-CPW hot-via interconnect structure was 3000 μm, including the microstrip line on the chip (1000 μm) and the CPW line on the substrate (750 μm). In the design, finite-ground coplanar (FGC) waveguide was employed on the substrate instead of the conventional CPW with large ground planes to effectively suppress the parallel plate and higher order modes. To eliminate coupling of CPW mode into slotline mode, the symmetry was always kept along the signal transmission lines [5]. During optimization, the simulated results indicated that smaller radius for the via holes and bumps and higher bumps height led to lower reflection at the interconnects. However, due to the fabrication concerns, the dimensions of the via holes and bumps were fixed in the optimization of the design to simplify the fabrication process. The diameters of the via holes (d_v) and bumps (d_b) were both 50 μm; the bump height (h_b) was 30 μm. The width of the ground pads on the chip (w_p) was set at 228 μm, and the gap (g_c) was 46 μm. The length of the pads (l_p) was 76 μm; the signal length on the chip backside (l_b) was 100 μm. The locations of the via holes and bumps were optimized, where $w_{iv} = 198$ μm and $w_{ib} = 228$ μm. The goal of the optimized design was to achieve low reflection at the interconnect with a very broad bandwidth from dc to 60 GHz.

Conventionally, the microstrip MMICs have the ground pads and vias at the ends of the microstrip lines to enable the on-wafer measurements with the GSG (ground–signal–ground) probes. However, this might induce some parasitics in the interconnects. Therefore, in Design II, the ground pads and vias on the chip was removed in the fabricated structure to investigate the parasitic effects due to the existence of the ground pads and vias, as shown in Fig. 2(c).

For the typical dimensions of the flip chip interconnects, the bump transition shows a strong capacitive behavior resulting from the dielectric loading due to the presence of the chip and substrate dielectrics [6]. It degrades the reflection property at high frequencies. It was suggested that the bump pads should be as small as possible to lower the capacitance. However, this always causes great concerns in the real fabrication. To achieve the low reflection at the bump transition, one efficient way was adopted in this study by implementing the high impedance line in front of the bump transition; the design is designated as Design III. The high impedance line exhibits an inductive effect to compensate the capacitive part in the reactance. The location and dimensions of the compensated patterns were optimized by electromagnetic (EM) simulation, as shown in Fig. 2(d), where $w_c = 16$ μm and $l_c = 50$ μm.

The demonstrated MS-to-CPW hot-via interconnect structures were then fabricated with the in-house developed modified backside process steps. The substrate circuits with Au bumps were fabricated by using the standard Au bumping process as reported in [7]. The Au-to-Au thermocompression process was performed to bond the chip samples to the substrate samples. Fig. 3 shows the scanning electron microscope (SEM) image of the bonded hot-via interconnect structure. The three different structures were RF characterized up to 67 GHz to test the broadband interconnect performance of the hot-via approach.

III. Experimental Results

The scattering parameters of the fabricated MS-to-CPW hot-via flip chip interconnect structures were characterized by using the on-wafer probing measurement system. During the measurements, a 10 mm thick layer of Rohacell 31 ($\epsilon_r = 1.04$ at 26.5 GHz) was placed between the samples and the metal chuck of the probe station to avoid the grounded backside under the substrate. Fig. 4 shows the measured transmission coefficients of the three hot-via interconnect structures. From the measured results, Design I and II showed small variation both in the reflection and insertion properties, indicating the ground pads and vias had minor influences on the interconnect performance. From dc to 20 GHz, the return loss was less than 25 dB; from 20 to 50 GHz, the return loss was less than 15 dB. Above 50 GHz, the reflection became worse but was less than 12 dB.

To further improve the transmission performance of the proposed hot-via architecture, the high impedance line was adopted on the circuits in Design III. From the results in Fig. 4, further improvements of the insertion and reflection properties in the interconnect structure were achieved in this design. At 60 GHz,

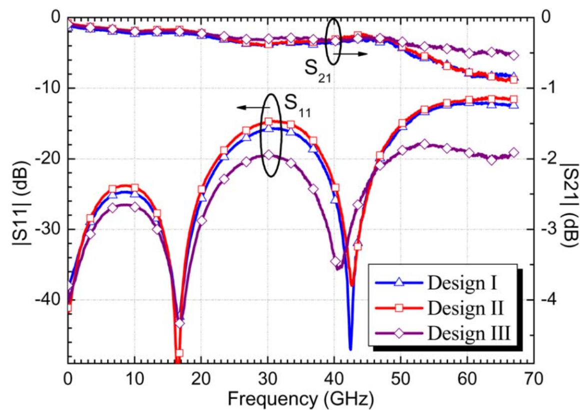

Fig. 4. Comparison of the measured transmission coefficients.

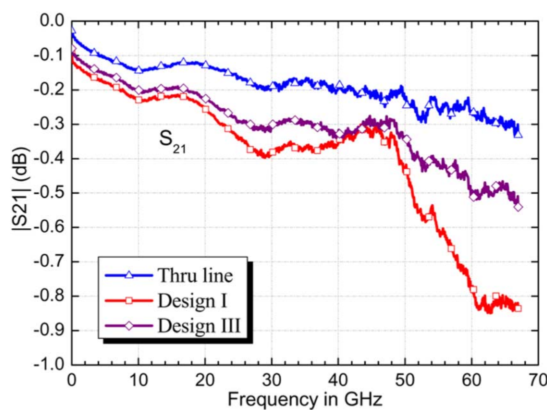

Fig. 5. Comparison of the measured insertion loss versus frequency between the thru line on the Al_2O_3 substrate and the two designs of the hot-via flip chip interconnect structures (Design I and III).

TABLE I
LOSSES

Frequency (GHz)	20	40	60
Loss of the interconnect structure (dB)	0.22	0.32	0.49
Loss of the transmission line (dB)	0.13	0.19	0.26
Loss of the transitions (dB)	0.09	0.13	0.23

the return loss was improved from 12 to 19 dB, and the insertion loss was also improved from 0.8 dB to 0.5 dB. The compensation design improved both the transmission characteristics and the bandwidth. From dc to 67 GHz, the return loss was less than 18 dB, and the insertion loss was within 0.5 dB. Based on the bump/hot-via transition model in [4], the values of each section for the transition in this study were calculated and optimized, where $Z_{bump} = 175\ \Omega$, $Z_{b\text{-}CPW} = 50\ \Omega$, $Z_{hot\text{-}via} = 60\ \Omega$, and $C_{open\text{-}end} = 8$ fF. Because of the overall capacitive effect, the return loss became worse as the frequency increased. The high impedance line optimized by EM simulation was calculated to have the inductance about 34 pH, which compensated the capacitive effect of the transition to match close to 50 Ω and therefore gave a broadband interconnect performance.

Fig. 5 shows the comparison of the measured insertion loss versus frequency of the CPW transmission line on the Al_2O_3 substrate and the two interconnect structures, Design I and Design III. The CPW transmission line was equal in length to the two interconnect structures. The insertion loss of the two interconnect structures was both a little higher than that of the CPW thru line. Compared with the thru line structure, the hot-via flip chip interconnect structure had four more vertical transitions including two hot-via transitions at the chip side and two bump transitions at the substrate side. At 60 GHz, the insertion loss of Design I was 0.8 dB, which was 0.5 dB worse than the CPW thru line. However, the compensated hot-via interconnect structure, Design III, just exhibited the insertion loss about 0.5 dB at 60 GHz, which was only 0.2 dB higher than that of the CPW thru line. Table I shows the calculated losses of the hot-via and bump transitions (Design III) at 20, 40, and 60 GHz. It should be noticed that the four vertical transitions (two hot-vias and two bumps) induced only 0.23 dB in the insertion loss at 60 GHz.

It is demonstrated that with the compensated design the hot-via architecture can achieve low reflection and low insertion loss with a very broad bandwidth over 60 GHz. The excellent performance reveals the potential of the hot-via approach for microstrip packaging solutions up to V band and above.

IV. CONCLUSION

This study demonstrates a hot-via architecture exhibiting excellent interconnect performance with very low transition loss over a very broad bandwidth from dc at least up to 60 GHz. Three different designs of the hot-via interconnect structures were fabricated in-house with the patterned backside process. It was demonstrated that the ground pads and vias on the MMIC had minor influence on the interconnect performance. With the compensated design, the MS-to-CPW hot-via flip chip interconnect structure was demonstrated to have the insertion loss within 0.5 dB and return loss below 18 dB from dc to 67 GHz, where the hot-via and bump transitions only accounted for 0.23 dB loss. This study demonstrates the promising results for the use of the hot-via approach as the packaging solutions for the microstrip design based MMICs at high frequencies up to 60 GHz and above.

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