12 吋矽晶圓半導體 CVD 製程設備及 BST 介電薄膜成長研究（Ⅰ）

Research and Development of CVD Process Equipment for a 12-inch Single Silicon Wafer and Growth of BST Dielectric Film（Ⅰ）

計畫編號：NSC 89-2212-E-009-037

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一、中文摘要

本整合型群體研究計畫將以四年時間設計與建立一座實驗用的 12 吋矽晶圓 CVD 反應爐，此反應爐之進氣系統將針對未來極可能用於 1 Gbit DRAM 以上的 BST 介電薄膜來設計。由於 Ba 及 Sr 的 Liquid Sources 揮發性很低，且在高溫下容易分解，因此不能以一般的 Bubbling 方式來產生蒸氣，本研究採用 Flash evaporation 建立此成長 BST 薄膜的進氣系統。此外，本計畫亦將探討矽晶圓上的 BST 薄膜製程參數，微結構分析，並進行熱物理性質、材料性質及電性量測，也將對 12 吋矽晶圓進行熱應力分析。

本群體研究計畫共有三個子計畫。子計畫一的主要工作是設計與建立 12 吋矽晶圓 CVD 反應爐的加熱及控溫系統，以及成長 BST 薄膜的進氣系統，並進行整個反應爐的系統整合。子計畫二的主要工作是 BST 薄膜及其所使用的基材的熱物理性質量測和 BST 薄膜在 12 吋矽晶圓上之熱應力分析。子計畫三的主要工作是尋求 BST 薄膜成長的製程參數，並進行 BST 薄膜微結構分析與材料及電學性質量測，提供子計畫一設計反應爐所需之參考資料。

這些子計畫將以 Interactive 及 Iterative 的方式整合在一起，一步步改進系統設計及設備。在第一年的研究（88 年 9 月至 89 年 7 月），各子計畫已完成預期的工作項目，獲得初步的結果。詳細的成果，請參閱各子計畫之精簡報告。

關鍵詞：CVD 反應爐設計，BST 薄膜成長

Abstract

This four-year group research project intends to design and establish an experimental CVD (Chemical Vapor Deposition) reactor for a 12-inch single silicon wafer. In the present study the gas feeding unit for the reactor is especially designed for the growth of the BST thin film. This film is considered to be a very suitable dielectric layer for the future DRAM with capacity larger than 1 Gbit. In view of the low volatility of the Ba and Sr sources and their easy decomposition at high temperature, the vaporization of these sources can not be fulfilled by the usual bubbling technique. We use flash evaporation to establish the gas feeding unit for the growth of BST thin film. In addition, this project plans to investigate the process parameters for the BST thin film growth on the silicon wafer, the micro-structure of the BST thin film and the thermalphysical, material and electrical properties of the film. Besides, the thermal stress in the 12-inch wafer will be predicted.

There are three individual projects in

this group research project. The first individual project intends to design and build the heating and temperature control system for the 12-inch single wafer CVD reactor, the gas feeding unit for the BST thin film growth, and the integration of various components to form a CVD reactor system. The major task in the second individual project is to measure the thermalphysical properties of the BST film and silicon wafer and analyze the thermal stress in the 12-inch silicon wafer. While in the third individual project the process parameters for the BST thin film growth will be determined. Besides, the micro-structure of the BST thin film will be analyzed and the material and electrical properties of the film will be measured. The results from this study will provide the data for the design of the reactor in the first individual project.

These individual projects will be integrated together through regular iterative discussion and interactive tests and improvement of the system design. In the first year of the study (August 1999~July 2000) some preliminary results have been obtained. The details on these results can be found in the brief reports from each individual project.

Keyword: CVD reactor design, BST thin film growth

二、計畫緣由及目的

由於微電子元件之日益急速微小化及晶片功能之大幅提昇，積體電路已由 VLSI **發展到** ULSI**，晶片也由** 8 **吋擴大至** 12 **吋，因此如何精確地控制熱流條件使在大晶圓上成長的各類薄膜能達到均勻厚度、純度、線寬等之要求，以及減低晶片內之熱應力等，實為目前急需解決之重要問題。本整合型計畫之主要目的即在探討如何經由詳細分析、實驗及實作來建立未來** IC **製程中常用之** 12 **吋矽晶圓** CVD **反應爐，建立一套新的實驗系統，成長未來** 1 Gbit **以上的** DRAM **將採用深具潛力之** BST **薄膜，對於國內自行建立** CVD **反應爐之能力甚有助益。**

CVD **為** IC **晶片製造之重要製程之一，先進國家在這方面已有甚多之研究，但國內至今做的並不多，尤其是在建立** CVD **反應爐設備方面，落後甚多。過去的** IC **晶片製造大多為** resistance heating**，較難精確製造細微線路，且能源消耗較多。近來所發展之單一大晶片的** rapid lamp heating **則較省能，微細線路控制較好，但只要有少許之溫度不均勻，易造成薄膜厚度不均勻，且晶片及薄膜易受熱應力而變形或破裂。**

有關 rapid lamp heating CVD **製程研究，近年來國外已有不少，但如何由國內獨立** CVD **設備技術則尚須努力。重要之相關** CVD **專書及近年之** review**，如** refs **【**1-19**】。**

三、結果與討論

（1**）子計畫一已提出實驗用** 12 **吋矽晶圓** CVD **反應爐設計圖（圖一），且已完成主動式熱控制器之建立，初步測試結果顯示，晶圓溫度之均勻性可獲大幅改善。另外，亦針對** BST **薄膜成長設計進氣系統，此系統目前正在建立。**

（2**）子計畫二已建立晶圓及其薄膜熱物理性質的量測系統，已進行初步測試，同時亦獲得一些熱應力分析之結果。**

（3**）子計畫三利用小型** CVD **成長爐，已初步獲得** BST **薄膜成長之製程參數，正深入瞭解薄膜性質。**

四、計畫成果自評

在此第一年的研究，各子計畫均按預定項目執行，並已獲得初步成果，對於 12 **吋大晶圓之熱流控制已漸能掌握, 並對** BST **薄膜之成長參數也有深入瞭解，可作為將來在大晶圓上薄膜成長之參考。**

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