An Innovative Understanding of Metal–Insulator–Metal (MIM)-Capacitor Degradation Under Constant-Current Stress

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***Abstract*—This paper provides a new understanding of metal–insulator–metal-capacitor-degradation behavior under a wide range of constant-current-stress conditions. It was found that capacitance degrades with stress, but the behavior of the degradation strongly depends on the stress-current density. At high stress levels, the capacitance increases logarithmically as the injection charge increases until dielectric breakdown occurs. At lower stress conditions, the degradation rate is proportional to the stress current and reverses after a certain period of time. A metal-insulator interlayer is observed using cross-sectional transmission-electron-microscopy micrographs, which possibly explains this reversal phenomenon.**

***Index Terms*—Capacitance, constant-current stress (CCS), interface, metal–insulator–metal (MIM).**

I. Introduction

METAL–INSULATOR–METAL (MIM) capacitors embedded in the backend interlevel dielectric layers as passive components are widely used for analog and RF applications. The stability of MIM capacitors is an important issue when considering the accuracy of analog functions. For applications requiring extreme precision, such as A/D and D/A converters, only a $\pm 0.01\%$ mismatch is allowed [1]. However, the capacitance-degradation behavior of a single capacitor has not been well characterized. Besset *et al.* [2] depicted the MIM-capacitance variation under electrical stress and observed that the relative-capacitance variation was dependent on the injected charge but was independent of stress current.

In this paper, the degradation of SiO_2 MIM capacitors was investigated under a wide range of stress conditions. It was found that the capacitance increases logarithmically as the injection charge increases, but the correlation between the injected charge and the capacitance variance is different for various stressed currents. Furthermore, a reversal in the degradation after a certain period of time, depending on the stress level, was also observed and began earlier at higher temperatures. This paper provides an innovative understanding of MIM-capacitor-degradation behavior under a wide range of constant-current-stress (CCS) conditions.

II. Experimental Setup

A 380-Å SiO_2 MIM structure with a 1-fF/μm^2 capacitance and an area of 6000 μm^2 was used in this paper. A SiO_2 layer was deposited using plasma-enhanced chemical-vapor deposition. AlCu and TiN/AlCu layers were used as the top and bottom electrodes of the MIM, respectively. An Agilent 4072 A parametric tester with a 4284 A LCR meter was used to perform the stress and to measure the capacitance in the 50-mV signal at 100 kHz. The samples were stressed under a constant current in the range of 0.01–20 nA, corresponding to a current density of 0.17–333 μA/cm^2, at various temperatures from 25 °C to 75 °C in order to study the capacitance variations under different electrical stress conditions. The initial capacitance C_0 of the sample was measured before stressing, and the stress was interrupted at regular intervals of 10 s to measure the capacitance. The capacitances were also monitored after removing the stress to investigate the dielectric relaxation characteristics. In addition, transmission-electron-microscopy (TEM) micrographs were utilized to characterize the cross-sectional structures.

III. Results and Discussion

To determine the degradation, a capacitor with an initial capacitance C_0 was measured periodically while under stress conditions. Fig. 1 shows the relative-capacitance variation $(C-C_0)/C_0$ as a function of the injected charge at 25 °C for various CCS values from 0.01 to 20 nA, corresponding to a current density of 0.17–333 μA/cm^2. In general, the relative-capacitance variation increases logarithmically as the injected charge increases and is similar to the charge-trapping behavior in dielectric film [3], which implies a correlation between the capacitance variation and the charge trapping.

In an MIM system, which is composed of two parallel metallic plates with an insulator thickness d, the capacitance is calculated by using

$$C = \varepsilon \frac{A}{d} \quad (1)$$

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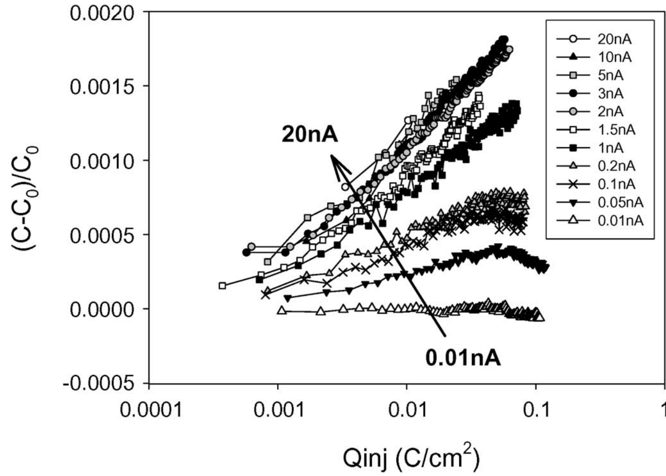


Fig. 1. Relative-capacitance variation as a function of the injected charge at 25 °C for various CCS values from 0.05 to 20 nA.

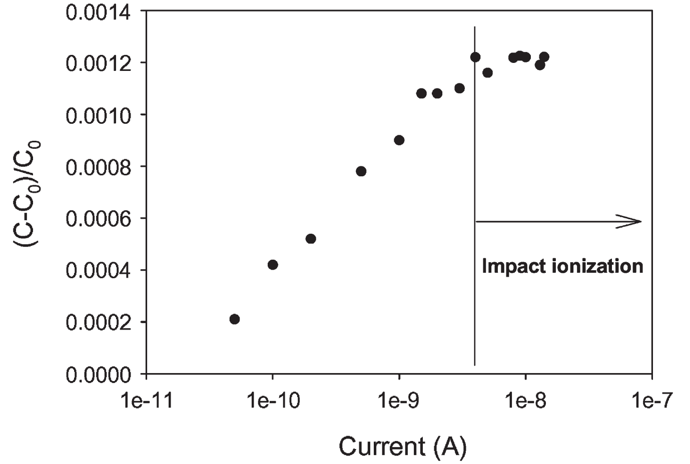


Fig. 2. Dependence of relative-capacitance variations on stressed current at an injected charge of 0.01 C/cm^2.

where ε is the permittivity of the insulator, and A is the area of the plate. The capacitance is proportional to the dielectric permittivity. Moreover, the dielectric local permittivity ε can be expressed as a function of the trapped charge [4]

$$\begin{aligned}\varepsilon &= \varepsilon_{\mathrm{SiO_2}} + N^e \cdot \frac{8 \cdot \alpha \cdot q^2}{\pi \cdot A^3 \cdot K^e} + N^h \cdot \frac{8 \cdot \alpha \cdot q^2}{\pi \cdot A^3 \cdot K^h} \\ &= \varepsilon_{\mathrm{SiO_2}} + \varepsilon_q \end{aligned} \tag{2}$$

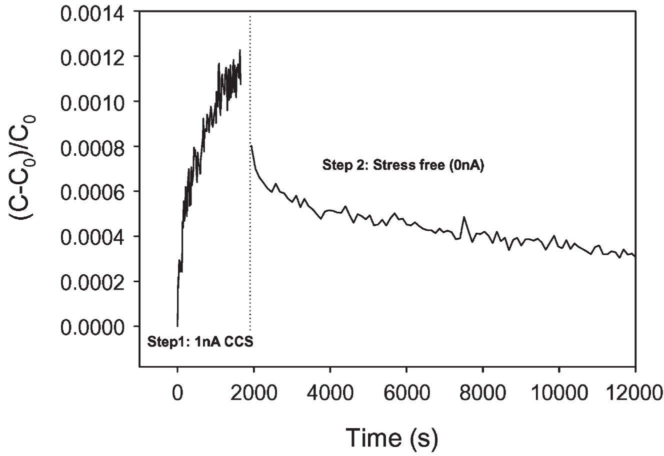
where α is the atomic polarizability of the dielectric, q is the unit charge, A is the distance between the molecules, and K^e/K^h and N^e/N^h are the potential energy profile of the trap (spring constant) and the density of the trapped charges inside the dielectric for the electron and the hole, respectively. The increase in capacitance can be correlated to the generation of new dipoles in the dielectric as a result of charge trapping [2], [5].

The dependence of relative-capacitance variations on the different stress-current levels at a 0.01-C/cm^2 injected charge is shown in Fig. 2. When applying a current greater than 3 nA, the variation is injected-charge-dependent and stress-current-independent as other studies have observed [2]. However, in lower current conditions, the variations are shown to be not only dependent on the injected charge but also dependent on the stress current. The differences in behavior of stressed currents greater than 3 nA could be correlated to the onset of impact ionization within the oxide during stress. The critical electric field that triggers impact ionization is approximately 9 MV/cm in SiO_2 with a thickness of 380 Å [6], and the voltage monitored under 3 nA conditions is about 33.5 V, corresponding to an electric field of 8.8 MV/cm for a thickness of 380 Å. The current level associated with this field is also shown in Fig. 2. Furthermore, high current stress is applied through a higher voltage, and hence, the charge carriers are more energetic and can create traps in the dielectric. This may explain the stress-current dependence before the onset of impact ionization.

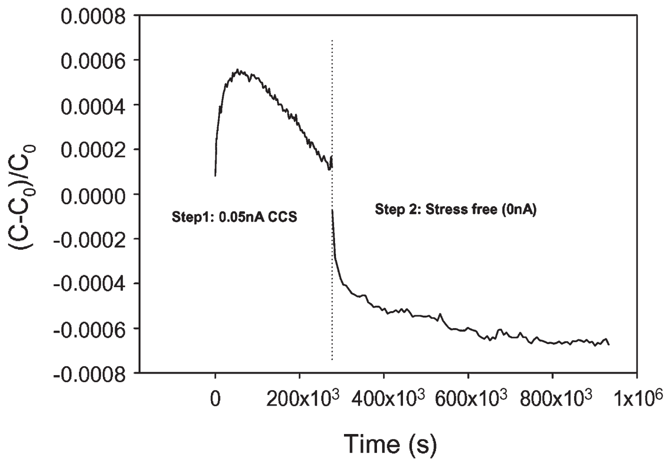
The capacitance in most samples continued to increase until such time that a breakdown occurred. However, for lower stressed-current conditions that are able to sustain stress for longer durations without breaking down, such as 0.1 and 0.05 nA, corresponding to current densities of 1.66 and 0.83 μA/cm^2, respectively, a reversal in capacitance variation was observed after a certain period of time, as shown in Fig. 1. It appears that the relative-capacitance variation is a combination of two opposite effects, but in the early stage, it increases dramatically and is dominant over the decreasing factors. When applying a current greater than 1 nA, a breakdown occurred in the sample, and further stressing could not continue; thus, the reversal phenomenon was not observed in samples subjected to higher stress levels due to the relatively short stress time.

To evaluate the capacitance changes after detrapping, a two-step experiment was performed. Fig. 3(a) shows the time dependence of the capacitance variation during both ON and OFF stress at 1 nA. Once the stress bias is removed, the capacitance begins to decrease rapidly. The poststress capacitance variation appears to have a saturationlike behavior after the initial rapid decrease, which is similar to the well-known charge-detrapping phenomenon [6] that demonstrates that the capacitance decrease is associated with the detrapping of the previously trapped charge. For lower stress conditions, together with the variation reversal shown in Fig. 3(b), the capacitance also decreases, when the stress bias is removed, and culminates to a lower value than the initial capacitance value, which indicates that the capacitance decreases intrinsically when the effect of the trapped charge is not considered. The figures are replotted in a log time scale with a normalized start point, as shown in Fig. 4.

Fig. 5 shows the TEM cross-sectional images for both a fresh sample and a sample that had been stressed for an extended period. An interlayer is observed between the top AlCu electrode and the SiO_2 dielectric. This interlayer may play an important role in the capacitance variation. Trap filling and generation also occurred and became more pronounced with the increase in charge carrier energy, which were followed by charge detrapping after discontinuing the stress. In contrast, the change of interlayer properties such as thickness will affect

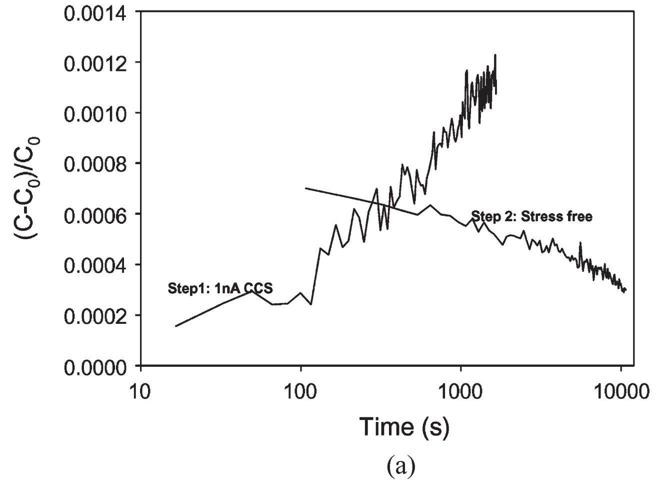


(a)

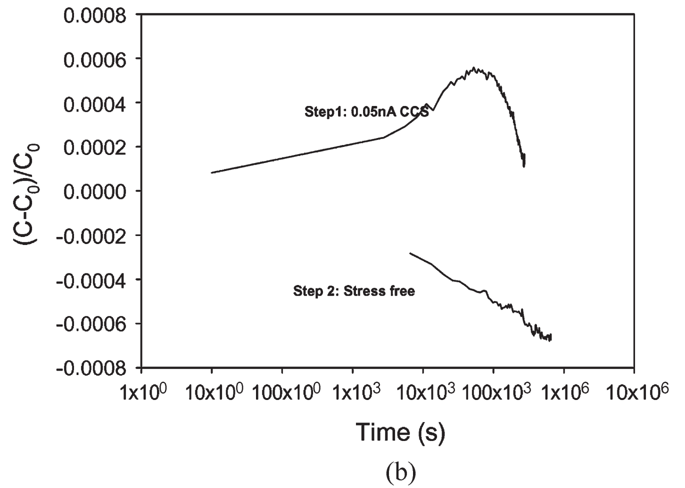


(b)

Fig. 3. Time dependence of the capacitance variation during ON and OFF stress for $I = $ (a) 1-nA and (b) 0.05-nA stress conditions.



(a)



(b)

Fig. 4. Plot of time dependence of the capacitance variation during ON and OFF stress for $I = $ (a) 1-nA and (b) 0.05-nA stress conditions using log time scale with a normalized start point.

the final capacitance. The total capacitance of the capacitors connected in series can be calculated using

$$\frac{1}{C_{\text{total}}} = \frac{1}{C_{\text{ox}}} + \frac{1}{C_{\text{int}}} \tag{4}$$

$$C_{\text{total}} = \frac{C_{\text{ox}} C_{\text{int}}}{C_{\text{ox}} + C_{\text{int}}} \tag{5}$$

where C_{ox} and C_{int} are the capacitances of the dielectric SiO_2 and the interlayer, respectively. A thicker interlayer results in a lower capacitance and influences the total capacitance of the MIM system, which might explain the capacitance reversal phenomenon in a capacitor under long-term stress conditions.

Although the change in thickness is so small, and the metal oxide has a high permittivity, the decrease in the capacitance is still reasonable. Consider an extreme case where only 1-Å Al_2O_3 $(k = 10)$ formed on the 380-Å SiO_2 $(k = 3.9)$. The capacitance

$$C = \frac{k \cdot \varepsilon_0 \cdot A}{d} = B \cdot \frac{k}{d} \tag{6}$$

where B is a constant, the capacitance of the original 380-Å SiO_2

$$C_{\text{ox}} = B \cdot \frac{3.9}{380} \tag{7}$$

and the capacitance of 1-Å Al_2O_3

$$C_{\text{int}} = B \cdot \frac{10}{1}. \tag{8}$$

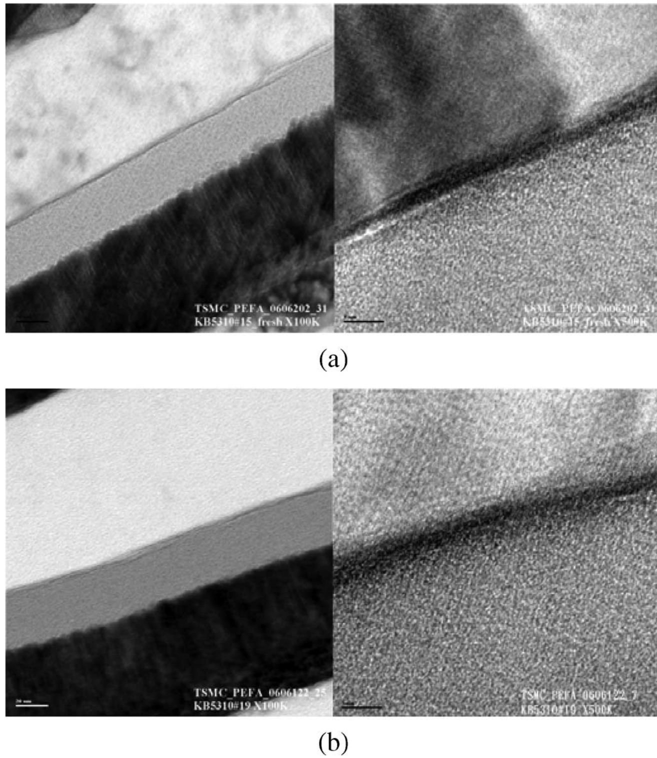
The total capacitance can be calculated using

$$C_{\text{total}} = \frac{C_{\text{ox}} C_{\text{int}}}{C_{\text{ox}} + C_{\text{int}}} = B \cdot \left[\left(\frac{3.9}{380} \cdot \frac{10}{1} \right) \Big/ \left(\frac{3.9}{380} + \frac{10}{1} \right) \right]. \tag{9}$$

Furthermore, the relative-capacitance variation

$$\frac{C_{\text{total}} - C_{\text{ox}}}{C_{\text{ox}}} = -0.001025264 \approx -0.1\%. \tag{10}$$

In this paper, the overall capacitance change is a small value of $< 0.1\%$, as shown in Fig. 2(b). This implies that the overall thickness change should be a small value and may not be easily observed.



(a)

(b)

Fig. 5. TEM cross-sectional images for (a) a fresh sample and (b) a sample that was stressed for an extended period.

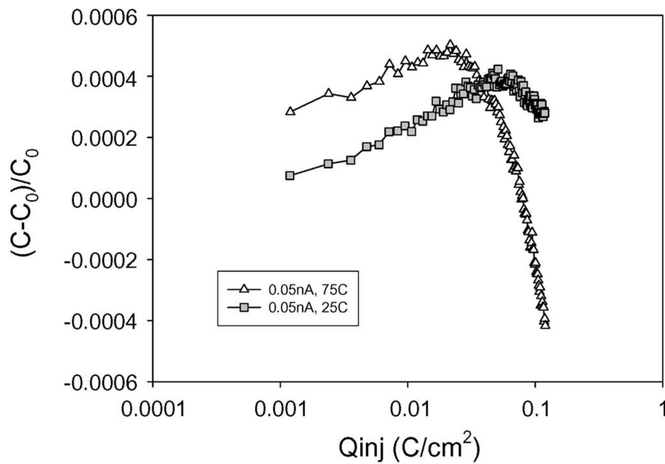


Fig. 6. Dependence of the relative-capacitance variation on the injected charge under a CCS of 0.05 nA at 25 °C and 75 °C.

Experiments that combined both electrical and thermal effects were also performed in this paper. Fig. 6 shows the relationship between the variation in relative capacitance and the injected charge at both 25 °C and 75 °C under a constant stress current of 0.05 nA, where the reversal phenomenon begins earlier at higher temperatures. Temperature tends to enhance trapping and, thus, the dipole number, which leads to a higher capacitance during the variation-increase stage. The temperature also tends to enhance the reaction of the interlayer growth. Therefore, the reversal begins earlier when the temperature is 75 °C as compared with 25 °C.

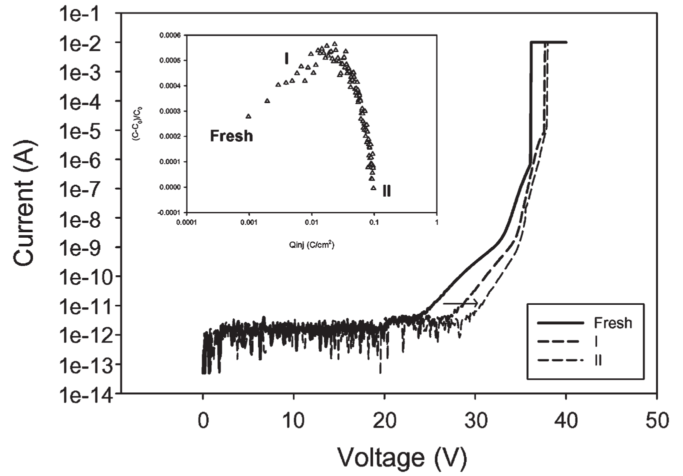


Fig. 7. I–V characteristics of the samples before and after CCS.

In order to identify the charge-trapping behavior in the dielectric at different stages during the stress, the I–V curves were characterized. Fig. 7 shows the I–V curves obtained from both a fresh sample and two stressed samples in the stages both before and after the reversal point. Except for the fresh sample, the samples were stressed under conditions of 0.1 nA at 50 °C. Slightly increasing the temperature can enhance the reversal phenomenon and enlarge the capacitance difference between the samples. The I–V curves can be divided into two regions, which indicates that more than one conduction mechanism exists. This may possibly be the combination of the Pool–Frankel current (at low voltages) and the Fowler–Nordheim tunneling (at high voltages) mechanisms for CVD oxide, as reported in a previous study [7]. The curves are shifted to higher voltages following stress, both at the capacitance-increase stage and at the reversal stage, which indicates a substantial amount of negative charge trapping within the dielectric during stress.

As shown in Fig. 1, the maximum degradation of a single SiO_2 capacitor is about 0.2%. This value implies that mismatch degradation may possibly be an issue for high-precision analog applications. However, the stress conditions used in this paper are not realistic and are much higher than real-use conditions. By extrapolating from Fig. 2, the degradation is expected to be negligible when the stress current is lower than 0.01 nA, corresponding to a current density of 0.17 μA/cm^2. This was verified by performing an extended stress experiment using a stress current of 0.01 nA; its results can be seen in Fig. 1. For standard-use conditions, the applied voltage is usually less than 5 V, and consequently, the stress current is lower than 0.01 nA, as indicated by the I–V characteristics shown in Fig. 7. Furthermore, the ac stress in real-use conditions has an additional adverse effect on charge trapping and sequential degradation. Therefore, the 380-Å SiO_2 MIM capacitor will not be vulnerable to degradation in most normal-use conditions. However, for materials that have more obvious charge-trapping properties, the degradation might be a concern when considering the accuracy of analog functions that require extreme precision.

IV. Conclusion

The degradation of 380-Å SiO_2 MIM capacitors under a wide range of CCS was investigated in this paper. It was observed that differences in behavior occur under both high- and low current-stress conditions, which can be correlated to the onset of impact ionization. Oxide-trapped charges increase local permittivity, thus leading to an increase in capacitance. At lower stress conditions, in capacitors that are able to sustain stress for a longer duration without the oxide breaking down, the degradation reversed after a certain period of time. The decrease in capacitance may arise from a growth in the interlayer between the metal electrode plate and the dielectric. In the experiment combining both electrical and thermal effects, the reversal phenomenon begins earlier at higher temperatures. In most normal-use conditions, the 380-Å SiO_2 MIM capacitor will not be vulnerable to degradation. However, for materials that have more obvious charge-trapping properties, the degradation may be an issue for high-precision analog applications.

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