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(54) RESISTIVE RANDOM ACCESS MEMORY (RRAM) USING STACKED DIELECTRICS AND METHOD FOR MANUFACTURING THE SAME

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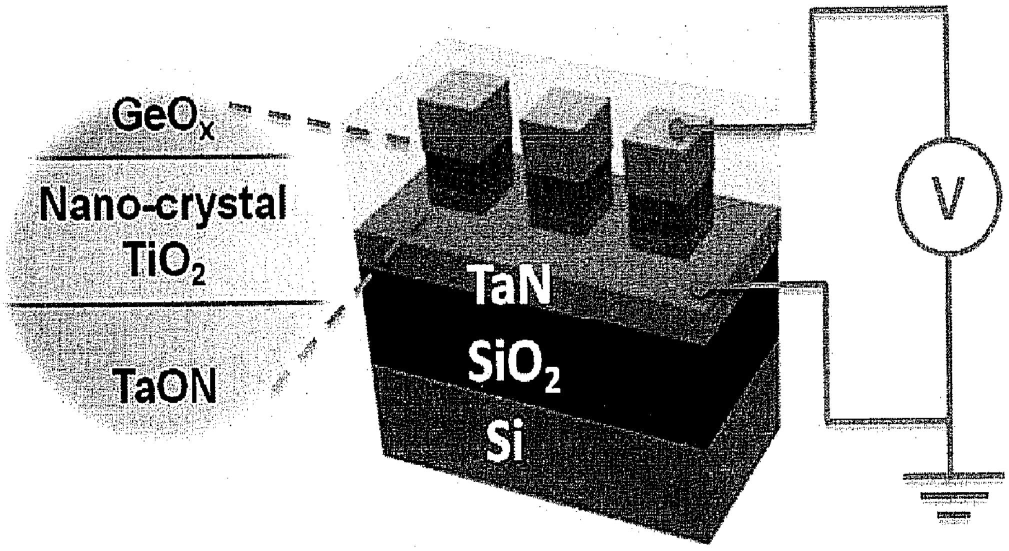
B82Y 30/00	(2011.01)

(52) **U.S. Cl.**

USPC **257/4**; 438/382; 257/E45.003; 977/773; 977/811; 257/E21.645; 257/E21.004

(57) ABSTRACT

Resistive random access memory (RRAM) using stacked dielectrics and a method for manufacturing the same are disclosed, where a setting power of only 4 μW, an ultra-low reset power of 2 nW, good switching uniformity and excellent cycling endurance up to 5×10^9 cycles were achieved simultaneously. Such record high performances were reached in a Ni/GeO_x/nano-crystal-TiO_2/TaON/TaN RRAM device, where the excellent endurance is 4~6 orders of magnitude larger than existing Flash memory. The very long endurance and low switching energy RRAM is not only satisfactory for portable SSD in a computer, but may also create new applications such as being used for a Data Center to replace high power consumption hard discs.



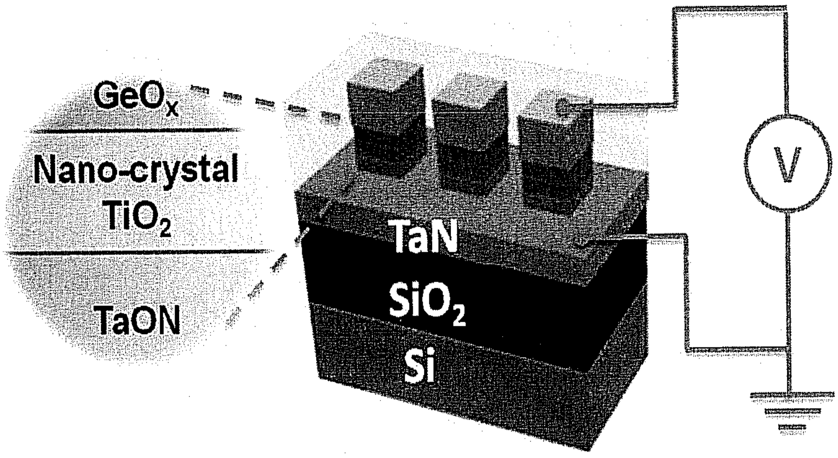

GeOx
Nano-crystal TiO2
TaON
TaN
SiO2
Si
V

Fig. 1(a)

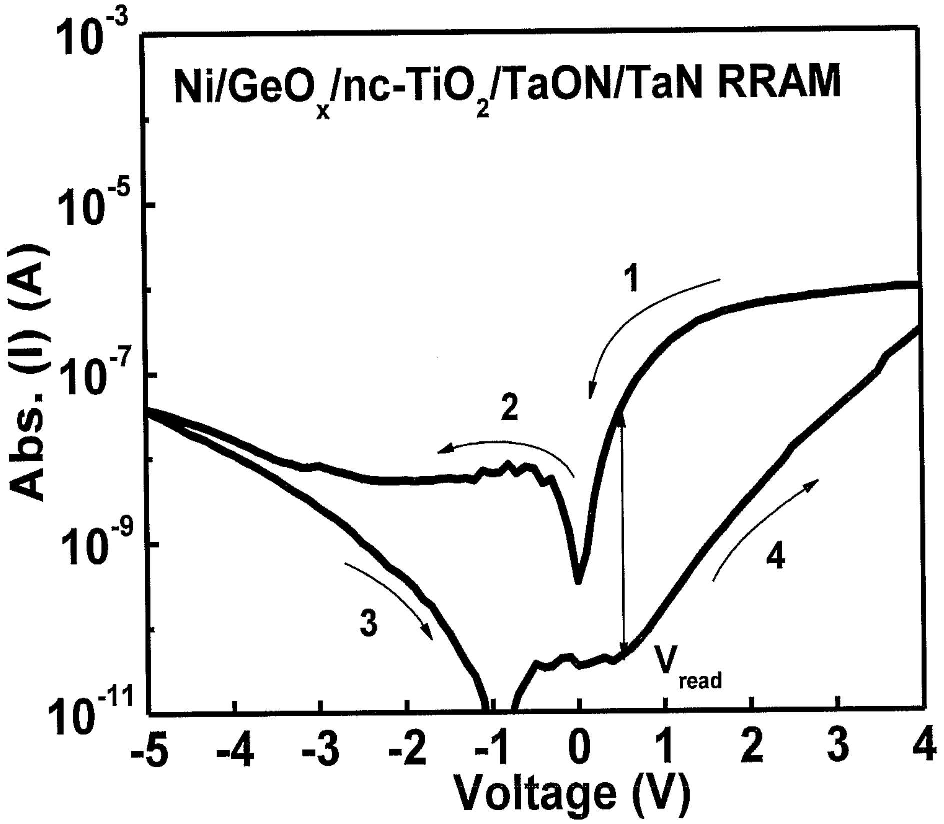

Ni/GeOx/nc-TiO2/TaON/TaN RRAM
Abs. (I) (A)
10-3
10-5
10-7
10-9
10-11
1
2
3
4
Vread
-5
-4
-3
-2
-1
0
1
2
3
4
Voltage (V)

Fig. 1(b)

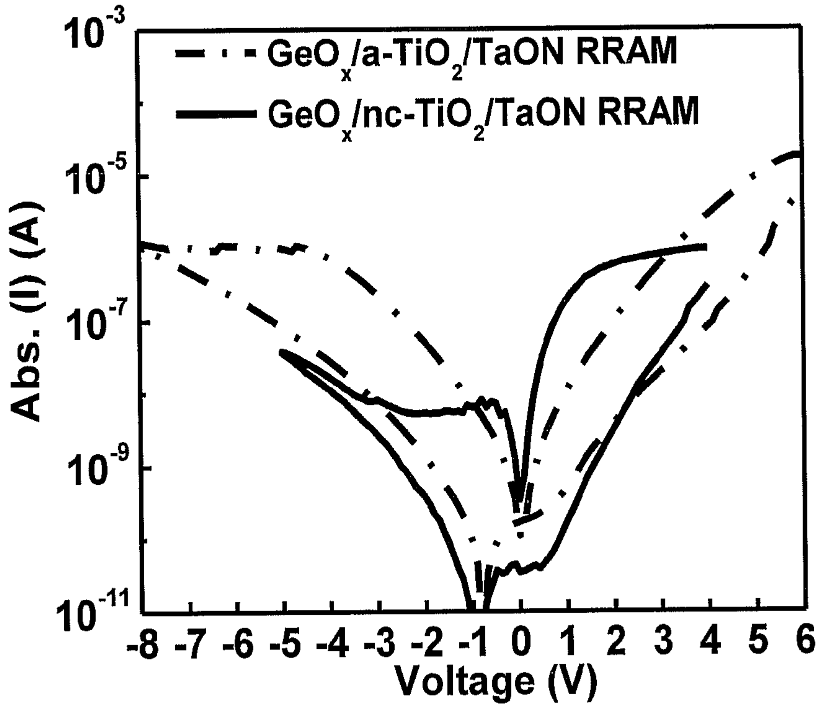

10^{-3}
10^{-5}
10^{-7}
10^{-9}
10^{-11}
Abs. (I) (A)
GeO$_x$/a-TiO$_2$/TaON RRAM
GeO$_x$/nc-TiO$_2$/TaON RRAM
-8 -7 -6 -5 -4 -3 -2 -1 0 1 2 3 4 5 6
Voltage (V)

Fig. 2(a)

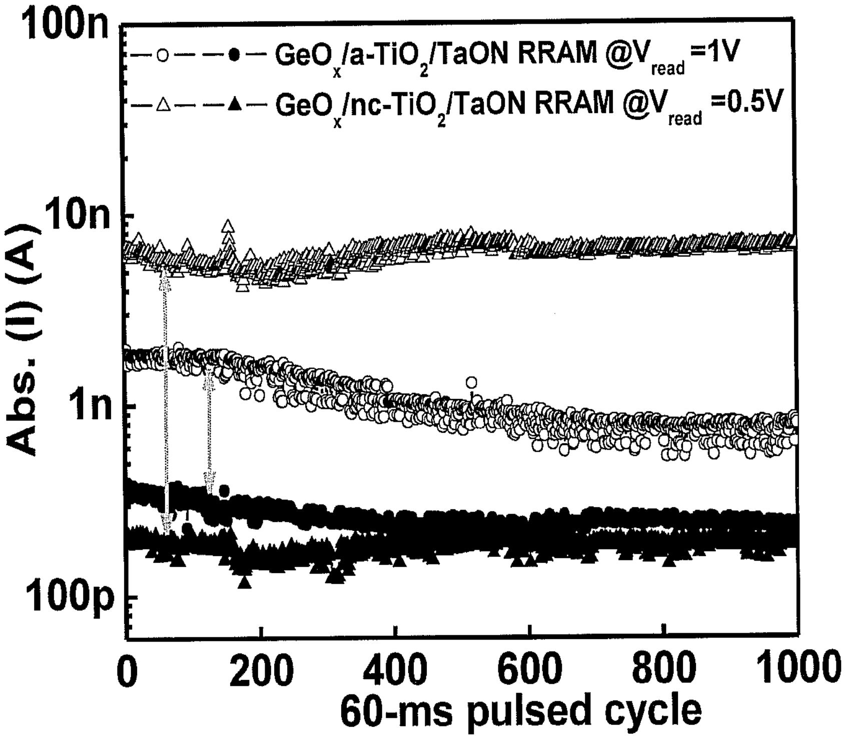

100n
10n
1n
100p
Abs. (I) (A)
GeO$_x$/a-TiO$_2$/TaON RRAM @V$_{read}$=1V
GeO$_x$/nc-TiO$_2$/TaON RRAM @V$_{read}$=0.5V
0 200 400 600 800 1000
60-ms pulsed cycle

Fig. 2(b)

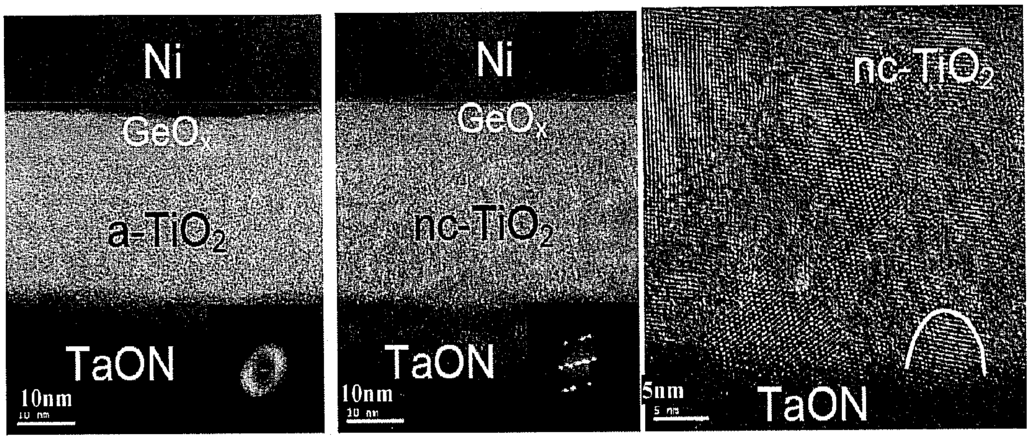

Ni
GeO$_x$
a-TiO$_2$
TaON
10nm
Ni
GeO$_x$
nc-TiO$_2$
TaON
10nm
nc-TiO$_2$
5nm
TaON

Fig. 2(c)

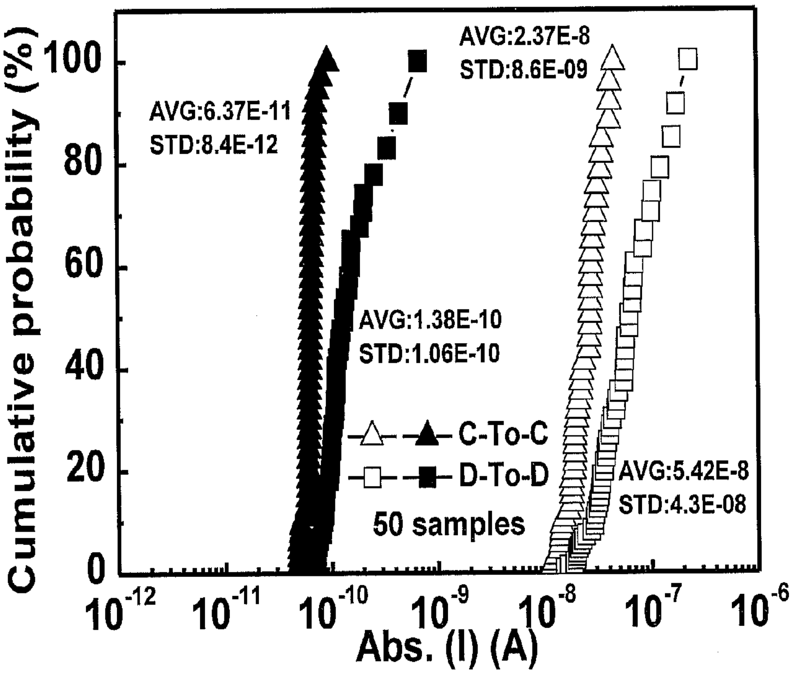

Cumulative probability (%)
0
20
40
60
80
100
10^{-12}
10^{-11}
10^{-10}
10^{-9}
10^{-8}
10^{-7}
10^{-6}
Abs. (I) (A)
AVG:6.37E-11
STD:8.4E-12
AVG:1.38E-10
STD:1.06E-10
AVG:2.37E-8
STD:8.6E-09
AVG:5.42E-8
STD:4.3E-08
C-To-C
D-To-D
50 samples

Fig. 3(a)

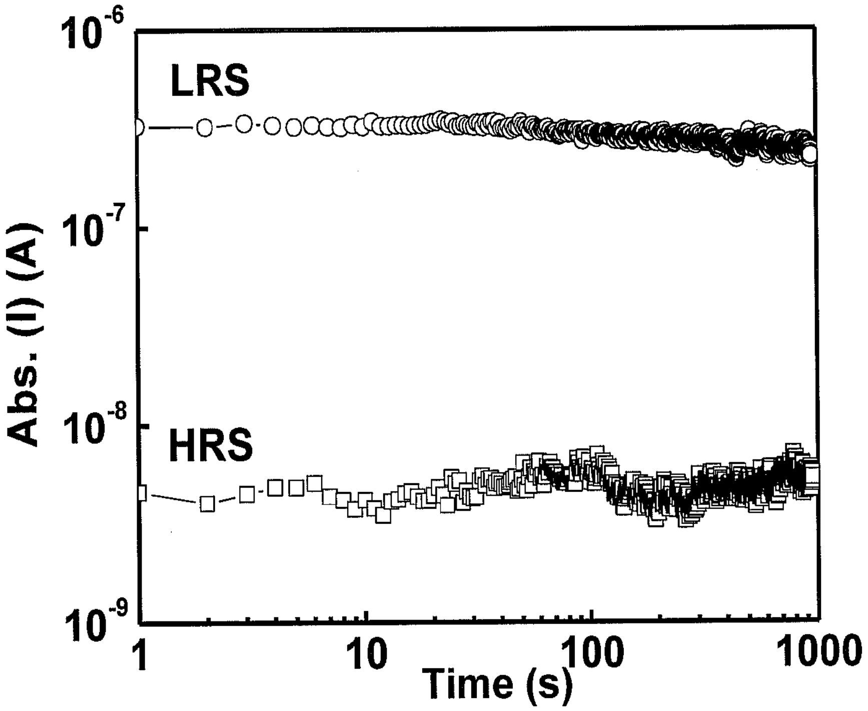

LRS
HRS
10^{-6}
10^{-7}
10^{-8}
10^{-9}
Abs. (I) (A)
1
10
100
1000
Time (s)

Fig. 3 (b)

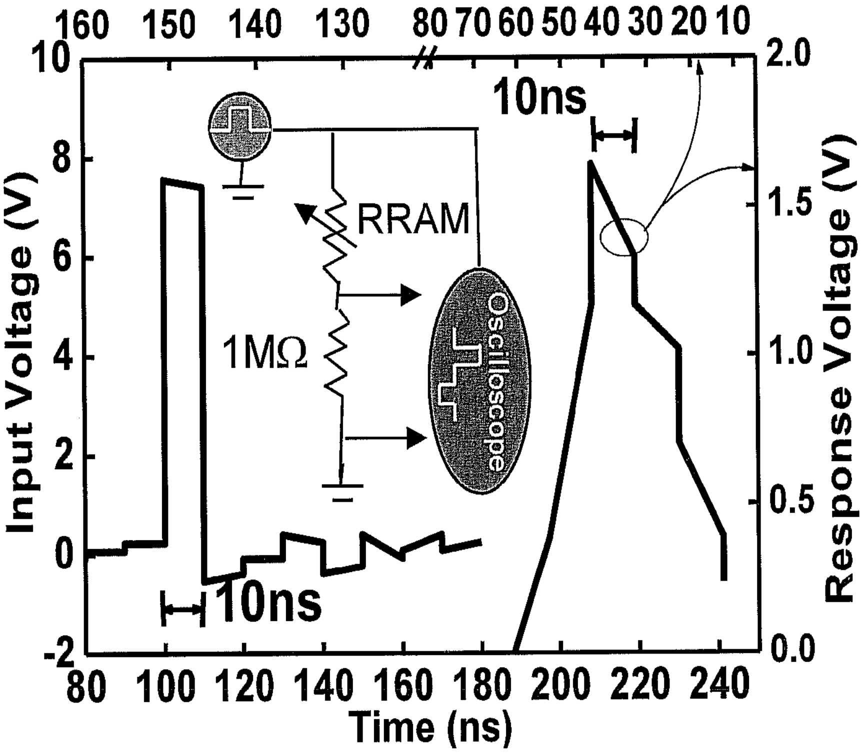

160 150 140 130 80 70 60 50 40 30 20 10
10ns
RRAM
1MΩ
Oscilloscope
10ns
Input Voltage (V)
10
8
6
4
2
0
-2
Response Voltage (V)
2.0
1.5
1.0
0.5
0.0
80 100 120 140 160 180 200 220 240
Time (ns)

Fig. 4(a)

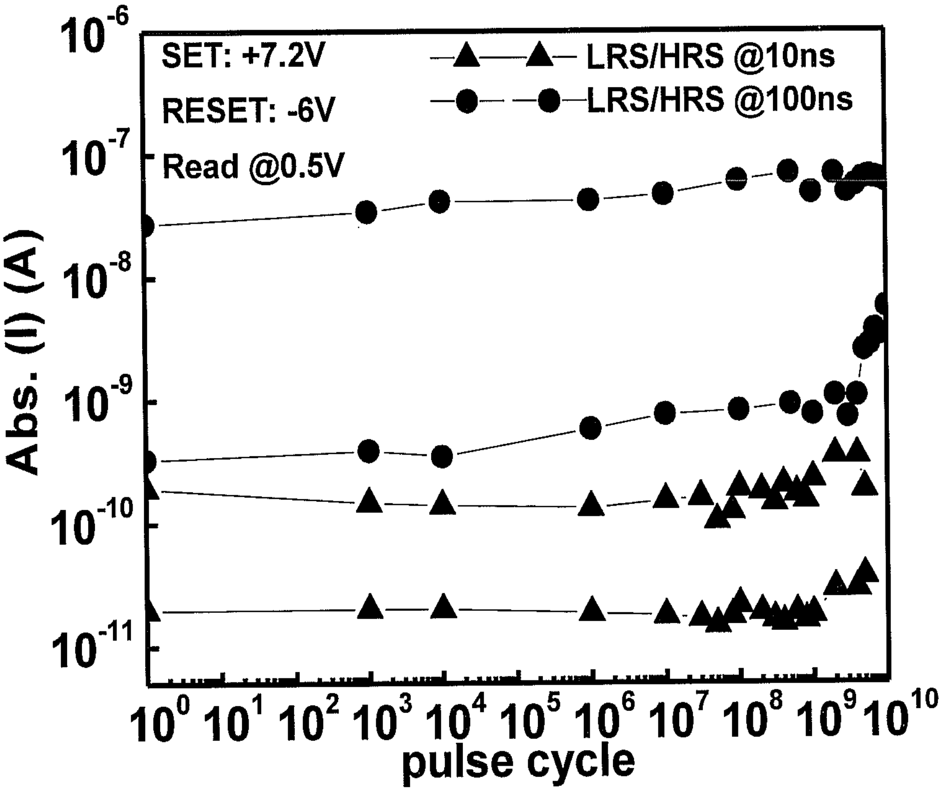

SET: +7.2V
RESET: -6V
Read @0.5V
LRS/HRS @10ns
LRS/HRS @100ns
Abs. (I) (A)
10^-6
10^-7
10^-8
10^-9
10^-10
10^-11
10^0 10^1 10^2 10^3 10^4 10^5 10^6 10^7 10^8 10^9 10^10
pulse cycle

Fig. 4(b)

RESISTIVE RANDOM ACCESS MEMORY (RRAM) USING STACKED DIELECTRICS AND METHOD FOR MANUFACTURING THE SAME

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a resistive random access memory (RRAM) and method for manufacturing the same and, in particular, to a PRAM with a metal-insulator-metal (MIM) structure, using stacked dielectrics of semiconductor-oxide/nano-crystal (nc) metal-oxide/metal-oxynitride, and different work-function top and bottom electrodes. The RRAM device is implemented in stacked dielectrics of GeO_x/nc-TiO_2/TaON with low cost top (Ni) and bottom (TaN) electrodes. This RRAM device has special merits of ultra-low sub-100 fJ switching energy, tight distributions of set/reset currents and extremely long endurance of 5×10^9 cycles simultaneously.

[0003] 2. Description of the Prior Art

[0004] According to International Technology Roadmap for Semiconductors (ITRS) at www.itrs.net, Flash Non-Volatile Memory (NVM) will continue to scale down into sub-20 nm, by replacing the current poly-Si Floating-Gate (FG) with SiN Charge Trapping (CT) structure. However, the degraded endurance from 10^5 to 10^4 program/erase cycles is a fundamental physics limitation due to the smaller amount of charges stored in the sub-20 nm cell size. Such degraded endurance is unsuitable for high-end products such as solid-state drive (SSD), and therefore new NVM devices should be developed. To address this issue, non-charge-based resistive random access memory (RRAM) has attracted much attention, and the simple cross-point structure is more suitable for embedded NVM applications and low-cost three-dimensional (3D) integration. However, high set/reset currents, high forming power, wide set/reset margin and poor endurance are difficult challenges for RRAM.

SUMMARY OF THE INVENTION

[0005] The present invention reveals a novel high endurance and ultra-low switching power RRAM device, with a setting power of only 4 μW, an ultra-low reset power of 2 nW, a large resistance window >50x, good switching uniformity, and excellent cycling endurance up to 5×10^9 cycles, all achieved simultaneously. Such record high performances were reached in a Ni/GeO_x/nc-TiO_2/TaON/TaN RRAM device, where the excellent endurance is 4~6 orders of magnitude larger than existing Flash memory. The low switching energy and very long endurance RRAM is not only satisfactory for portable SSD in a computer, but may also create new applications such as being used for a Data Center to replace high power consumption hard discs.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] FIG. **1**(*a*) is a schematic illustration of the RRAM and FIG. **1**(*b*) illustrates a measured swept I-V curve of Ni/GeO_x/nc-TiO_2/TaON/TaN RRAM devices;

[0007] FIG. **2**(*a*) illustrates swept I-V curves, FIG. **2**(*b*) illustrates resistive switching behaviors under 60 ms set/reset stress cycles, and FIG. **2**(*c*) are cross-sectional TEM images of Ni/GeO_x/TiO_2/TaON/TaN RRAM with nc-TiO_2 or control amorphous-TiO_2 layer;

[0008] FIG. **3**(*a*) illustrates current distributions and FIG. **3**(*b*) illustrates disturbance characteristics of Ni/GeO_x/nc-TiO_2/TaON/TaN RRAM;

[0009] FIG. **4**(*a*) illustrates an extracted voltage waveform of a fixed 1 Mega-ohm resistor connected to the RRAM device at a fast speed of 10 ns; and FIG. **4**(*b*) illustrates set/reset endurance characteristics at a 10 ns or 100 ns switching pulse of Ni/GeO_x/nc-TiO_2/TaON/TaN RRAM.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0010] The RRAM devices were integrated into VLSI backend for embedded memory application. First, a 200-nm-thick backend SiO_2 layer was formed on the Si substrates. The 100 nm TaN layer was deposited by sputtering. After patterning the bottom TaN electrode, the 24-nm-thick TaON film was deposited and followed by oxygen annealing. Then the 26-nm-thick TiO_2 film was deposited on TaGN/TaN, where the crystallinity of TiO_2 was measured by transmission electron microscopy (TEM) using fast Fourier transition (FFT) technique. An amorphous-TiO_2 control sample was also fabricated for performance comparison. After that, a 6-nm-thick GeO_x layer was covered to form the stacked dielectrics of GeO_x/TiO_2/TaON. Finally, a 50-nm-thick Ni layer was deposited and patterned to form the top electrode by a metal mask.

[0011] FIG. **1**(*a*) is a schematic illustration of the Ni/GeO_x/nc-TiO_2/TaON/TaN RRAM. FIG. **1**(*b*) is a measured swept I-V curve of Ni/GeO_x/nc-TiO_2/TaON/TaN RRAM devices. Good resistive switching characteristics were measured, where a large resistance window of >100X at 0.5 V was obtained. In addition to the free-forming and self-compliant operation, the RRAM of the present invention can be set to a low resistance state (LRS) at an ultra-low power of 4 μW (1 μA at 4 V) and reset to a high resistance state (HRS) at a very low power of only 2 nW (−0.4 nA at −5 V). The nc-TiO_2 (nano-crystal TiO_2) plays an important role to reach low switching power in RRAM. FIGS. **2**(*a*), **2**(*b*) and **2**(*c*) show swept I-V curves, resistive switching behaviors under 60 ms set/reset stress cycles, and cross-sectional TEM images of Ni/GeO_x/TiO_2/TaON/TaN RRAM, respectively, where different nc-TiO_2 or amorphous-TiO_2 in RRAM devices were used for comparison. Although a similar I-V switching behavior can be observed, the control device with amorphous-TiO_2 needs larger set and reset voltages of 6 V and −8 V, respectively. Besides, significantly higher switching currents for set (18 μA) and reset (1.2 μA) were found in the RRAM device with amorphous-TiO_2 than those with nc-TiO_2. The distributions of resistance states are an important concern for RRAM. FIG. **3**(*a*) shows the current distributions of Ni/GeO_x/nc-TiO_2/TaON/TaN RRAM, where very tight current distributions for both LRS and HRS were reached. The excellent switching uniformity (both cycle-to-cycle and device-to-device) is linked to the low power operation with low set/reset currents and self-compliance, which is significantly better than a conventional RRAM using metallic filament conduction. The switching speed is a key factor for RRAM. To address the issue of whether low switching power may cause read disturbances in RRAM, the RRAM devices were subjected to constant voltage stress (CVS) at a different read bias for 1000 sec. As shown in FIG. **3**(*b*) (disturbance characteristics of Ni/GeO_x/nc-TiO_2/TaON/TaN RRAM), stable LRS and HRS values can be maintained at a 0.5 V read voltage for 1000 sec, which is equivalent to 10^{10} reading cycles at a 100 ns pulse. The negligible read disturbance for LRS is because the read voltage is 8 times lower than the set voltage, while the voltage polarity for reset is different from the read voltage.

[0012] FIG. **4**(*a*) shows the switching response of an input voltage applied on a fixed 1 M-ohm external resistor connected to the RRAM. Fast switching response is measured at the applied over-stressed set pulse of 10 ns, where the distorted output waveform is due to parasitic capacitance and bonding wire. Such fast switching capability is only measured in Ni/GeO_x/TiO_2/TaON/TaN RRAM with nc-TiO_2 but not amorphous-TiO_2 devices. Endurance is also a severe limiting factor for conventional metallic filament RRAM. FIG. **4**(*b*) shows the measured endurance characteristics under an over-stressed set pulse of 7.2 V and reset pulse of −6 V for 10 and 100 ns. Stable switching with a nearly constant HRS/LRS ratio is obtained for extremely long 5×10^9 set/reset cycles, with ultra-low sub-100 or sub-10 fJ switching energy. Such excellent endurance is ascribed to the fast switching speed, low switching power, easy hopping via grain boundaries, and higher-κ nc-TiO_2 (κ.>40) to lower stress electrical field. FIG. **4**(*c*) shows the measured cycling characteristics as a function of over-stressed voltage with a longer 60-ms pulse. The measured 5×10^4 cycles guarantees more than 10^{10} cycles using a faster 100 ns pulse, which is consistent with measured data in FIG. **4**(*b*).

[0013] According the experiment data above, the Ni/GeO_x/nc-TiO_2/TaON/TaN RRAM device of the present invention has only a 4 μW setting power, an ultra-low reset power of 2 nW, a large resistance window of >50X, good switching uniformity, and an excellent cycling endurance up to 5×10^9 cycles. The excellent endurance is 4~6 orders of magnitude larger than existing Flash memory. The very long endurance and ultra-low switching energy RRAM is not only sufficient for portable SSD in a computer, but may also create new applications such as being used for a Data Center to replace high power consumption hard discs.

[0014] The preferred embodiment mentioned above is only for illustrative purposes, and any RRAM which is formed by Metal-Insulator-Metal (MIM) structure or based on the Metal-Insulator-Semiconductor (MIS) structure, should be regarded as the same as the embodiment disclosed. Also, the dielectric materials can be selected from the semiconductor oxide of GeO_2, SiO_2, metal-oxide of SnO_2, Al_2O_3, HfO_2, ZrO_2,TiO_2, CeO_2, NiO, Ta_2O_5, ZnO, WO, CuO_2, $SrTiO_3$, and related oxynitride thereof. The material of the electrodes can be selected from metal, metal-nitride, or conductive metal-oxide of Ta, TaN, Ti, TiN, W, WN, MoN, Al, Ni, Ir, Pt, Ru, Ag, Cu, Au, and ITO (Indium Tin Oxide). The nano-crystal (nc) metal oxide or metal-oxynitride such as TiO_2, TiON, Ta_2O_5, TaON, etc can be formed by any one of furnace annealing, RTA, laser annealing, and in-situ annealing in PVD/CVD systems.

1. A resistive random access memory (RRAM) using stacked dielectrics, wherein the RRAM is formed by stacked dielectrics composited of semiconductor-oxide, nano-crystal (nc) metal-oxide, and metal-oxynitride.

2. A RRAM using stacked dielectrics, wherein the RRAM is formed by Metal-Insulator-Metal (MIM) structure or based on the Metal-Insulator-Semiconductor (MIS) structure.

3. The resistive random access memory (RRAM) using stacked dielectrics as claimed in claim **1**, wherein the RRAM further includes top and bottom electrodes having different work functions.

4. The RRAM using stacked dielectrics as claimed in claim **1**, wherein the material of the dielectrics is selected from oxides such as GeO_2, SiO_2, SnO_2, Al_2O_3, HfO_2, ZrO_2, TiO_2, CeO_2, NiO, Ta_2O_5, ZnO, WO, CuO_2, $SrTiO_3$ or related oxynitride thereof.

5. The RRAM using stacked dielectrics as claimed in claim **2**, wherein the material of the dielectrics is selected from semiconductor-oxide oxides such as GeO_2, SiO_2, metal-oxide of SnO_2, Al_2O_3, HfO_2, ZrO_2, TiO_2, CeO_2, NiO, Ta_2O_5, ZnO, WO, CuO_2, $SrTiO_3$, or related oxynitride thereof.

6. The RRAM using stacked dielectrics as claimed in claim **3**, wherein the material of the electrodes is selected from metal, metal-nitride, and conductive metal-oxide of Ta, TaN, Ti, TiN, W, WN, MoN, Al, Ni, Ir, Pt, Ru, Ag, Cu, Au, and Indium Tin Oxide (ITO).

7. The RRAM using stacked dielectrics as claimed in claim **2**, wherein the material of the metal is selected from Ta, TaN, Ti, TiN, W, WN, MoN, Al, Ni, Ir, Pt, Ru, Ag, Cu, Au, and Indium Tin Oxide (ITO).

8. A method for manufacturing RRAM with stacked dielectrics, wherein nano-crystal (nc) metal oxides such as TiO_2, Ta_2O_5, HfO_2, ZrO_2, ZnO, $SrTiO_3$ are formed by at least one of furnace annealing, RTA, laser annealing, and in-situ annealing in PVD/CVD systems.

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