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Dual-metal-gate-integration complementary metal oxide semiconductor process scheme using Ru positive-channel metal oxide semiconductor and TaC negative-channel metal oxide semiconductor gate electrodes

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This article presents the development of a wet removal process on the integration of complementary metal oxide semiconductor (CMOS) dual metals with Ru for positive-channel metal oxide semiconductor and TaC for negative-channel metal oxide semiconductor on high-k HfO_2 gate dielectric. The integration scheme focused on the wet etching capability for the first metal and the selectivity control on the high-k dielectrics under the metal gate. Using the developed chemical, ceric ammonium nitrate and nitric acid mixture used for Ru metal removal and HfO_2 treated with Ar/O_2 plasma by selective diluted hydrofluoric wet etching, a CMOS dual-metal-gate structure was achieved with satisfactory device fabrication.
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I. INTRODUCTION

The complementary metal oxide semiconductor (CMOS) dual-metal-gate process on bulk Si with two metal gate materials using a gate-first approach is the main stream of present integration methodology. The candidate metals for both positive-channel metal oxide semiconductor (PMOS) and negative-channel metal oxide semiconductor (NMOS) rely on a proper integration scheme to implement on the Si wafer. According to the International Roadmap for Semiconductors,[1] the introduction of high dielectric constant (high-k) gate materials and dual-metal-gate electrodes with appropriate work functions is demanded in the near future to reduce the gate direct tunneling leakage current[2–6] and to eliminate boron (B) penetration and polydepletion effect when the device scaling down is below 65 nm. In order to optimize the threshold voltage (V_t) in high performance devices, a metal gate with tunable work function, about 4.1–4.6 eV for NMOS and about 4.8–5.1 eV for PMOS devices, is required for advanced transistor structures such as fin field effect transistors or ultrathin-body metal oxide semiconductor field effect transistors.[7–9] Several approaches have been proposed, including a full silicided (FUSI) metal gate,[10–13] a midgap metal gate, and dual metal gates in CMOS integration.[14–21] FUSI is an extension of self-aligned silicide technology that has been widely used in CMOS devices. In a FUSI process, the poly-Si gate is totally silicided with the metal. The major advantage of the FUSI method is a CMOS compatible process integration. Among common silicides reported, NiSi FUSI has been demonstrated to have the best work function *tunability* and stable silicide/gate oxide interface. However, NiSi has the poorest thermal stability and thermal treatment prior to silicidation process results in the incomplete elimination of boron penetration in p-channel device.[22] Since the work function of the metal salicide cannot be modulated, a straightforward dual metal gate on the high-k dielectric CMOS process is hence proposed for N+- and P+-like gates in the 90 nm node or below. A versatile integration scheme has been developed which employs a wet etch process to remove the first metal selectively before depositing the second metal. Zhang *et al.* reported TaSiN (NMOS) and Ru (PMOS) on HfO_2, utilizing a TaSiN wet etch then following a dual-metal-gate dry etching process to fabricate the 85 nm devices.[17] Lu *et al.* and Samavedam *et al.* demonstrated Ti (NMOS), Mo (PMOS), TaSiN (NMOS), TiN (PMOS) dual-metal-gate integration on Si_3N_4, and HfO_2 gate dielectrics via the wet etching process, respectively.[18,19]

The semiconductor industry is feverishly investigating high-k materials with a low equivalent oxide thickness (EOT) for the gate stack to replace SiO_2 or SiON due to unacceptable leakage current when EOT is further scaled down. At present, the dielectric films based on hafnium oxides such as HfO_2, HfAlO, HfSiO, HfON, and HfSiON are the leading contenders. There are also integration issues as depositing thin stoichiometric layers with acceptable electrical properties and then removing the high-k gate oxide without damaging the source and drain areas. Recently, plasma etching on HfO_2 gate dielectric was investigated[23,24] and ion implantation was found to enhance wet chemical etching of HfO_2.[25] However, further study is required on the etch selectivity of HfO_2 over Si substrate for the integrated process control.

In this article, we demonstrate a dual-metal-gate CMOS flow with Ru (PMOS) and TaC (NMOS) on HfO_2. This flow utilizes a Ru wet etching process that is highly selective to high-k dielectric and a post-dual-metal-gate dry etching stop

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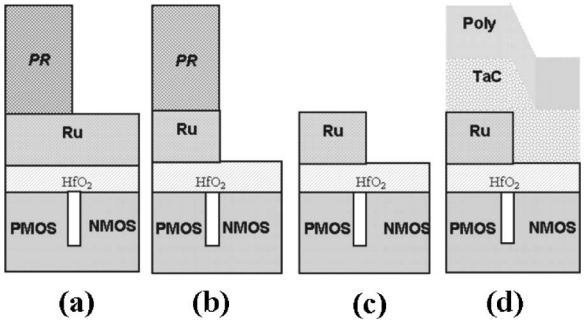

FIG. 1. CMOS dual-metal-gate fabrication integrates process flow: (a) NMOS define with photoresist, (b) first metal wet etch, (c) photoresist strip, and (d) second metal and polydeposition.

on HfO_2, then with Ar/O_2 plasma treatment and diluted hydrofluoric (HF) (H_2O:49% HF=100:1) (DHF) wet etching process to subsequently remove the high-*k* dielectric to fabricate the 75 nm devices. The etching characteristics of the HfO_2 film with inductively coupled plasma based on the mechanism of ion energetic reactions and ion bombardment in Ar/O_2 were studied. Etching behaviors of various HfO_2 films in DHF solution were also investigated.

II. EXPERIMENTAL DETAILS

A metal wet etching module shown in Fig. 1 was incorporated into the conventional CMOS flow to fabricate Ru and TaC dual-metal-gate CMOS transistors. The high-*k* HfO_2 dielectrics about 2 nm thick was deposited first by atomic layer chemical vapor deposition at 350–400 °C then annealed in N_2 ambient at 700 °C, followed by physical vapor deposition (PVD) of about 10 nm the first metal (Ru) for PMOS transistor electrode. A mask was used to define the PMOS then patterned with *I*-line (365 nm) photoresist which served as a protection layer at the PMOS area during the first metal wet removal. A solution containing ceric ammonium nitrate ($(NH_4)_2Ce(NO_3)_6$) and nitric acid (HNO_3) mixture was applied for Ru metal to selectively remove from the NMOS area without damaging the photoresist and the high-*k* underlayer. The photoresist was then removed by amine base chemistry. Afterwards, the second metal (TaC) was deposited by PVD process, followed with a 150 nm polycapped with a tetraethoxysilane (TEOS) hard mask deposition. ArF (193 nm) photoresist was used to define the 75 nm gate length. The chlorine (Cl_2) based chemistry was used for the TaC metal film etching, followed with an oxygen (O_2) based chemistry for the Ru film etching in a Lam etcher TCP-9400. During the Ru dry etching process, the HfO_2 layer served as an etching stop to control the NMOS/PMOS

TABLE I. Selectivity control of chemicals for Ru wet removal.

Wet etching solution	Ru etching rate (nm/min)	HfO_2 etching rate (nm/min)
$(NH_4)_2Ce(NO_3)_6$:HNO_3=6:1	70	0.06
$(NH_4)_2Ce(NO_3)_6$:HNO_3=50:1	20	0.007

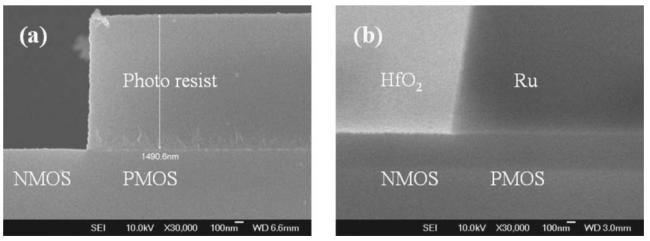

FIG. 2. SEM observation of photoresist removed by solvent: (a) before photoresist removal and (b) after photoresist removal.

area loading. A subsequent DHF wet etching solution was used to remove the high-*k* dielectric with minimum Si substrate loss to achieve the device requirement.

To characterize the dual metal gate on the high-*k* dielectric gate structure, the stoichiometry, texture, phase, and etching rate of Ru on HfO_2 were examined by x-ray photoelectron spectroscopy (XPS, VG Microlab-350), x-ray diffraction (XRD, PANalytical X'pert Pro-MRD) with Cu K_α radiation, scanning electron microscopy (SEM, JEOL 6700F) operating at 10 keV, and transmission electron microscope (TEM, Philips CM-200) operating at 200 keV, respectively. The cross-sectional TEM (XTEM) samples were prepared by focus ion beam (FIB, FEI 235) operating at 30 kV with a gallium (Ga) source and thinned to about 0.1 μm in thickness.

III. RESULTS AND DISCUSSION

The key process required for a dual-metal-gate integration relies on the successful wet removal of the first metal (Ru) without damaging the high-*k* HfO_2 underlayer. In this study, with suitable adjustment of ceric ammonium nitrate/nitric acid ratio, the selectivity of Ru to HfO_2 could be controlled over 2800 without HfO_2 loss after 10 nm Ru metal removal (see in Table I). The capability of photoresist to protect the PMOS area was also one of the critical factors which must resist the wet etch during the Ru removal and should be removed easily after the first metal removal. Traditional O_2 plasma dry stripping is known to cause the damage when the HfO_2 dielectric surface is exposed during photoresist stripping. As shown in Figs. 2 and 3, amine based wet chemical stripping plays an important role as it removes the photore-

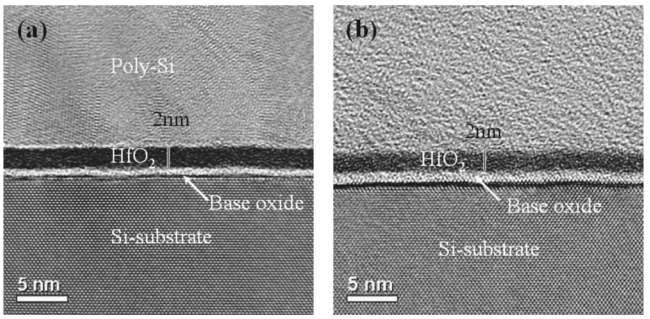

FIG. 3. High-resolution TEM inspection of HfO_2 thickness after Ru etching: (a) deposited film subjected to post-700 °C annealed and (b) after PR removal.

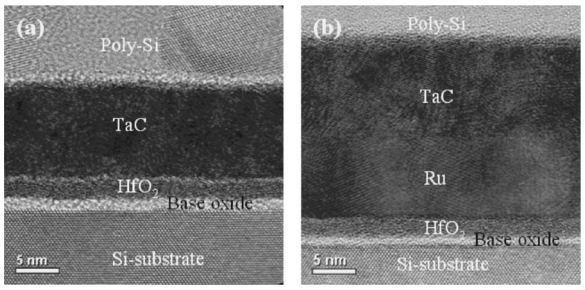

FIG. 4. Post second metal deposition: (a) NMOS:TaC/HfO_2 and (b) PMOS:TaC/Ru/HfO_2.

sist only but has no damage to the high-*k* dielectric. Post second metal and polydeposition indicated that the dual-metal-gate stack of NMOS/PMOS areas is well defined in this integration scheme, as shown Fig. 4. These high-resolution XTEM micrographs evidence that the interface between TaC and HfO_2 is free of interfacial contamination. This indicates that the Ru wet etching with such scheme is suitable for the dual-metal-gate integration.

For NMOS/PMOS profile control during dual gate etching step, the proposed HfO_2 etching was carried out by using the DHF wet removal method instead of dry plasma etching for the lower Si substrate damage and recess control. Before the high-*k* dielectric HfO_2 wet removal, a high selectivity etching gas (Ar/O_2) was applied for PMOS area Ru dry etching and stopping on the HfO_2 layer, as shown in Fig. 5. Both NMOS and PMOS were well controlled to stop on the high-*k* dielectric layer after dry etching of Ru with Ar/O_2. In this study, by properly controlling the radio frequency (rf) bias power during Ru metal dry etching step and the extended over etching time with Ar/O_2 plasma bombardment could be contributed to remove the HfO_2 layer with DHF solution. The O_2 gas that provided high etching selectivity of Ru metal and stopped on the HfO_2 layer that followed extended overetching Ar/O_2 plasma implants of O ion through HfO_2 into substrate resulted in faster DHF etching benefit. In practice, Fig. 6 reveals that the threshold rf bias power over 70 W is required to remove HfO_2 film through the pretreatment condition of Ar/O_2 plasma bombardment for 90 s. In fact, that the bias power is related to ion plasma treated time combined sufficient energy for 4 nm HfO_2 film bombardment. The results shown in Fig. 6 also indicate that Si recess after post-DHF wet etching is controllable by rf bias power during Ar/O_2 plasma bombardment of HfO_2 film surface treatment.

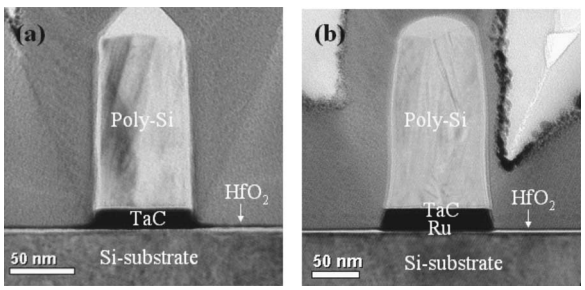

FIG. 5. Post-dual-metal-gate etched stop on HfO_2: (a) NMOS:TaC/HfO_2 and (b) PMOS:TaC/Ru/HfO_2. The gate surfaces are passivated with oxide, Pt–Pd, and carbon coating for XTEM specimen fabrication with FIB.

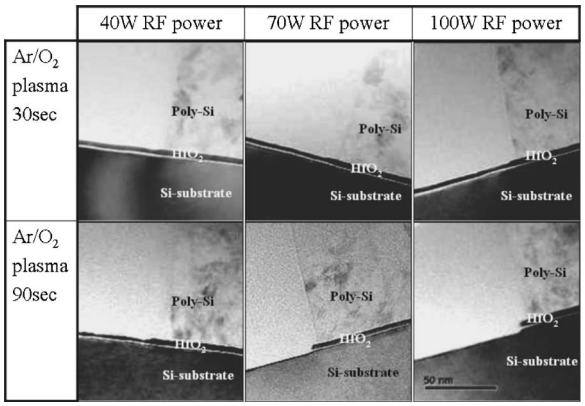

FIG. 6. Correlation between bombardment parameters and HfO_2 was removed in 100:1 diluted HF solution for 60 s. The HfO_2 films are examined with 4 nm thickness.

Four postsurface treatments for HfO_2 films, e.g., 500 and 700 °C annealing in N_2 ambient, Ar/O_2 plasma bombardment, and Ar/O_2 bombardment followed by 700 °C annealing, were examined so as to identify their effects on DHF etching rate. As shown in Fig. 7, the increase of annealing temperature reduces the etching rate of HfO_2 film in DHF solution. This indicates that the etching rate decreases with the improvement of crystallinity of HfO_2 film. Such a result is confirmed by XRD analyses shown in Fig. 8 which shows that the crystallinity of annealed HfO_2 film is better than that of plasma bombarded films. Furthermore, due to the amorphism generated by the plasma bombardment, the Ar/O_2 bombarded HfO_2 film hence possesses the fastest etching rate in comparison with the HfO_2 films subjected to other treatments. However, the plasma bombarded HfO_2 became difficult to be etched away by DHF solution after a subsequent 700 °C anneal which caused the recrystallization of HfO_2 film. The Ar/O_2 plasma bombardment induces physical transformation in HfO_2 film that may accelerate the remedy of crystallinity of HfO_2 film during subsequent thermal treatment. The HfO_2 film subjected to Ar/O_2 bombardment

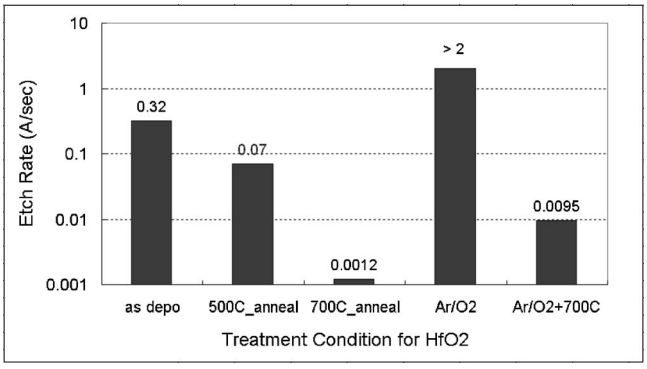

FIG. 7. 100:1 dilute HF etching rate on HfO_2 subjected to Ar/O_2 treatment.

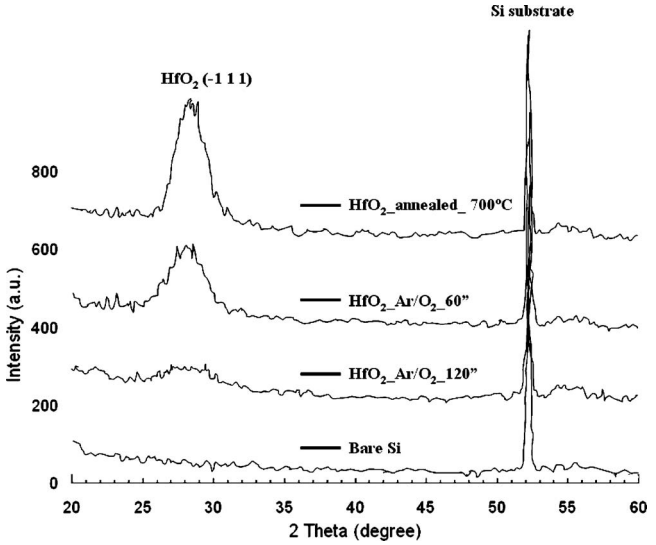

FIG. 8. XRD intensity ratio analysis of HfO_2 after Ar/O_2 bombarded treatment. The amorphous HfO_2 phase increased after Ar/O_2 plasma bombardment.

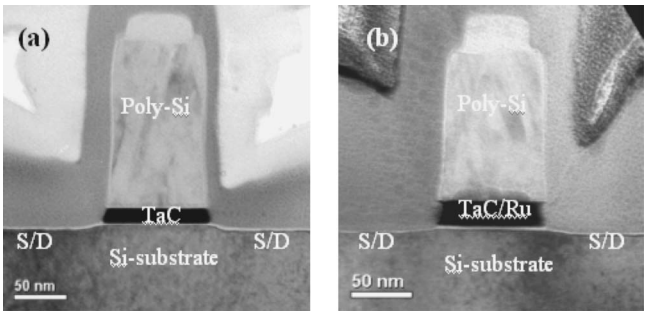

FIG. 10. Post-HfO_2 etching with 100:1 dilute HF solution for 60 s: (a) NMOS: TaC/HfO_2 and (b) PMOS: TaC/Ru/HfO_2.

followed by 700 °C annealing hence exhibits the lowest etching rate in DHF solution. Hence, not only plasma treatment time but also rf bias power benefits from complete physical transformation resulting in a near completely amorphous HfO_2 film which can be completely removed by DHF solution.

To get a complete look at the differences between the two HfO_2 films which are annealed with 700 °C and post-Ar/O_2 plasma treatment, the high-resolution regions of O 1*s* and Hf 4*f* were examined. According to the result of XPS analyses of annealed and Ar/O_2 plasma bombarded HfO_2 films shown in Fig. 9, the O 1*s* subpeak at 534.2 eV disappears after Ar/O_2 bombardment whereas the O to Hf atomic concentration ratio increased followed by O ion implementation, suggesting the occurrence of phase transition. The atomic concentration ratio was calculated from the photoelectron peak areas by subtracting a linear-type background. In addition, a correlation with XRD confirmed that the HfO_2 films are amorphousized by Ar/O_2 plasma bombardment due to phase transition and benefited by DHF etching. The Ar/O_2 plasma processing contributes to chemical shift of O 1*s* spectra from high bonding energy peak of crystalline shifted to lower bonding energy peak of amorphous HfO_2. Again, this indicates that the amorphism of high-*k* HfO_2 dielectrics subjected to Ar/O_2 plasma bombarded film benefits its wet etching in DHF solution. Both NMOS and PMOS gate profiles are shown in Fig. 10; those high-*k* HfO_2 films under gate are defined by following with pretreatment condition of Ar/O_2/90 s under 70 W rf bias power then post-HfO_2 etched by 100:1 dilute HF for 60 s. The source-drain area gate poly, metal, and high-*k* dielectric layers are successfully defined by this dual-metal-gate process scheme.

IV. CONCLUSIONS

The dual-metal-gate CMOS devices are demonstrated with Ru and TaC gate electrodes on high-*k* HfO_2 Key process modules such as a highly selective metal wet etching

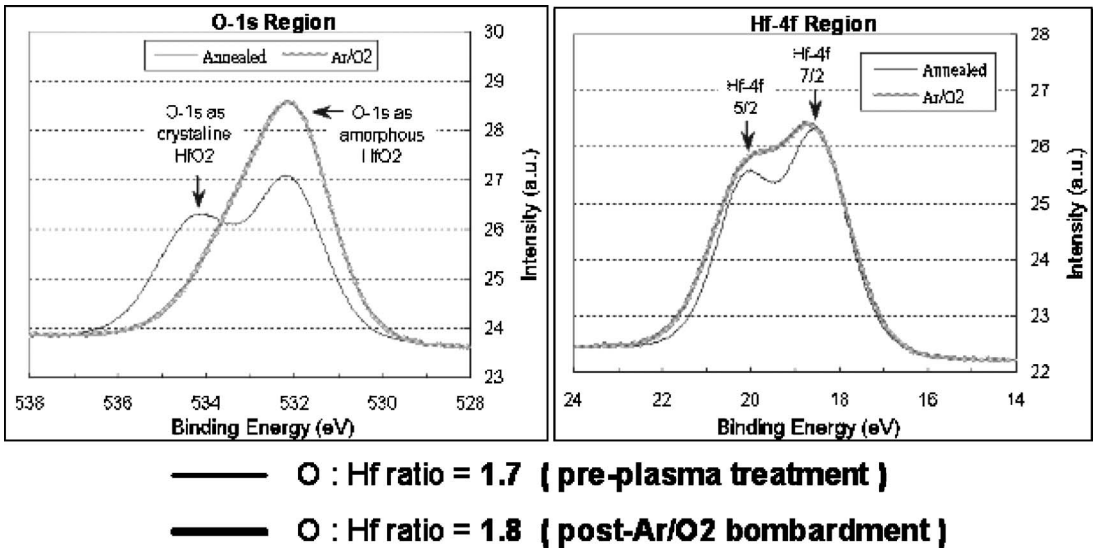

FIG. 9. XPS Hf 4*f* and O 1*s* spectra from annealed and Ar/O_2 plasma bombarded HfO_2. The O/Hf atomic ratio increased after Ar/O_2 plasma bombardment.

and dual-metal-gate plasma bombardment combined with wet etch process have been developed. The ceric ammonium nitrate and nitric acid mixture is used for Ru metal removal with highly selective control on the high-k HfO_2 Moreover, the HfO_2 treated with appropriate bias power Ar/O_2 plasma bombardment approach followed by selective DHF wet etching provides wide process window control to minimize Si substrate damage. Well-behaved CMOS transistors with gate length down to 75 nm indicate that these process modules can be readily utilized to fabricate the dual-metal-gate CMOS for below 65 nm node.

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