A Robust and Fast Digital Background Calibration Technique for Pipelined ADCs

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***Abstract*—This paper presents a background calibration scheme for pipelined analog-to-digital converters (ADCs) that is robust and has short calibration time. For a switched-capacitor (SC) pipeline stage, by splitting its input sampling capacitor, a random sequence can be injected into the ADC's signal path, and then calibration data can be extracted from the ADC's digital output without interrupting its normal conversion operation. Using an input-dependent scheme to generate the calibration random sequence, no additional signal range is required to accommodate the extra calibration signal. Furthermore, using random choppers to scramble signal can ensure that all necessary calibration data can be collected within a given time regardless of input conditions, resulting in a more robust ADC. A split-channel ADC architecture is proposed to reduce the calibration time. The split-channel ADC consists of two A/D channels that receive the same analog input but employ different random sequences for calibration. The calibration time can be greatly reduced by comparing the digital outputs from both channels and then removing the embedded perturbations before extracting the calibration data. The proposed calibration techniques are analyzed by using both theoretical formulation and system-level simulation.**

***Index Terms*—Analog-to-digital (A/D) conversion, calibration, digital background calibration, mixed analog–digital integrated circuits.**

I. Introduction

DIGITAL background calibration techniques have been applied to pipelined analog-to-digital converters (ADCs) to improve resolution and/or reduce power dissipation [1]–[3]. A pipelined ADC comprises several cascaded pipeline stages. Each pipeline stage includes a sub-ADC to quantize the stage's analog input. The digital output of the sub-ADC then drives a sub digital-to-analog converter (DAC) to generate a corresponding analog signal. The analog output of the pipeline stage is generated by subtracting the sub-DAC's output from the stage's analog input and then multiplying the residue by a constant gain factor. Considering only the linear term of the stage's transfer function, to calibrate a pipeline stage is to measure the conversion characteristic of the sub-DAC and the gain factor of the pipeline stage. The calibration data are then used to correct the ADC's digital output, yielding a linear analog-to-digital (A/D) conversion characteristic.

The background calibration schemes mentioned above can conduct the necessary calibration procedures while the ADC is performing its normal A/D conversion operation. In some schemes, extra calibration signal is injected into the signal path and thus additional signal range is required [1], [2]. Although there are schemes that require no extra signal range by changing the circuit configuration of pipeline stages [3], they are not robust. A calibration scheme is called robust if its effectiveness does not rely on the statistics of the input samples, and if all calibration data can be obtained within a given time regardless of input condition. Furthermore, all the schemes mentioned above require long calibration time since they are correlation-based designs, which require a huge amount of samples to extract calibration data while large interferences are present. For a N-bit ADC, the number of required input samples is on the order of 2^{2N} [1], [4].

There are other calibration schemes that require a much smaller number of samples for calibration [4]–[7]. They all need more than one A/D channels. There are schemes that use a reference ADC to calibrate the main ADC [5], [6]. Those schemes are not robust and require an additional accurate albeit slow reference ADC. Other fast calibration schemes use a split-channel ADC architecture, in which two parallel A/D channels quantize the same analog input simultaneously [4], [7]. At the same time, the two A/D channels are subjected to different calibration arrangements by either injecting different calibration signals or arranging different circuit configurations. It is possible to calibrate both A/D channels rapidly by exploring the correlation between their respective digital outputs. The previously published split-channel calibration schemes have only been applied to cyclic ADCs [4], [7]. The scheme described in [4] cannot be applied directly to pipelined ADCs. Although the scheme described in [7] is intended for pipelined ADCs, it is not robust. In addition, it neglects the gain and offset mismatches between the two A/D channels, which lessens the advantages of the split-channel architecture. The mismatch effect becomes more severe when calibrating internal pipeline stages further away from the input.

In [1], the pipelined ADC was assembled with radix-2 1.5-bit switched-capacitor (SC) pipeline stages. For those pipeline stages subjected to calibration, their input sampling capacitors are split into several equal fragments. A random sequence is injected into one of the capacitor fragments. It is then possible to calibrate the pipeline stage without interrupting its normal A/D conversion. Although this calibration scheme is robust,

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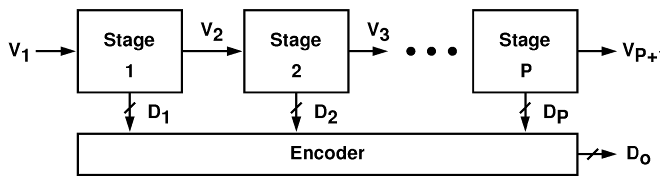

Fig. 1. Pipelined ADC.

it extends the output signal range of pipeline stage under calibration. A compromise has to be made between the number of capacitor fragments and the extra signal range. A larger number of capacitor fragments can release the extra signal range requirement at the expense of longer calibration time. Moreover, this correlation-based scheme inevitably requires long calibration time.

In this paper, we extend the work of [1] and eliminate its deficiencies. An input-dependent generation of the calibration random sequence is proposed to minimize the number of capacitor fragments while eliminating the extra signal range requirement [8]. Random choppers are added to maintain the robustness of the calibration scheme. Finally, a new split-channel ADC calibration technique is proposed to greatly reduce the number of required samples for calibration.

The rest of this paper is organized as follows. Section II gives a brief review of the calibration scheme of [1]. Section III introduces the proposed technique to generate random sequence used in calibration. Also detailed in Section III are corresponding techniques for calibration data extraction, ADC calibration procedures, and ADC output encoding. Section IV describes the reason for adding random choppers. Section V describes the proposed split-channel ADC calibration and its digital signal processing procedures. Section VI presents a 15-bit pipelined split-channel ADC design example. Finally, Section VII draws conclusions.

II. Split-Capacitor Calibration Scheme

The general form of a pipelined ADC is shown in Fig. 1, which consists of P pipeline stages. For the jth stage, its analog input, V_j, is quantized by an internal sub-ADC. Its digital output, D_j, drives an internal sub-DAC to generate a corresponding analog signal, $V_j^{\rm da}(D_j)$. The value of $V_j^{\rm da}(D_j)$ is an rough estimate of V_j. The jth stage's analog output, V_{j+1}, can be expressed as

$$V_{j+1} = G_j \times \left[V_j - V_j^{\rm da}(D_j)\right]. \tag{1}$$

The V_{j+1} output is an estimation residue obtained by subtracting $V_j^{\rm da}(D_j)$ from V_j, and amplified by G_j gain factor. If G_j and $V_j^{\rm da}(D_j)$, for $j = 1, \cdots, P$, are known, the ADC's backend encoder can correctly estimate the ADC's input, V_1, using the digital outputs from all pipeline stages, $D_1, D_2, \cdots, D_P$.

Fig. 2 shows a radix-2 1.5-bit SC pipeline stage and the corresponding conversion characteristic of the pipeline stage is shown in Fig. 3. The sub-ADC comprises two comparators with thresholds at $+0.25V_r$ and $-0.25V_r$, respectively. When $\phi_1 = 1$, the V_j input is sampled on capacitors C_f and C_s, and

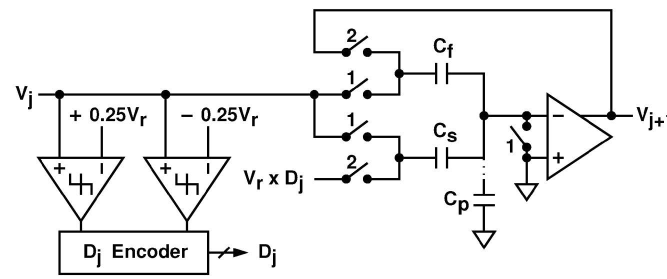

Fig. 2. Radix-2 1.5-bit SC pipeline stage.

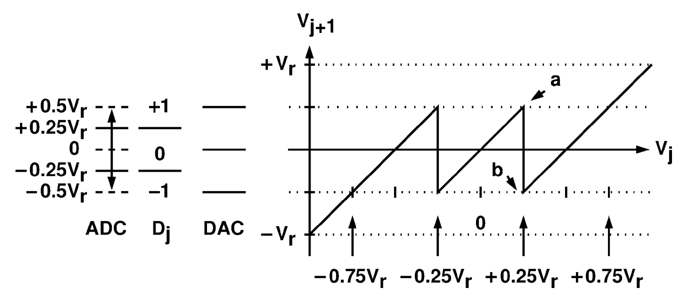

Fig. 3. Conversion characteristic of Fig. 2's pipeline stage.

$D_j \in \{-1, 0, +1\}$ is determined by comparing V_j with the $+0.25V_r$ and $-0.25V_r$ references. When $\phi_2 = 1$, the V_{j+1} output can be written as

$$V_{j+1} = \hat{G}_j \times \left[V_j - \hat{V}_j^{\rm da}(D_j) - V_j^{\rm os}\right] \tag{2}$$

with

$$\hat{G}_j = \frac{C_s + C_f}{C_f} \times \frac{1}{1 + \frac{1}{A_0} \cdot \frac{C_s + C_f + C_p}{C_f}} \tag{3}$$

$$\hat{V}_j^{\rm da}(D_j) = V_r \cdot \frac{C_s}{C_s + C_f} \times D_j. \tag{4}$$

In (3), A_0 is the opamp's dc voltage gain and C_p is the capacitance associated with the opamp's negative input node. The $V_j^{\rm os}$ term represents the offset of the jth stage, which summarizes the offset effect due to the input-referred offset voltage of the opamp, the charge injection from the analog switches, and the offset of the sub-DAC. Due to component mismatches and variations in fabrication process, supply voltage, and temperature, both $\hat{G}_j$ and $\hat{V}_j^{\rm da}(D_j)$ may deviate from the expected values of G_j and $V_j^{\rm da}(D_j)$, respectively.

As detailed in [1], calibration of the jth pipeline stage involves measuring the magnitude of $R_j(D_c)$, which is defined as

$$R_j(D_c) = \hat{G}_j \times \hat{V}_j^{\rm da}(D_c) \tag{5}$$

where D_c is any possible value of D_j. The transition height of the $V_j - V_{j+1}$ transfer function in Fig. 3 is the step size of $R_j(D_c)$ when the D_c digital code is changed by one. During calibration, $R_j(D_c)$ is measured and digitized by a backend pipelined ADC which comprises the $(j+1)$th, $(j+2)$th,$\cdots$, and Pth pipeline stages.

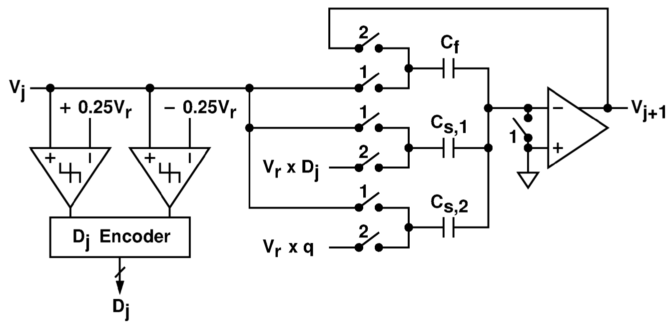

Fig. 4. Split-capacitor SC pipeline stage suitable for background calibration.

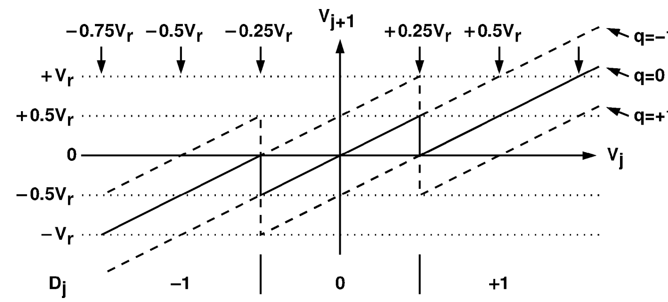

Fig. 5. Transfer characteristic of Fig. 4's pipeline stage.

The split-capacitor SC pipeline stage shown in Fig. 4 can be used to measure and quantize $R_j(D_c)$ of (5) without interrupting its normal A/D operation [1]. The capacitor C_s is split into two fragments of equal value, $C_{s,1}$ and $C_{s,2}$, such that $C_s = C_{s,1} + C_{s2}$. When $\phi_1 = 1$, all capacitors are connected to sample the V_j input. When $\phi_2 = 1$, the $q \cdot V_r$ voltage is connected to one of the C_s fragments, $C_{s,i}$, where $i \in \{1, 2\}$, while the $D_j \cdot V_r$ voltage is connected to the other C_s fragment. The q signal is a digital binary-valued sequence generated from a pseudo random generator. A random sequence with a magnitude of $R_{j,i}(D_c)$ is injected into the signal path of the pipeline stage. The output of the pipeline stage can be expressed as

$$V_{j+1} = \hat{G}_j \times \left[V_j - \hat{V}_j^{\mathrm{da}}(D_j) - V_j^{\mathrm{os}} \right] + R_{j,i}(D_c) \times (D_j - q) \tag{6}$$

where

$$R_{j,i}(D_c) = R_j(D_c) \times \frac{C_{s,i}}{C_s} \tag{7}$$

and D_c is either $+1$ or -1, depending on the polarity of q. To measure $R_{j,i}(+1)$, q alternates between $+1$ and 0. To measure $R_{j,i}(-1)$, q alternates between -1 and 0. Using the techniques described in Section III-B, magnitude information of $R_{j,i}(D_c)$ can be extracted in the digital domain. Then, the magnitude information of $R_j(D_c)$ can be obtained by using $R_j(D_c) = \sum_i R_{j,i}(D_c)$.

Fig. 5 shows the transfer characteristic of the split-capacitor SC pipeline stage of Fig. 4, and the transfer function of the pipeline stage now depends on the state of q. Introducing the q sequence increases the required voltage range of V_{j+1}. If the V_j input is confined between $\pm 0.5V_r$, then the V_{j+1} output expands between $\pm V_r$, comparing with the $\pm 0.5V_r$ span of the Fig. 2 design. The extra output range requirement can be reduced by splitting C_s into more fragments, but at the expense of longer calibration time [1].

III. Calibration With Input-Dependent "q"

In this section, a new scheme for generating the q random sequence is proposed to eliminate the extra output range demand of the split-capacitor pipeline stage of Fig. 4. The q generation scheme is introduced in Section III-A. Its corresponding calibration data extraction is described in Section III-B. General procedures to calibrate the entire ADC are detailed in Section III-C. Encoding and performance evaluation of ADC's digital output are discussed in Section III-D.

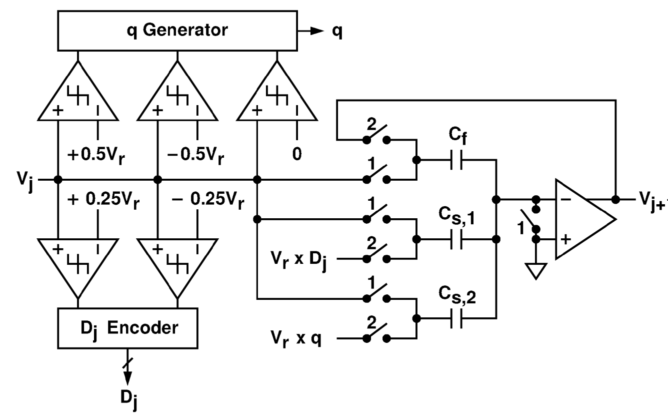

Fig. 6. Split-capacitor SC pipeline stage with redundant comparators.

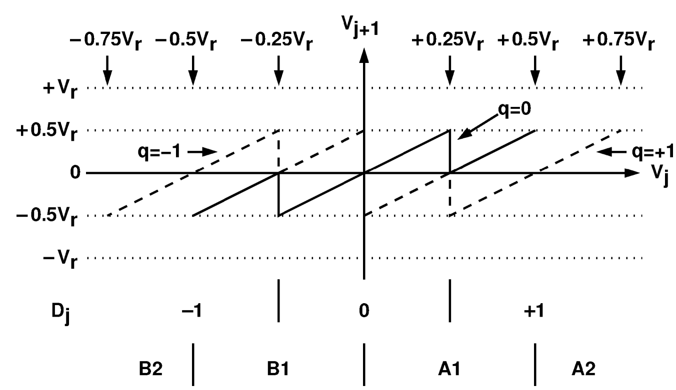

Fig. 7. Transfer characteristic of Fig. 6's pipeline stage.

A. Input-Dependent "q" Generation

The output range of a split-capacitor pipeline stage can be manipulated by input-dependent q generation schemes [8], [9]. The proposed technique is illustrated in Figs. 6 and 7. Comparing with the Fig. 4 pipeline stage, the one shown in Fig. 6 adds three more comparators. They compare the V_j input with three references at 0 and $\pm 0.5V_r$. The comparison results are then used to determine the q sequence. The algorithm to control the q generation is illustrated in Fig. 7 and described as follows. The V_j input range is divided into four different regions, A1, A2, B1, and B2, with boundaries at 0 and $\pm 0.5V_r$. When V_j appears in the A1 region, q can only alternate randomly between $+1$ and 0. When V_j appears in the A2 region, q is always $+1$. When V_j appears in the B1 region, q can only alternate randomly between -1 and 0. When V_j appears in the B2 region, q is always -1.

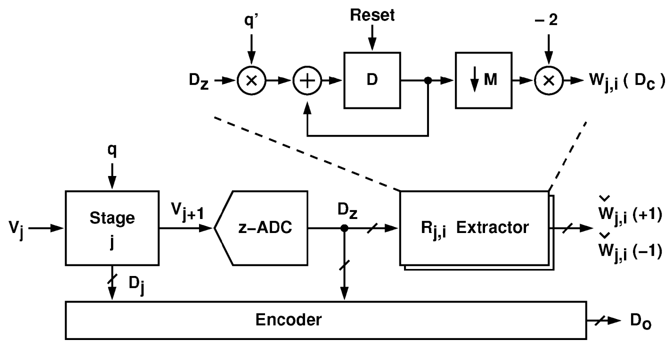

Fig. 8. Background calibration block diagram.

The resulting transfer characteristic for the new pipeline stage is shown in Fig. 7. The voltage range of the V_{j+1} output can now be confined between $\pm 0.5V_r$ as long as the V_j input is confined between $\pm 0.75V_r$.

B. $R_{j,i}$ Extraction

Fig. 8 shows the scheme to extract $R_{j,i}(D_c)$ in the background during normal A/D operation. The z-ADC digitizes V_{j+1} and generates a corresponding D_z digital code. The z-ADC is the backend portion of the pipelined ADC, comprising the $(j+1)$th, $(j+2)$th,$\cdots$, and Pth pipeline stage. The relationship between V_{j+1} and D_z is defined as

$$V_{j+1} = \frac{G_z}{\hat{G}_z} \times D_z + O_z + Q_z. \tag{8}$$

This A/D conversion has a gain error of $G_z/\hat{G}_z$, an offset of O_z and a quantization error of Q_z. Here, G_z represents the specified stage gain factor and $\hat{G}_z$ is the realized stage gain factor [1].

The $R_{j,i}(D_c)$ is then extracted from the $q' \times D_z$ correlation in the digital domain. The q' sequence has the same waveform pattern as q, except its value alternates between $+1$ and -1. The $q' \times D_z$ product is integrated on an accumulator. The resulting $W_{j,i}(D_c)$ digital output is taken out only after M samples of integration, where M is the period of the q random sequence. After averaging the samples over the entire M cycles, it is assumed that $E[q'] = 0$ and $E[q \times q'] = 1/2$.

Note that, for a given pair of j and i, $R_{j,i}(+1)$ and $R_{j,i}(-1)$ are extracted simultaneously. Two separate $R_{j,i}$ extractors are required. Each D_z sample from the z-ADC is either discarded or directed to one of the extractors according to the corresponding V_j value. Two separate pseudorandom number generators, q_{r1} and q_{r2}, are used to generate the q sequence. If V_j appears in the A1 region, q_{r1} advances by one step, q adopts the q_{r1} value, and the corresponding D_z is added to the $R_{j,i}(+1)$ extractor. If V_j appears in the B1 region, q_{r2} advances by one step, q adopts the q_{r2} value, and the corresponding D_z is added to the $R_{j,i}(-1)$ extractor. If V_j appears in either the A2 or the B2 region, both q_{r1} and q_{r2} are frozen, q is set to either $+1$ or -1, and the corresponding D_z is discarded. Assuming that the $R_{j,i}(+1)$ extractor has received M samples for $i = 1$, it can be reconfigured immediately for $i = 2$, without waiting for the $R_{j,i}(-1)$ extractor to collect all its M samples.

The $R_{j,i}$ extractor's output, $W_{j,i}(D_c)$, is an estimation of $R_{j,i}(D_c)$. It can be expressed as

$$\frac{G_z}{\hat{G}_z} \times W_{j,i}(D_c) = \check{R}_{j,i}(D_c) = R_{j,i}(D_c) - \Delta R_{j,i}(D_c). \tag{9}$$

The $\Delta R_{j,i}(D_c)$ variation term is caused by the perturbation of the normal A/D residual signal in V_{j+1}. Assuming that this residual signal is uniformly distributed between 0 and $+0.5V_r$ or between 0 and $-0.5V_r$, its average power can be approximated to $V_r^2/48$. The correlation, integration, and dump function within the extractor can reduce the effect of this perturbation power by a factor of M. Thus, the variance of $\Delta R_{j,i}(D_c)$ can be expressed as

$$\sigma^2(\Delta R_{j,i}) = \frac{1}{M} \times \frac{V_r^2}{48}. \tag{10}$$

Once $W_{j,i}(+1)$ and $W_{j,i}(+1)$ for all $i \in \{1, 2\}$ are extracted, the $W_j(D_c)$ calibration data are calculated by using

$$W_j(D_c) = W_{j,1}(D_c) + W_{j,2}(D_c) \tag{11}$$

where $D_c \in \{-1, +1\}$. In case of $D_c = 0$, one can let $W_j(0) = 0$. The relationship between $W_j(D_c)$ and $R_j(D_c)$ can be expressed as

$$\frac{G_z}{\hat{G}_z} \times W_j(D_c) = \check{R}_j(D_c) = R_j(D_c) - \Delta R_j(D_c). \tag{12}$$

Since $R_j(D_c) = R_{j,1}(D_c) + R_{j,2}(D_c)$, the variance of $\Delta R_j(D_c)$ is $\sigma^2(\Delta R_j) = 2\sigma^2(\Delta R_{j,i})$.

C. ADC Calibration

For a pipelined ADC, there is no need to calibrate all the pipeline stages. In practice, only the first K stages are subjected to calibration. Accuracy of the remaining pipeline stages are ensured by circuit components' inherent characteristics. At the beginning, $W_j(D_c)$ for all $j \in \{1, 2, \cdots, P\}$ and all $D_c \in \{-1, 0, +1\}$ are initialized by setting $W_j(D_c) = G_j \times D_c$. After the initialization, calibration proceeds backward and sequentially from the Kth stage toward the 1st stage in every calibration cycle. Calibration of the Kth stage updates both $W_K(+1)$ and $W_K(-1)$ using the techniques described in Section III-B. The new $W_K(D_c)$ data are then used in calibrating the $(K-1)$th stage. The procedures are repeated until the first stage is carried out. The next calibration cycle begins by calibrating the Kth stage again.

When calibrating the jth stage, the D_z digital output of the corresponding backend z-ADC is obtained by using the following equation:

$$D_z = \sum_{m=j+1}^{P} \frac{W_m(D_m)}{G_{j+1}G_{j+2}\cdots G_m}. \tag{13}$$

The D_z output is encoded with the sub-ADC outputs from the $(j+1)$th, $(j+2)$th,$\cdots$, and Pth pipeline stages.

It is assumed that random q sequence with an identical length of M is employed to calibrate each pipeline stage. A total of $4KM$ samples are required to complete one calibration cycle.

D. ADC Output Encoding

The raw digital output of the overall ADC, D_{o0}, can be encoded by using the following equation:

$$D_{o0} = \sum_{j=1}^{P} \frac{W_j(D_j)}{G_1 G_2 \cdots G_j}. \tag{14}$$

Neglecting quantization error, the relationship between the D_{o0} digital output and the V_1 analog input is

$$D_{o0} = g \cdot V_1 + r_{j,i}(D_c) \cdot (D_j - q) + o \tag{15}$$

where

$$g = \frac{\hat{G}_1 \hat{G}_2 \cdots \hat{G}_P}{G_1 G_2 \cdots G_P} \tag{16}$$

$$r_{j,i}(D_c) = \frac{g}{\hat{G}_1 \hat{G}_2 \cdots \hat{G}_j} \times R_{j,i}(D_c) \tag{17}$$

$$o = -g \times \sum_{j=1}^{P} \frac{V_j^{\mathrm{os}}}{\hat{G}_1 \hat{G}_2 \cdots \hat{G}_{j-1}}. \tag{18}$$

In (15), g is the overall A/D conversion gain, o is the overall offset, and $r_{j,i}(D_c)$ is the magnitude of the pseudorandom noise injected into the pipeline signal path for calibration. The relationship between $W_{j,i}(D_c)$ and $r_{j,i}(D_c)$ is

$$\frac{W_{j,i}(D_c)}{G_1 G_2 \cdots G_j} = \check{r}_{j,i}(D_c) = r_{j,i}(D_c) - \Delta r_{j,i}(D_c) \tag{19}$$

where $\check{r}_{j,i}(D_c)$ is an estimation of $r_{j,i}(D_c)$ calculated from $W_{j,i}(D_c)$. Let $r_j = r_{j,1} + r_{j,2}$, we also have

$$\frac{W_j(D_c)}{G_1 G_2 \cdots G_j} = \check{r}_j(D_c) = r_j(D_c) - \Delta r_j(D_c). \tag{20}$$

The final digital output of the ADC is generated by subtracting $[W_{j,i}(D_c)/(G_1 G_2 \cdots G_j)] \cdot (D_j - q)$ from D_{o0}. From (15) and (19), the D_o final output can be expressed as

$$D_o = g \cdot V_1 + o + \underbrace{\Delta r_{j,i}(D_c) \cdot (D_j - q)}_{n_{\mathrm{cal}}} + n_{\mathrm{enc}} \tag{21}$$

where the calibration noise, n_{cal}, is the residue introduced by the calibration process. From (17), the average power of n_{cal} can be found to be

$$N_{\mathrm{cal}} = \sigma^2(\Delta r_{j,i}) = \sigma^2(\Delta R_{j,i}) \times \frac{g^2}{(\hat{G}_1 \hat{G}_2 \cdots \hat{G}_j)^2}. \tag{22}$$

In (21), the encoding noise, n_{enc}, is added to represent the introduced error when using $W_j(D_c)/(G_1 G_2 \cdots G_j) = \check{r}_j(D_c)$ to encode D_{o0}. Since the $\check{r}_j(D_c)$ data, for all j and D_c, are slow-varying variables compared with a normal V_1 input, the n_{enc} encoding noise in (21) is input-dependent and difficult to be modeled. To simplify the analysis, it is assumed that the $\Delta r_j(D_c)$ variables, for all j and D_c, are random and mutually uncorrelated. Then, the average power of n_{enc} can be approximated to

$$N_{\mathrm{enc}} \approx \sum_{j=1}^{K} \sigma^2(\Delta r_j) \approx 2\sigma^2(\Delta R_{j,i}) \times \sum_{j=1}^{k} \frac{1}{2^{2j}} \approx \frac{2}{3} \cdot \sigma^2(\Delta R_{j,i}). \tag{23}$$

The total noise power due to both calibration and encoding is $N_{\mathrm{cal}} + N_{\mathrm{enc}} = (11/12)\sigma^2(\Delta R_{j,i})$, with $\Delta R_{j,i}$ expressed in (10). It is assumed that the first pipeline stage is calibrated for worst case condition, in which $N_{\mathrm{cal}} = \sigma^2(\Delta r_{j,i}) = 0.25\sigma^2(\Delta R_{j,i})$ with $j = 1$. To estimate the required value of M, let $N_{\mathrm{cal}} + N_{\mathrm{enc}}$ be less than the average power of the ADC's quantization noise, N_{qn}. For an ideal N-bit ADC with an input range of $\pm 0.5V_r$, its N_{qn} is $(1/12)(V_r/2^N)^2$. Thus, the required value for M is

$$M \geq \frac{11}{12} \times 2^{2N-2} \approx 2^{2N-2}. \tag{24}$$

Large M is necessary to achieve high A/D resolution, but also results in long calibration time. If the input is a full-range sine wave, i.e., $V_1(t) = 0.5V_r \sin(\omega_i t)$, the signal-to-distortion-plus-noise ratio (SNDR) of the D_o of (21) is

$$\mathrm{SNDR}_o \approx \frac{g^2 \cdot E\left[V_1^2\right]}{N_{\mathrm{cal}} + N_{\mathrm{enc}}} \approx \frac{72}{11} \times M. \tag{25}$$

The equation assumes $g = 1$ and neglects the quantization noise.

IV. Input Scrambling Using Random Choppers

In the calibration scheme described Section III, each $R_{j,i}(D_c)$ extractor must accumulate M samples to complete one extraction. However, the valid samples depend on the value of V_j. If V_j seldom appears in the A1 region, then it takes a long time for the $R_{j,i}(+1)$ extractor to collect enough samples to estimate $R_{j,1}(+1)$ and $R_{j,2}(+1)$.

Random choppers are used to ensure that all calibration data can be collected within a given time regardless of input condition. As shown in Fig. 9, a chopper, CHP1, is placed at the j-stage's input. The V_j input is scrambled so that it can appear in either the A1 or B1 region of Fig. 7 with equal probability. The CHP1 chopper is controlled by a binary-valued random sequence, $q_c \in \{+1, -1\}$. In CMOS fully-differential circuit configurations, the CHP1 can be realized by using 4 analog switches, so it passes the inputs directly when $q_c = +1$ and interchanges the inputs when $q_c = -1$.

If the comparator associated with the 0 reference has an input offset, then its output is a constant when $V_j = 0$, regardless of the CHP1 chopper's current state. Thus, as shown in Fig. 9, an additional chopper is placed at the inputs of the 0-reference comparator. This chopper is controlled by a binary-valued sequence, $q_{cz} \in \{+1, -1\}$. Each 0-reference comparator in the pipeline stages subjected to calibration is required to be equipped with an input chopper. The q_{cz} sequence can be a simple square wave alternating its value every clock cycle.

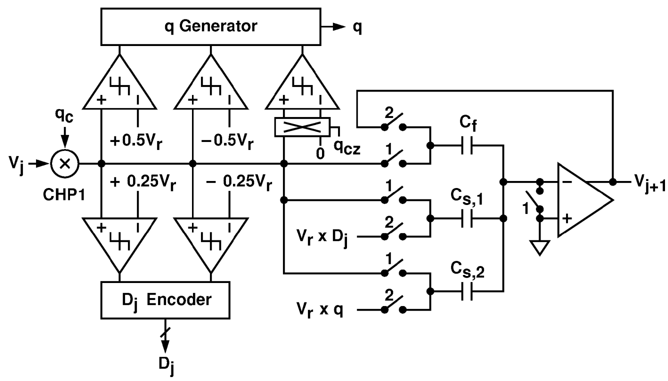

Fig. 9. Split-capacitor SC pipeline stage with random choppers.

For an entire pipelined ADC, only the first pipeline stage requires a CHP1 chopper. If the CHP1 chopper is embedded in the ADC's input sampling network, its design is not trivial. For most ADCs, the CHP1 chopper can be placed behind ADC's sample-and-hold amplifier to lessen the matching requirement of its analog switches.

Even with a CHP1 chopper, the calibration process will slow down if the V_j input is so large that it appears in the A2 or B2 region of Fig. 7 for most of time. But these are rare cases. A practical application usually includes an automatic gain-control mechanism that can prevent the ADC from being overloaded.

The use of CHP1 chopper modulates the ADC's input with a q_c random sequence. Demodulation of the ADC's digital output can be expressed as $q_c \times D_o$. As a result, the ADC's offset, i.e., the o term in (21), becomes a $q_c \times o$ random noise in the ADC's final digital output, which degrades the ADC's signal-to-noise ratio (SNR) performance. Offset cancellation is covered in Section V-B.

V. Split-Channel ADC Architecture

The correlation-based calibration schemes usually suffer from long calibration time when applied to high-resolution ADCs. Referring to Fig. 8 and (6), the V_{j+1} stage output contains both the $R_{j,i}(D_c)$ calibration term and the nominal A/D residue term. To extract $R_{j,i}(D_c)$ from the D_z digital codes, a large number of samples are required for the correlator to attenuate the perturbation caused by the V_j stage input, as expressed by (10). To decrease calibration time, i.e., decrease the M in (10), all signals other than the $q \times R_{j,i}(D_c)$ term must be reduced at the inputs of the $R_{j,i}$ extractors.

Fig. 10 shows the proposed split-channel ADC architecture that can be used to reduce the calibration time. The ADC is formed by splitting the original single-channel ADC into two identical parallel A/D channels. Both the A channel and the B channel quantize the same analog input, V_i. Their separate outputs are then combined to produce the final D_o digital output. Each split channel has the same circuit topology as the single-channel ADC but with devices half of the original size. Comparing with the original single-channel ADC, the operating speed and total power dissipation are preserved in the split-channel ADC. Considering only the effect of kT/C thermal noises, each split path contains thermal noises with

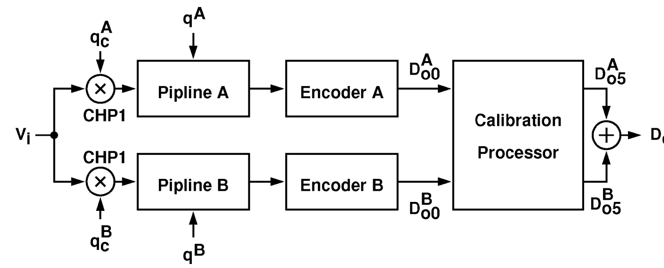

Fig. 10. Split-channel ADC architecture for background calibration.

average powers twice as large as those in the original design. But since both split paths convert the same analog input, the combined digital output has the same SNR as the output of a single-channel ADC [4], [7].

The two CHP1 random choppers in Fig. 10 are controlled by two mutually-uncorrelated binary random sequences, q_c^A and q_c^B, which alternate between $+1$ and -1. The choppers are added to scramble the V_i input for the reason described in Section IV. The input scrambling is also useful in extracting the input offsets of the two A/D channels, which is described in Section V-B. The other two random sequences, q^A and q^B, are injected into the respective pipeline stages for $R_{j,i}$ calibration. The q^A and q^B sequences are designed to be statistically uncorrelated, and their generation is described in Section III-A. The two A/D channels are calibrated concurrently.

Unlike the calibration procedures described in Section III in which the $R_{j,i}(D_c)$ is extracted from the output of the backend z-ADC, the calibration scheme described in this section extracts $R_{j,i}(D_c)$ from the overall ADC digital output. From (14), (15) and (21), the raw digital outputs of the two A/D channels can be expressed as

$$\begin{aligned} D_{o0}^A &= q_c^A \cdot g^A \cdot V_i + r_{j,i}^A \cdot \left(D_j^A - q^A\right) + o^A + n_{\text{enc}}^A \\ D_{o0}^B &= q_c^B \cdot g^B \cdot V_i + r_{j,i}^B \cdot \left(D_j^B - q^B\right) + o^B + n_{\text{enc}}^B. \end{aligned} \quad (26)$$

The definitions of g^A, g^B, o^A, and o^B are the same as those of (15). The $r_{j,i}^A$ and $r_{j,i}^B$ symbols are simplified notations for $r_{j,i}^A(D_c)$ and $r_{j,i}^B(D_c)$, respectively. Both n_{enc}^A and n_{enc}^B are encoding noises due to the errors in $r_{j,i}^A(D_c)$ and $r_{j,i}^B(D_c)$ estimations, as defined in (21). In the equations mentioned above and for the following analysis, a variable with a superscript of A or B is denoted as a variable in one of the A/D channel. A variable without the A or B superscript implies it can be applied to both channels.

Fig. 11 shows the block diagram of the calibration processor in Fig. 10. The D_{o0}^A and D_{o0}^B raw digital outputs from the encoders are subjected to identical signal processing procedures in the calibration processor. Instead of sending D_{o0} to the $r_{j,i}$ extractors directly, the offset in D_{o0}, i.e., the o term in (26), is eliminated by using the offset correction (OC) functional block. The resulting D_{o3} is subtracted by D_{o7} generated from the other channel to eliminate the $q_c g V_i$ term in (26). If both o and $q_c g V_i$ can be removed effectively in the resulting D_{o8} signal, the required number of samples for $r_{j,i}$ extraction can then be decreased to reduce calibration time. The output of the $r_{j,i}$ extractor is an estimation of $r_{j,i}$, i.e., the $\check{r}_{j,i}$ defined in (19).

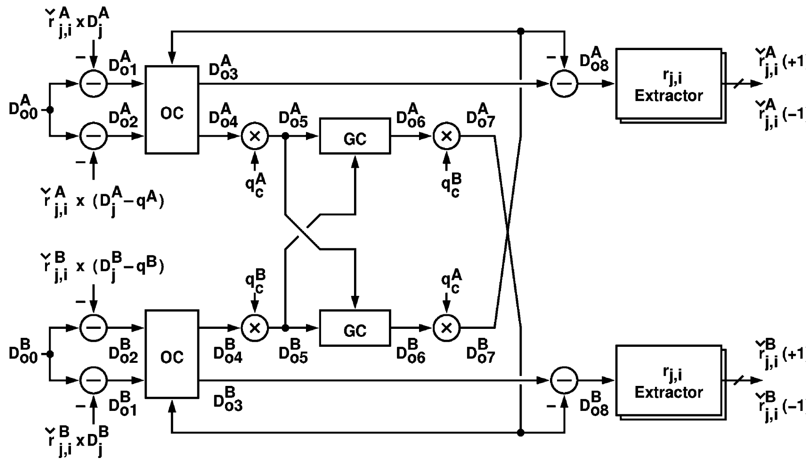

Fig. 11. Calibration processor for the split-channel ADC.

It will become clear later that the D_{o6} signal in either channel is a V_i duplicate of the other channel. They can be expressed as

$$\begin{aligned} D_{o6}^A &= g_c^A g^A \cdot V_i + g_c^A q_c^A \\ &\quad \cdot \left[\Delta r_{j,i}^A \left(D_j^A - q^A\right) - \Delta o^A + n_{\text{enc}}^A\right] \\ D_{o6}^B &= g_c^B g^B \cdot V_i + g_c^B q_c^B \\ &\quad \cdot \left[\Delta r_{j,i}^B \left(D_j^B - q^B\right) - \Delta o^B + n_{\text{enc}}^B\right]. \end{aligned} \tag{27}$$

The g_c is a gain correction factor generated from the gain correction (GC) functional block. Both $\Delta r_{j,i}$ and Δo are residues due to non-ideal $r_{j,i}$ extraction and offset cancellation. Their values will be reduced to a level as low as the ADC's LSB. Neglecting $\Delta r_{j,i}$, Δo, and n_{enc}, if $g_c^A g^A = g^B$, the $q_c^B g^B V_i$ term in D_{o0}^B of (26) can be eliminated by subtracting $D_{o7}^A = q_c^B D_{o6}^A$ from D_{o0}^B. The GC block adaptively adjusts the g_c^A GC factor so that $g_c^A \times g^A \approx g^B$. The gain mismatches are defined as

$$\begin{aligned} \Delta g^A &= g^A - g_c^B \times g^B \\ \Delta g^B &= g^B - g_c^A \times g^A. \end{aligned} \tag{28}$$

The detailed signal processing procedures of the calibration processor are described in the following subsections.

A. Calibration Noise Reduction

As shown in Fig. 11, the $r_{j,i}$ random term in (26) is first subtracted from D_{o0} to yield D_{o1} and D_{o2}, respectively. The $\check{r}_{j,i}$ value used in the subtraction is an estimation of $r_{j,i}$ obtained in the previous calibration cycle using the $r_{j,i}$ extractor. The difference between $r_{j,i}$ and $\check{r}_{j,i}$ is $\Delta r_{j,i}$, as defined in (19).

The $r_{j,i}q$ term is kept in D_{o1}. The calibration processor extracts $r_{j,i}q$ from D_{o1} to obtain a new $\check{r}_{j,i}$.

B. Offset Correction

Due to the use of the CHP1 random chopper shown in Fig. 10, the only dc components in the D_{o1} and D_{o2} signals are the input-referred offsets of the A/D channels [10], i.e., the o terms in (26). Fig. 12 shows the block diagram of the OC block for the A channel. The OC block uses the integration and dump technique to estimate the channel offset from D_{o2}^A. The D_{o2}^A signal is first subtracted by D_{o7}^B, and the result, D_{os}^A, is then integrated on an accumulator (ACC). The o_c offset estimation is taken out only after M_c cycles of integration, where M_c is the period of the q_c^A random sequence shown in Fig. 10. The difference between o and o_c is defined as

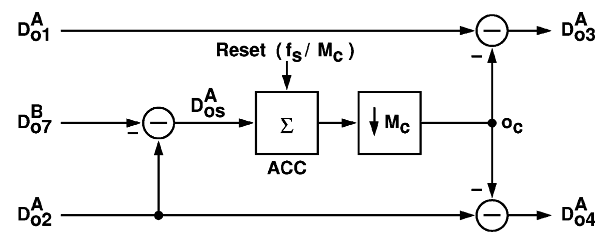

Fig. 12. OC block diagram.

$$\Delta o = o - o_c. \tag{29}$$

The OC block's outputs D_{o3}^A and D_{o4}^A are generated by subtracting o_c from D_{o1}^A and D_{o2}^A, respectively.

In Fig. 12, the reason to undertake $D_{os}^A = D_{o2}^A - D_{0o7}^B$ before the integration is to reduce the perturbation of the $q_c^A g^A V_i$ term in (26) and decrease the required integration time for offset estimation. When the calibration process converges, Δo, $\Delta r_{j,i}$, and n_{enc} are reduced to a level close to the ADC's LSB, the only significant perturbation remaining in D_{os}^A is the $\Delta g^A V_i$ term. Thus, the variance of Δo can be approximated to

$$\sigma^2(\Delta o) \approx \frac{1}{M_c} \times \left\{\sigma^2(\Delta g) \cdot E\left[V_i^2\right]\right\}. \tag{30}$$

C. Gain Correction

As shown in Fig. 11, $D_{o5} = q_c \cdot D_{o4}$, thus D_{o5} contains the unscrambled $g \cdot V_i$ term. In the GC blocks, D_{o5} is multiplied by a GC factor, g_c, to generate D_{o6}. The D_{o7} is generated by scrambling the D_{o6} of (27) with the q_c random sequence of the other channel. The GC blocks are used to generate the g_c gain factors so that the Δg^A and Δg^B of (28) can be minimized.

Fig. 13 is the GC's block diagram in the A-channel signal path, which is similar to the adaptation scheme of [11], and is a variation of least-mean-square (LMS) algorithm [12]. The GC

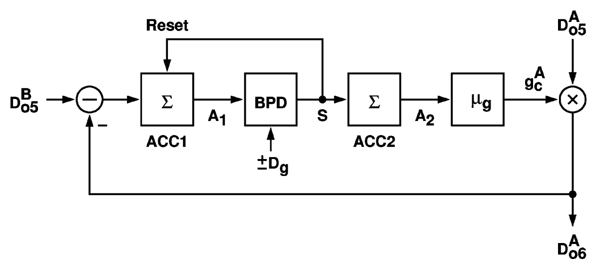

Fig. 13. GC block diagram.

block adaptively adjusts the g_c^A GC factor to minimize the difference between D_{o6}^A and D_{o5}^B. The converged g_c^A yields $g_c^A \times g^A \approx g^B$. In Fig. 13, the difference between D_{o6}^A and D_{o5}^B is integrated on the ACC1 accumulator. The bilateral peak detector (BPD) monitors the ACC1's output, A_1, and generates a corresponding triple-valued output, $S \in \{+1, 0, -1\}$. The BPD has two thresholds, $+D_g$ and $-D_g$. When $A_1 > +D_g$, $S = +1$. When $A_1 < -D_g$, $S = -1$. Otherwise, $S = 0$. In addition, if $S = +1$ or $S = -1$, the ACC1 accumulator will be reset in the following clock cycle. Thus, $-(D_g + 1) \leq A_1 \leq +(D_g + 1)$, and S can only remain $+1$ or -1 for one clock cycle. The S sequence is integrated on the ACC2 accumulator, yielding A_2. The g_c^A GC factor is $\mu_g \times A_2$.

This automatic gain-control loop has two design parameters, i.e., D_g and μ_g. Small D_g and large μ_g result in fast converging speed but larger fluctuation in g^A. On the other hand, large D_g and small μ_g result in slow converging speed but smaller fluctuation in g^A.

If the V_i input is stable such that $E[|V_i|]$ is a constant, then the gain-control feedback loop can be modeled as a single-pole system with a τ_g time constant expressed as

$$\tau_g \approx \frac{1}{\mu_g} \times \frac{D_g}{E[|V_i|]}. \quad (31)$$

The τ_g must be much shorter than M, the period of the q^A and q^B random sequences. This ensures that the GC adaptation process has little effect on the overall calibration result.

This GC adaptation loop adjusts the g_C^A gain factor according to the difference between D_{o5}^B and $g_c^A D_{o5}^A$. As will be explained later, both D_{o5}^A and D_{o5}^B contain encoding noise, n_{enc}, and calibration noise, n_{cal}. Those noises cause g_c to fluctuate. The behavior of the loop can be analyzed by using stochastic signal processing technique [11]. It is desirable to make D_g larger than $\sqrt{N_{\text{enc}} + N_{\text{cal}}}$ so that both the n_{enc} and n_{cal} noises have little effect on the BPD's output, where N_{enc} and N_{cal} are the average powers of n_{enc} and n_{cal}, respectively. A semi-empirical expression for the variance of Δg is

$$\sigma^2(\Delta g) = \frac{\mu_g^2}{6} + \frac{\mu_g^2}{3} \times \frac{E[|V_i|]}{D_g} \times \frac{\sqrt{N_{\text{enc}} + N_{\text{cal}}}}{V_{\text{LSB}}} \quad (32)$$

where V_{LSB} is the ADC's LSB voltage. If D_g is large enough, the Δg of (28) has a mean of zero and fluctuates between $[P, P-\mu_g]$, where $P \in [0, \mu_g]$. The probability density function of Δg is $1 - |\Delta g|/\mu_g$. In such a case, the variance of Δg approximates to $\mu_g^2/6$, which is the first term on the right-hand side of (32). The second term on the right-hand side of (32) arises from the perturbation of n_{enc} and n_{cal}. Both noises are increased if smaller M is used, then large D_g is required. A compromise should be made between the $\sigma^2(\Delta g)$ and the convergent speed of the GC loop.

D. $r_{j,i}$ Extraction

As shown in Fig. 11, the input of the $r_{j,i}$ extractor, D_{o8}, is generated by subtracting D_{o7} coming from the other channel from D_{o3}. The $r_{j,i}$ extractors in Fig. 11 are identical to the $R_{j,i}$ extractor shown in Fig. 8. The D_{o8} signal contains the $r_{j,i}q$ term which the $r_{j,i}$ extractors is in need of, and other terms which can be regarded as perturbations and cause variation in the $r_{j,i}$ extraction. Among the perturbations, the $\Delta g V_i$ term is much larger than other ones that contain the residual $\Delta r_{j,i}$ or Δo terms. As the calibration process converges, both $\Delta r_{j,i}$ and Δo are reduced to a level close to the ADC's LSB. The variance of the $r_{j,i}$ estimation can be approximated to

$$\sigma^2(\Delta r_{j,i}) \approx \frac{1}{M} \times \left\{\sigma^2(\Delta g) \cdot E\left[V_i^2\right]\right\}. \quad (33)$$

Comparing (33) with (10), the required M for the split-channel architecture can be decreased by a factor comparable to $\sigma^2(\Delta g)$. Since much smaller M can be used, it is critical to ensure that the q random sequence has equal number of zeros and ones for consecutive M samples in each $r_{j,i}$ extraction cycle.

E. ADC Outputs

In Fig. 11, D_{o5}^A and D_{o5}^B are the final digital outputs for the two A/D channels. Both can be expressed as

$$D_{o5} = g \cdot V_i + q_c \cdot \left[\underbrace{\Delta r_{j,i} \cdot (D_j - q) - \Delta o}_{n_{\text{cal}}} + n_{\text{enc}}\right]. \quad (34)$$

The n_{cal} calibration noise is introduced by the calibration process. The n_{enc} encoding noise occurs when using the $\check{r}_{j,i}$ estimation to encode D_{o0}. The average power of n_{cal} can be expressed as

$$N_{\text{cal}} = 2\sigma^2(\Delta r_{j,i}) + \sigma^2(\Delta o) \approx \left(\frac{1}{M} + \frac{1}{M_c}\right) \times \sigma^2(\Delta g) \cdot E\left[V_i^2\right]. \quad (35)$$

The average power of n_{enc} can be approximated to

$$N_{\text{enc}} \approx 2K \times \sigma^2(\Delta r_{j,i}) \approx \frac{2K}{M} \times \sigma^2(\Delta g) \cdot E\left[V_i^2\right]. \quad (36)$$

Neglecting quantization noise, the SNDR of the D_{o5} digital output can be expressed as

$$\text{SNDR}_{o5} = \frac{g^2 \cdot E\left[V_i^2\right]}{N_{\text{cal}} + N_{\text{enc}}} \approx \frac{g^2}{\sigma^2(\Delta g)} \times \frac{1}{\frac{2K+1}{M} + \frac{1}{M_c}}. \quad (37)$$

The required M and M_c can be estimated by letting $N_{\text{cal}} + N_{\text{enc}}$ approximate the average power of ADC's quantization noise.

TABLE I
GAINS AND OFFSETS OF THE PIPELINE STAGES IN SIMULATIONS

Gain						
Channel	$\hat{G}_1$	$\hat{G}_2$	$\hat{G}_3$	$\hat{G}_4$	$\hat{G}_5$	$G_{z6}/\hat{G}_{z6}$
A	1.90	1.90	1.90	1.90	1.90	0.95
B	2.10	2.10	2.10	2.10	2.10	1.05

Offset						
Channel	V_1^{os}	V_2^{os}	V_3^{os}	V_4^{os}	V_5^{os}	O_{z6}
A	+0.05	+0.05	+0.05	+0.05	+0.05	+0.05
B	−0.005	−0.05	−0.05	−0.05	−0.05	−0.05

In Fig. 10, the final ADC output D_o is $D_{o5}^A + D_{o5}^B$. Assuming that the calibration noises and the encoding noises are uncorrelated, the SNDR of the D_o digital output is 3 dB better than the one predicted by (37).

Referring to Fig. 10, a CHP1 random chopper is placed in front of each A/D channel. It should be pointed out that mismatches among analog switches within the CHP1 chopper can superimpose a q_c-like noise at A/D channel's input. If this q_c-like noise has a non-zero mean value, it can cause offset estimation error in the OC block, and its mean value is added to the Δo. In practical cases, a minuscule increase in $|\Delta o|$ has little effect on the succeeding GC and $r_{j,i}$ extraction operations. However, it can degrades the SNDR of the ADC's final digital output, as manifested by (34).

VI. A 15-BIT ADC DESIGN EXAMPLE

A 15-bit pipelined split-channel ADC was simulated by using a C program to verify the proposed calibration techniques. The ADC employs the architecture of Fig. 10, which consists of two separate A/D channels. Each channel comprises 15 radix-2 1.5-bit pipeline stages. Each pipeline stage has a transfer characteristic of (2), and its nominal stage gain is $G_j = 2$. Referring to Fig. 3, and let $V_r = 1$, then the ADC's input range is ± 0.5. For 15-bit resolution, the ADC's LSB step size is $V_{\text{LSB}} = 2^{-15}$. Assuming the ADC's input is a full-range sine wave, i.e., $V_i(t) = 0.5\sin(\omega_i t)$, we have $E[|V_i|] = 1/\pi$ and $E[V_i^2] = 1/8$. The quantization noise power is $N_{qn} = (1/12) \times 2^{-30}$.

For each A/D channel, only the first five pipeline stages, i.e., from the 1st to the 5th stage ($K = 5$), are subjected to calibration and employ the schematic of Fig. 9. The CHP1 random choppers in Fig. 9 is removed and replaced with a single chopper at the ADC's input as shown in Fig. 10. The gains and offsets of the pipeline stages in each channel are assigned the values in Table I. The last ten stages in each A/D channel, i.e., from the 6th to the 15th stage, are summarized as a single 11-bit ADC with its own conversion gain and offset and an input range of ±1. Similar to (8), their functions are expressed as

$$V_6^A = \frac{G_{z6}^A}{\hat{G}_{z6}^A} \cdot D_{z6}^A + O_{z6}^A + Q_{z6}^A$$
$$V_6^B = \frac{G_{z6}^B}{\hat{G}_{z6}^B} \cdot D_{z6}^B + O_{z6}^B + Q_{z6}^B. \quad (38)$$

Both Q_{z6}^A and Q_{z6}^B are quantization errors. For 10-bit resolution over ± 0.5 input range, we have $|Q_{z6}^A| < 2^{-11}$ and $|Q_{z6}^B| < 2^{-11}$.

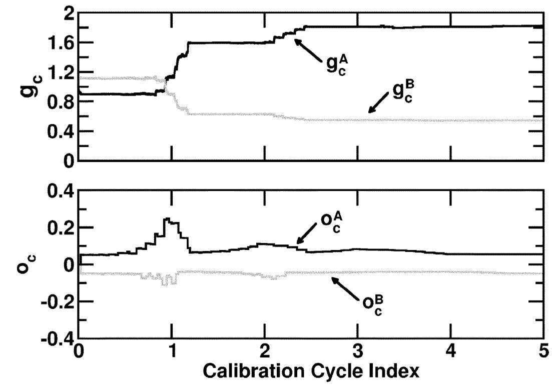

Fig. 14. Simulated g_c and o_c versus calibration cycle.

The ADC follows the calibration procedures described in Section III-C. For a split-channel ADC, its $r_j(D_c)$ is getting updated by calibration. A total of $5 \times 4M$ samples are required to calibrate 5 pipeline stages in one r_j calibration cycle.

In addition to the r_j calibration, the OC block and GC block shown in Fig. 11 operate concurrently. For both GC blocks, we choose $D_g = 2^{-6}$ and $\mu_g = 2^{-11}$. From (31), the time constant of the GC system is $\tau_g = 2^6$. From (32), (35), and (36), by letting $N_{\text{cal}} + N_{\text{enc}}$ equals the N_{qn} quantization noise power for 15-bit resolution, one can choose $M_c = 2^{11}$ and $M = 2^{14}$, resulting in $\sigma^2(\Delta g) = 8.5 \times 10^{-7}$, $N_{\text{cal}} \approx N_{\text{enc}} \approx 5.8 \times 10^{-11}$. However, simulations show that a system with $M_c = 2^{12}$ and $M = 2^{13}$ can also achieve 15-bit resolution and has a shorter calibration time.

Unless otherwise specified, the following simulations and discussions assume that $M_c = 2^{12}$, $D_g = 2^{-6}$, $\mu_g = 2^{-11}$, and $M = 2^{13}$. The V_i input is a sine wave with an amplitude of 0.5 and a frequency close to 1/10 of the ADC's sample rate.

Fig. 14 shows the transient behaviors of the g_c and o_c variables. The variables are shown against the progress of calibration cycle. Each calibration cycle spans $20M$ clock cycles. Both o_c^A and o_c^A are updated once every M_c clock cycles. Although both g_c^A and g_c^B are continuously adjusted, there are visible abrupt changes during initial calibration cycles. The abrupt changes occur whenever ADC's W_j variables are updated.

Fig. 15 shows the initial converging behavior of the calibration process in the split-channel ADC as well as the behavior in the single-channel ADC. Each calibration cycle spans $20M$ clock cycles, where $M = 2^{13}$ for the split-channel ADC and $M = 2^{25}$ for the single-channel ADC. The SNDR of the split-channel ADC is stabilized after five calibration cycles, while the SNDR of the single-channel ADC approximates its final value after only one calibration cycle. In a split-channel ADC, the effectiveness of $r_{j,i}$ extraction, OC, and GC, depends on each other. The coupling effect slows down the calibration progress. For this split-channel ADC with other design parameters unchanged, the calibration cannot converge if M is smaller than 2^9.

Fig. 16 shows the SNDR performance of the split-channel ADC with different M. It also compares the split-channel ADC with a single-channel ADC that consists of pipeline stages

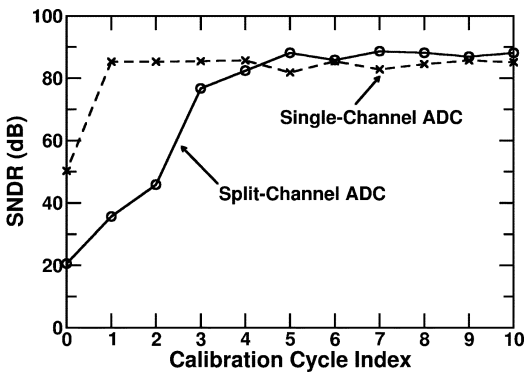

Fig. 15. Simulated ADC's SNDR versus calibration cycle.

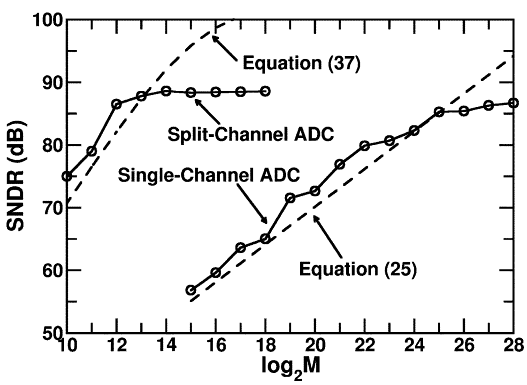

Fig. 16. Simulated SNDR performance with different values of M.

identical to those in the split-channel ADC. The SNDR of the split-channel ADC is calculated from the digital output of the A channel only. For the combined output of the split-channel ADC, its SNDR is 3 dB better than those shown in Fig. 16. The SNDR values predicted by (25) and (37) are more pessimistic than those obtained from simulations. Nevertheless, the equations are useful in the initial performance estimations. From both theoretical calculations and simulations, the required M for a split-channel ADC is significantly smaller than that for a single-channel ADC of similar design.

VII. Conclusion

This paper describes a robust and fast background calibration scheme for SC pipelined ADCs. By splitting the C_s capacitor of a SC pipeline stage, a "q" random sequence with information regarding both the stage's conversion gain and the sub-DAC's characteristic can be injected into the ADC's signal path. The information is then extracted from the ADC's digital output without interrupting the ADC's normal conversion operation. By applying input-dependent generation of the "q" random sequence, the C_s capacitor needs only to be split into two equal fragments to save calibration time, while requiring no extra signal range to accommodating this random sequence. Using random choppers to scramble signal ensures that all necessary calibration data can be collected within a given time regardless of the input condition, resulting in a more robust ADC. The split-channel ADC architecture consists of two identical A/D channels that receive the same V_i input but employ different random sequences for calibration. The calibration time can be greatly reduced by comparing the digital output streams from both channels and then removing the V_i-related term at the inputs of $r_{j,i}$ extractors and offset estimators. OC block and GC block are employed to equalize the transfer characteristics of the two A/D channels.

The proposed calibration scheme is most suitable for high-resolution ADCs realized in nano-scaled CMOS technologies. Most of the calibration overhead is digital circuitry, whose power consumption and area are scaled down with technology scaling. The calibration mitigates the device matching and opamp's dc gain requirements, yielding analog circuits with less power consumption. This calibration scheme requires no extra output voltage range for the opamps, which is crucial for circuits operating under low-voltage supplies. The proposed scheme eliminates the concern for long calibration time, which may become unacceptable in high-resolution ADC designs. The scheme is robust since it can function under any input condition as long as it does not exceed the specified ADC's input range.

Although only radix-2 1.5-bit SC pipeline stages are included in the discussions, the techniques described in this paper can be extended and applied to multi-bit pipeline stages as well as pipeline stages with circuit configuration not in the SC form.

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