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Field enhancement of omega-shaped-gated poly-Si TFT SONOS memory fabricated by a simple sidewall spacer formation

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ABSTRACT

A novel omega-shaped-gated (Ω-Gate) poly-Si thin-film-transistor (TFT) silicon–oxide–nitride–oxide–silicon (SONOS) nonvolatile memory devices fabricated with a simple process have been proposed for the first time. The Ω-Gate structure inherently covered two sharp corners manufactured simply via a sidewall spacer formation. Due to the sharp corner geometry, the local electric fields across the tunneling oxide could be enhanced effectively, thus improving the memory performance. Based on this field enhanced scheme, the Ω-Gate TFT SONOS revealed excellent program/erase (*P*/*E*) efficiency and larger memory window as compared to the conventional planar (CP) counterparts. In addition, owing to the better gate controllability, the Ω-Gate TFT SONOS also exhibited superior transistor performance with a much higher on-current, smaller threshold voltage, and steeper subthreshold swing. Therefore, such an Ω-Gate TFT SONOS memory is very promising for the embedded flash on the system-on-panel applications.

1. Introduction

Low-temperature poly-Si thin-film-transistors (LTPS–TFTs) have been put emphasis not only on the switching pixel elements but also the integrated peripheral driving circuit in the same glass substrate to meet the system-on-panel (SOP) applications [1,2]. In order to realize the low-cost, thinner and lower-power portable electronic products, integration of various functional memories and controllers in a chip is necessary for value-added SOP applications [3]. It is well known that the nonvolatile memory (NVM) is popularly used for portable memory because of the superior device durability and power saving. In addition, due to the potential device scalability, silicon–oxide–nitride–oxide–silicon (SONOS)-type devices, instead of traditional floating-gate ones, have been considered as a promising NVM candidate for SOP applications [4].

However, unlike floating gate NVM, the conventional planar (CP) TFT SONOS memories lack the gate-coupling design, thus suffering form the insufficient programming/erasing (*P*/*E*) efficiency [5]. To overcome these problems, various field-enhancement memory structures with edge corner, such as tri-gate [6] or pi-gate [7] nanowire TFT memories fabricated by e-beam lithography methods have been demonstrated to enhance *P*/*E* efficiency. Although the memory characteristics could be improved by device structure schemes, e-beam lithography was an expansive and low-throughput process, resulting in the cost concern. Likewise, another field-enhancement metal–oxide–nitride–oxide–polysilicon (MONOS) memory using sequential lateral solidified (SLS) crystallization method has been reported for the enlargement of the memory window [8]. Yet, the locations and heights of SLS tips were difficult to control which might arise the process complexity and device variation issues [9].

In this work, a simple and low-cost process was proposed to construct a novel field-enhanced structure on poly-Si TFT SONOS with Ω-Gate structure. Especially, the Ω-Gate TFT SONOS possessed excellent transistor performance and memory characteristics, thanks to the improved Ω-Gate controllability and the sharpened corner geometry.

2. Device fabrication

The process sequence of Ω-Gate poly-Si TFT SONOS device is schematically shown in Fig. 1 [10]. A 1.0-μm-thick thermal SiO_2 was first grown on single crystal silicon wafers for substituting glass substrate. Then, an etch-stop layer of Si_3N_4 (50-nm-thick) and a sacrificial layer of TEOS SiO_2 (300-nm-thick) were sequentially deposited through the low pressure chemical vapor deposition (LPCVD) system. After the sacrificial SiO_2 layer was anisotropic etched with several dummy strips (100-nm depth) by reactive ion etch (RIE) process (Fig. 1a), a 100-nm-thick a-Si film was conformally deposited by LPCVD at 550 °C. The source/drain pad photoresist (PR) was then patterned to overlap on the two

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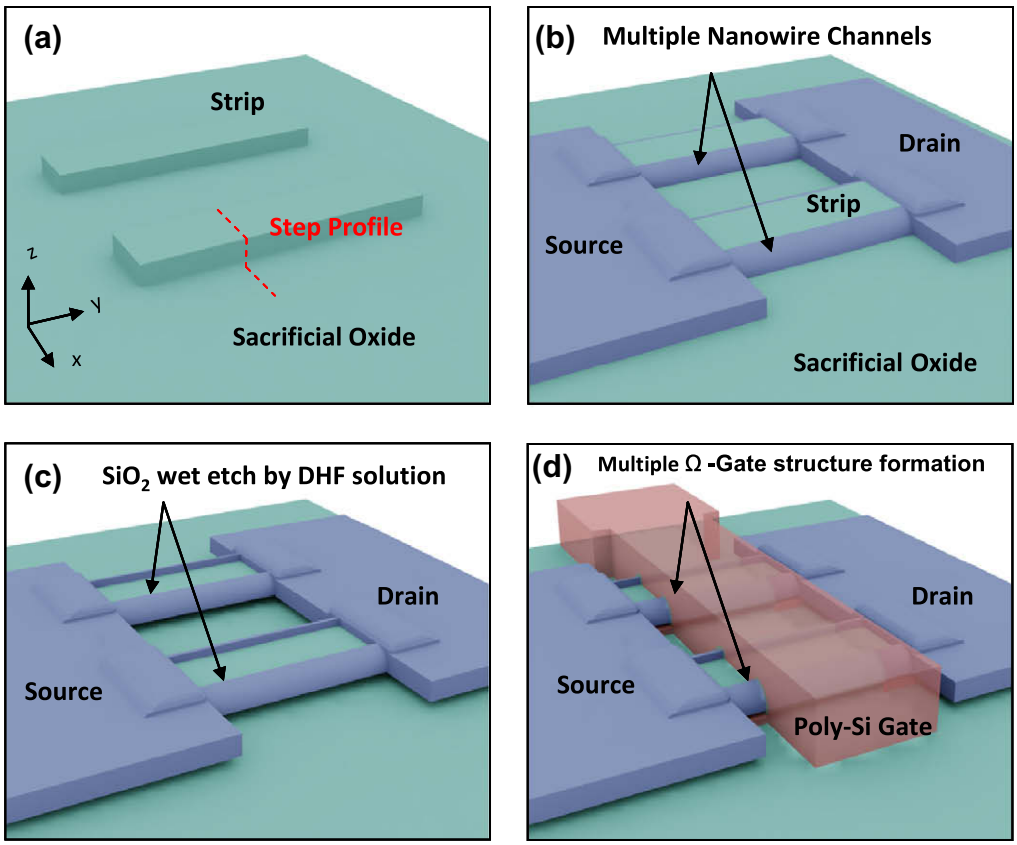

Fig. 1. Schematic diagrams of the fabrication process steps of the proposed Ω-Gate TFT SONOS: (a) the patterning of the dummy-oxide strips; (b) after source/drain (S/D)-pad lithography and its RIE process, couples of spacer nanowires were *in situ* resided against the sidewall of those designed strips and naturally connected to the S/D pads, which were formed to be the device active region, (c) the diluted hydro-fluoric acid (DHF) solution was used to etch the SiO_2 strip for 25-nm-thick, and (d) the gate electrode patterning.

ends of those dummy strips, and followed by an anisotropic RIE process to remove a-Si layer; meanwhile, pairs of a-Si sidewall spacer with a common source/drain (S/D) pad were *in situ* resided against both sidewalls of SiO_2 dummy strips (Fig. 1b). The a-Si film was then transferred into poly-Si by solid phase crystallization at 600 °C for 24 h in N_2 ambient. Next, the diluted hydro-fluoric acid (DHF) solution was used to etch the SiO_2 strip for 25-nm-thick, thus the external two sharp corners were exposed and the other one was still bound with the reminder SiO_2 strip to support the poly-Si nanowire (Fig. 1c).

Afterwards, the oxide–nitride–oxide (ONO: 3 nm/10 nm/6 nm) layer and 200-nm-thick phosphorous *in situ* doped poly-Si (with a doping level of 5×10^{19} cm^{-3}) were sequentially deposited to encompass two sharp corners and bevel edge of poly-Si spacer nanowires by LPCVD system. Fig. 2 shows the cross section transmission electron microscopy (XTEM) image of poly-Si spacer nanowire covered with ONO dielectrics and poly-Si Ω-Gate. According to XTEM photograph, the gate-covered width of the fabricated device was 168 nm. It was worth mentioning that the Ω-Gate poly-Si TFT SONOS was fabricated by simple sidewall spacer formation without any advanced lithography [6,7]. Subsequently, the *in situ* doped poly-Si was patterned and etched to form the gate electrode (Fig. 1d). After self-aligned phosphorous S/D implantation (at 30 keV to a dose of 5×10^{15} cm^{-2}), the 300-nm-thick passivation oxide deposition and S/D activation were sequentially performed. Finally, the contact opening and metallization were progressed. For the purpose of comparison, the conventional planar (CP) poly-Si TFT SONOS memory devices were also manufactured by using the same process sequence.

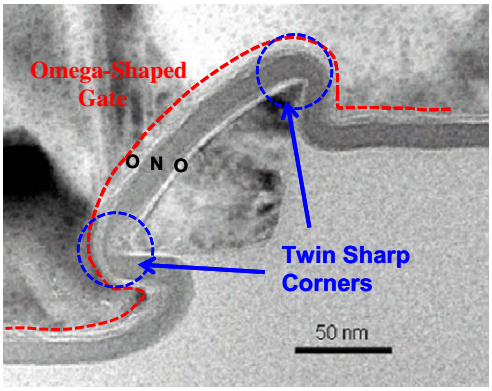

Fig. 2. The cross section transmission electron microscopy (XTEM) image of the Ω-Gate TFT SONOS structure with ONO dielectric conformally deposited on the two sharp corners and bevel edge of poly-Si spacer nanowires.

3. Results and discussion

The Fowler–Nordheim (FN) tunneling mechanism was employed in this paper for both the Ω-Gate and CP-TFT SONOS memory operations. For the programming and erasing operation, positive and negative voltage pulses were given at $V_{GS} = \pm 12$ V while S/D was grounded. The gate length (L) and channel width (W) of measured device were 1 μm and 2.7 μm, accordingly. The channel width of Ω-Gate TFT SONOS was defined by 16 nanowires with 8-strips structure [10].

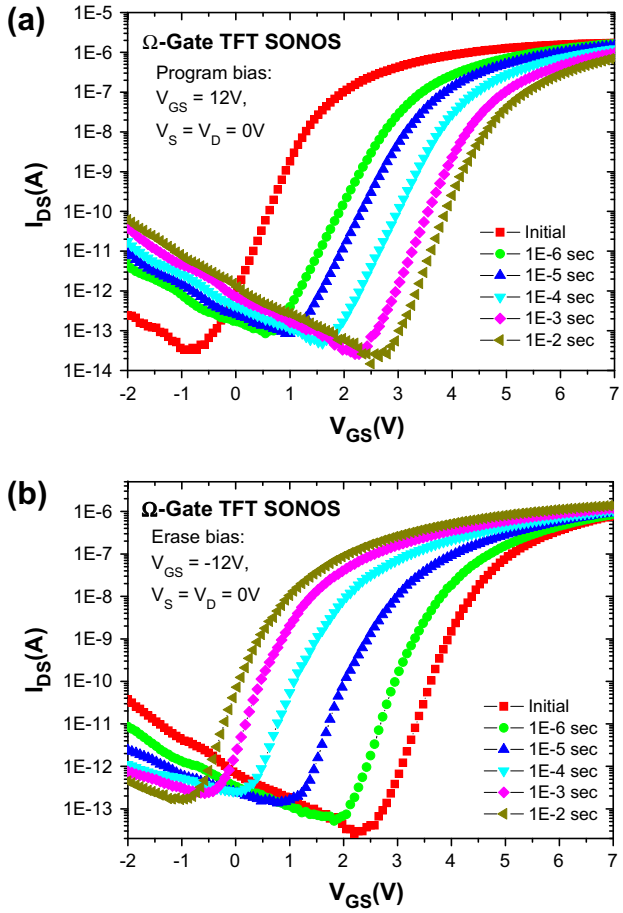

Fig. 3. The I_{DS}–V_{GS} curves of Ω-Gate TFT SONOS with: (a) programming and (b) erasing operation at V_{GS} = ±12 V.

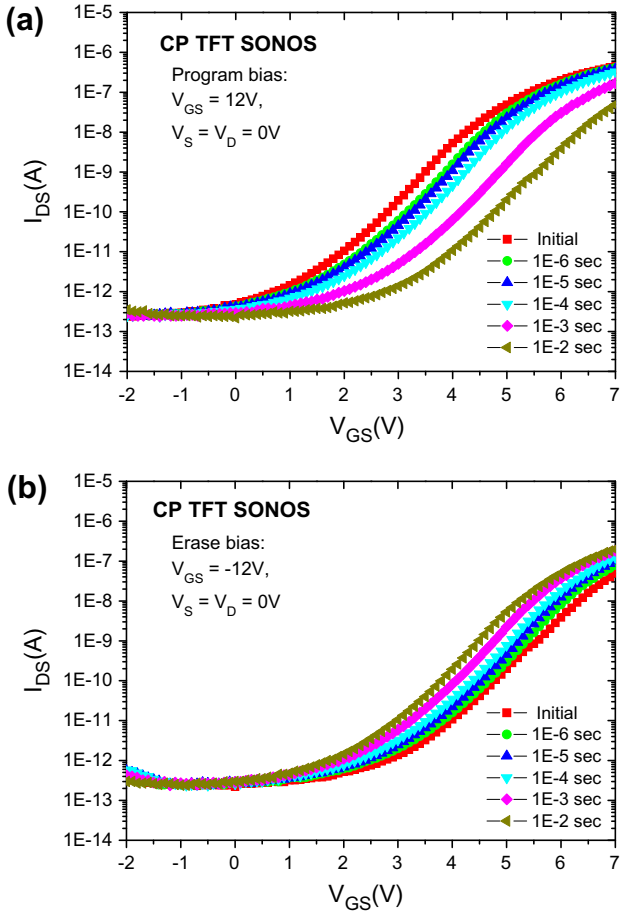

Fig. 4. The I_{DS}–V_{GS} curves of CP-TFT SONOS with: (a) programming and (b) erasing operation at V_{GS} = ±12 V.

The threshold voltage (Vth) was extracted by the constant drain current method and threshold current was specified at 10 nA × (W/L) for V_{DS} = 0.1 V. Figs. 3 and 4 present the measured transistor and memory characteristics of both Ω-Gate and CP-TFT SONOS devices, correspondingly. The initial Vth and subthreshold swing (SS) were 4.24 V and 635 mv/decade for the CP-TFT, while those values were 1.17 V and 289 mv/decade for the Ω-Gate TFT. It could be found that the transfer characteristics of fresh Ω-Gate SONOS displayed larger on-current, smaller Vth and SS, as compared to CP devices. This was because the Ω-Gate structure possessed superior gate control capability by means of 3D device geometry [7].

Fig. 5a and b shows the programming and erasing speeds of the Ω-Gate SONOS and CP SONOS, respectively. For the programming operation, the Ω-Gate SONOS exhibited a larger Vth shift of 3.02 V in 1 ms as compared to that of 1.34 V for CP one. Furthermore, the erase characteristics also showed the similar trend that the Ω-Gate SONOS devices were much faster (a Vth shift of 2.97 V in 1 ms) than the CP counterparts (a Vth shift of 0.84 V in 1 ms). As seen clearly, the Vth shift of Ω-Gate SONOS in 1 μs programming time at V_{GS} = 12 V was 1.46 V, while CP SONOS required more than 1 ms programming time to achieve the identical Vth shift of Ω-Gate SONOS. Therefore, the programming speed of Ω-Gate SONOS at V_{GS} = 12 V was about 1000 times larger than that for CP device, and the erasing speed of Ω-Gate SONOS at V_{GS} = 12 V was nearly 100 times higher than that for CP one. Since during the Ω-Gate SONOS operation, the local electric field of channel/tunneling oxide interface could be enhanced effectively through the two sharp corners and thereby improve the P/E efficiency. Additionally, the electric field in the blocking oxide was deservedly diminished accompanying the suppression of electron back-injection from the gate [11]. In contrary, the CP SONOS structures did not have such corner effect; hence displayed the poor P/E activity. The endurance characteristics of Ω-Gate SONOS under a program bias of 10 V for 1 ms and erase bias of −12 V for 1 ms are shown in Table 1. The Ω-Gate SONOS revealed a good endurance that the memory window was well maintained with a small reduction after 10 K P/E cycles. One point was worth making about Table 1, since the trap charges in the deep level traps of silicon nitride were not easy to remove, both the Vth of program and erase states were shifted slightly upward with cycling stress [7]. After memory operation, it was desirable to maintain the data as long as possible. Consequently, it was important to estimate the memory window for over 10 years. Fig. 6 shows the retention characteristics of Ω-Gate SONOS after 1 cycle and 10 K cycles. The memory window of 10 K cycles would be remained 1.1 V after extrapolating to retention time of 10 years, which was almost equal to the memory window of 1 cycle (1.2 V).

Table 1
The endurance characteristics of Ω-Gate TFT SONOS with a program bias of 10 V for 1 ms and an erasing bias of −12 V for 1 ms.

P/E cycles (times)	1E0	1E1	1E2	1E3	3E3	5E3	1E4
Program state (V)	3.02	3.09	3.20	3.29	3.34	3.37	3.40
Erase state (V)	0.3	0.42	0.57	0.75	0.97	1.06	1.25

In order to demonstrate the enhancement of the sharp-corner electric field across the ONO dielectrics in the Ω-Gate SONOS, a numerical simulation was also carried out using ISE. Fig. 7

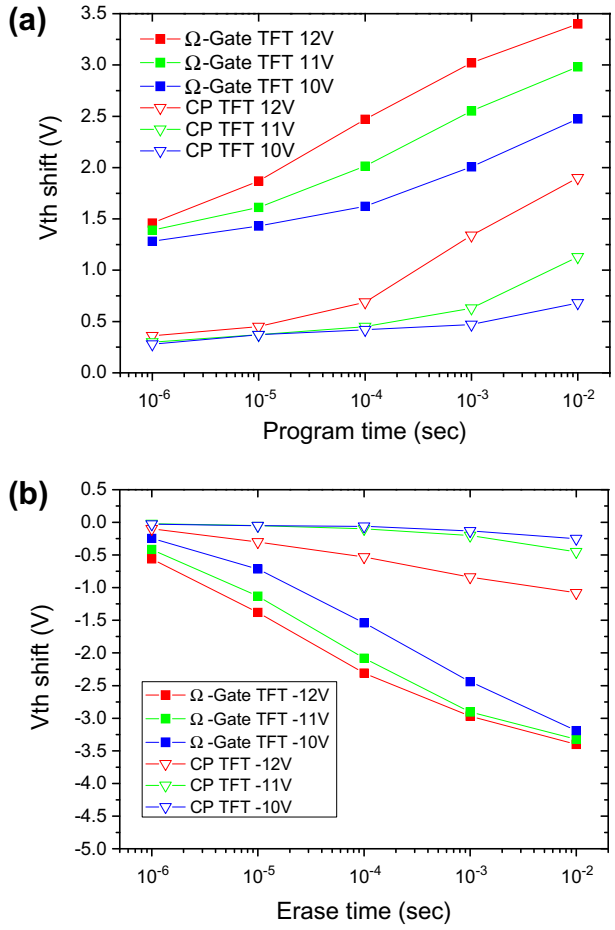

Fig. 5. (a) Programming and (b) erasing speed comparison of Ω-Gate TFT SONOS and CP-TFT SONOS at V_{GS} = ±10 V ~ ±12 V.

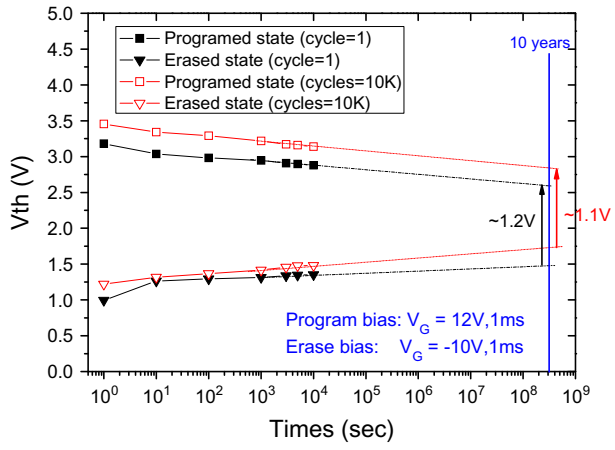

Fig. 6. The retention characteristics of Ω-Gate TFT SONOS. The memory window of 10 K cycles would be remained 1.1 V after extrapolating to retention time of 10 years.

displays the simulated electrical field distribution of both the Ω-Gate and CP SONOS across the stacked gate dielectrics at V_{GS} = 12 V. The sharp geometry of these two corners enhanced the local electric field (to be ~40 MV/cm) at the channel/tunneling oxide interface, which was about 4.5 times higher for the Ω-Gate SONOS to the CP device (to be ~8.7 MV/cm). The remarkable

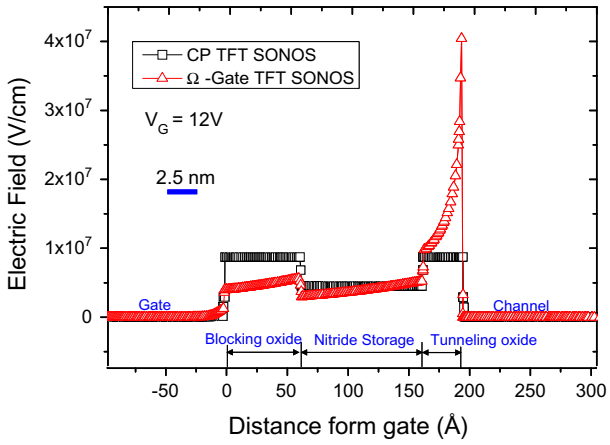

Fig. 7. The distribution of electrical field across the stacked ONO dielectrics for the Ω-Gate TFT SONOS and CP-TFT SONOS at V_{GS} = 12 V for programming operation.

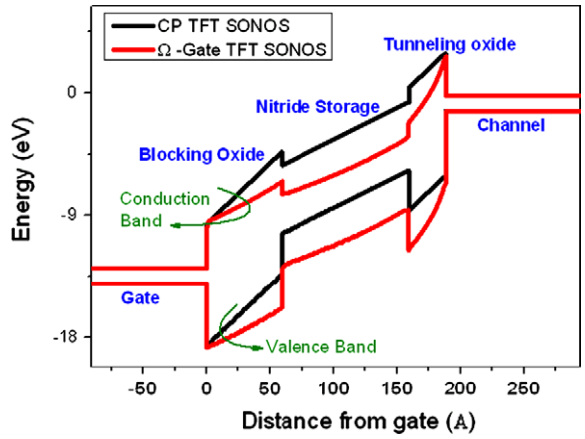

Fig. 8. The energy band diagrams of Ω-Gate and CP-TFT SONOS at V_{GS} = 12 V for programming operation.

electric field promotion at the channel/tunneling oxide interface enhanced the carrier-injection current into the nitride storage layer [12]. Moreover, the much lower electric field at the blocking oxide of Ω-Gate SONOS revealed that electron back-injection from gate could be depressed effectively. Since the *P*/*E* activity was favorable between the channel and tunneling oxide rather than between the blocking oxide and the gate, the Ω-Gate SONOS expressed better *P*/*E* efficiency which was consistent with experimental results. Instead, the electric field (~8.7 MV/cm) at tunneling oxide of CP SONOS was always equal to the blocking oxide, leading to lower the efficiency. Fig. 8 shows the simulated energy band diagram at V_{GS} = 12 V. The electrons tunneling barrier width of Ω-Gate SONOS was much shorter than CP SONOS. Due to the tunneling probability was increased exponentially with the tunneling length reduction, the Ω-Gate SONOS could provide greater memory window shift than that of the CP device.

4. Conclusions

A novel Ω-Gate TFT SONOS fabricated by a simple sidewall spacer formation has been demonstrated for the first time with better transistor performance owing to the enhanced gate controllability. In addition, the Ω-Gate TFT SONOS also exhibited superior memory characteristics with a faster Vth shift of 3.02 V and 2.97 V at V_{GS} = ±12 V in 1 ms for programming and erasing operations, respectively. The dramatic improvement was attributed to the

effective field enhancement at the two sharp corners and the suppressed electric field in the blocking oxide. The device simulation highlighted a larger electric field of external corner region could be obtained by the proposed Ω-Gate SONOS. Furthermore, the Ω-Gate TFT SONOS also revealed reasonable endurance and data retention characteristics. Such an Ω-Gate TFT SONOS memory would be very promising for the embedded NVM on the future SOP applications.

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