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Formation of stacked Ni silicide nanocrystals for nonvolatile memory application

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The formation of stacked Ni silicide nanocrystals by using a comixed target is proposed in this letter. High resolution transmission electron microscope analysis clearly shows the stacked nanocrystals embedded in the silicon oxide. The memory window enough to define "1" and "0" states is obviously observed at low voltage programming conditions, and good data retention characteristics are exhibited for the nonvolatile memory application. A physical model is also proposed further to explain the saturation phenomenon of threshold voltage at different programming voltages with operation duration. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2713177]

Recently, the requirements of memory device are the high density cells, low power consumption, high-speed operation, and good reliability. All of the charges stored in a floating gate will leak to the substrate if there is a leakage path in the tunnel oxide in the conventional floating gate (FG) memory device. Thus, the tunnel oxide thickness is difficult to scale down for the consideration of charge retention and endurance characteristics.[1,2] Memory-cell structures employing discrete traps as the charge storage media have been attracted as promising candidates to replace conventional FG nonvolatile memory for the device scaling down.[3–5] The metal nanocrystal nonvolatile memory (NVM) device desires several advantages, such as stronger coupling with the conduction channel and a wide range of available work functions.[6,7] Therefore, the requirements of obvious memory effect and low power consumption can be realized in a metal nanocrystal NVM. In the present research, the nickel silicon (Ni_xSi_{1-x}) nanocrystal was widely studied using cosputtering method (two targets used). However, it is difficult to uniformly control the component of the deposited nickel silicon thin film. Hence, the size and uniformity of nickel silicon nanocrystal were critically affected.[8] In this study, an easy process for nickel silicon nanocrystal formation will be proposed by the deposition of nickel silicide nanocrystals at low fabrication temperature.[9] The component of the Ni_xSi_{1-x} film can be well controlled using a comixed target with a fixed component ratio and compatible with current fabricating process of the integrated circuit manufacture.

4 in. *p*-type silicon wafers with (100) orientation were cleaned with a standard RCA process, followed by a dry oxidation process in an atmospheric pressure chemical vapor deposition furnace to form a 3-nm-thick tunnel oxide. Subsequently, an 8-nm-thick Ni_xSi_{1-x} ($x=0.3$) layer was deposited onto the tunnel oxide by sputtering a Ni_xSi_{1-x} ($x=0.3$) mixed target at the 80 W dc power. Then the Ni_xSi_{1-x} ($x=0.3$) layer was capped by a 20-nm-thick amorphous silicon (*a*-Si) layer deposited by sputtering a Si target in the oxygen environment. This step can obtain an oxygen-incorporated *a*-Si layer, as shown in Fig. 1(a). A rapid thermal oxidation (RTO) at 500 °C for 30 s was executed to oxidize the oxygen-incorporated *a*-Si layer, leading to improved quality of the blocking oxide. In addition, the deposited Ni_xSi_{1-x} ($x=0.3$) layer is precipitated to Ni silicide nanocrystals during the RTO process. Al gate electrode was finally patterned to form a metal/oxide/insulator/oxide/silicon (MOIOS) structure. High resolution transmission electron microscope (HRTEM) was adopted for the microstructure analysis. Electrical characteristics, including the capacitance-voltage (*C-V*) hysteresis, program efficiency, and retention characteristics, were also performed. The capacitance-voltage (*C-V*) characteristics were measured at a high frequency of 100 kHz by HP4284 Precision *LCR* meter.

A cross-sectional HRTEM of the oxide/Ni silicide nanocrystals/oxide stacked structure is shown in Fig. 1(d). The spherical and separated Ni silicide nanocrystals with a size of 4–6 nm are clearly observed embedded in the silicon oxide layer. The distributed aerial density of the nanocrystals is about 2.67×10^{12} cm^{-2} estimated by HRTEM analysis. The large charge storage ability at scaled-down devices can

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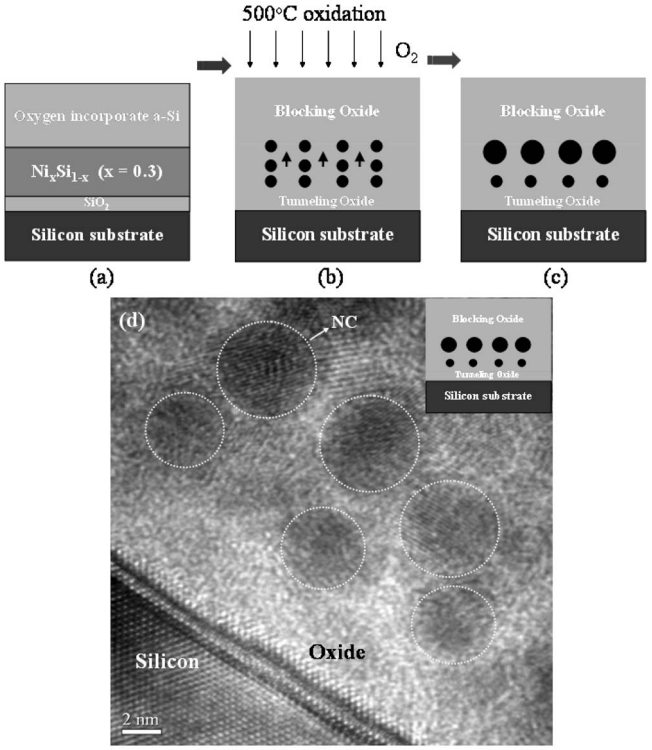

FIG. 1. Schematic of (a) as deposition for a silicon substrate/SiO_2/Ni_xSi_{1-x} (x=0.3)/oxygen-incorporated $a-$Si structure, (b) deposited Ni_xSi_{1-x} (x =0.3) layer precipitated to Ni silicide nanocrystals and oxygen-incorporated a-Si layer oxidized to form the blocking oxide during the RTO process, and (c) stacked Ni silicide nanocrystals embedded in silicon oxide after RTO process at 500 °C for 30 s. (d) Cross-sectional HRTEM analysis of stacked Ni silicide nanocrystals. The sizes of the nanocrystals (from substrate to blocking oxide) and density are 4–6 nm and 2.67×10^{12} cm^{-2}, respectively.

be maintained for the stacked structure with nanocrystals embedded in the dielectric.[10] Furthermore, the improved retention characteristics can be also maintained as electrons stored in the nanocrystals near the blocking oxide.[11]

Figure 1 exhibits the formation of stacked Ni silicide nanocrystals embedded in silicon oxide after a RTO process at 500 °C. It is observed that the stacked structure with nanocrystals embedded in the dielectric can be easily formed by oxidation at low temperature. In the initial stage, the oxidation process completely oxidizes the oxygen-incorporated a-Si layer. The size of the Ni silicide nanocrystals near the blocking oxide is obviously larger than that at the surface of the tunnel oxide due to the thermal driving of Ni atom during the blocking oxide formation [Figs. 1(b) and 1(c)].[12] Then, the Ni silicide nanocrystals are confined and separated between the tunnel oxide and blocking oxide, as shown in the HRTEM analysis of Fig. 1(d).

Figure 2 exhibits the capacitance-voltage (C-V) hysteresis after the bidirectional voltage sweeping from 5 to−5 V and from −5 to 5 V. It is clearly indicated that a 1.77 V memory window can be obtained under 5 V operation, which is suitable for the application of a low power device. It is perceived that the hysteresis is counterclockwise, due to injection of electrons from the deep inversion layer and discharge of electrons from the deep accumulation layer of Si substrate.[13]

The charge retention characteristics of the stacked structure with Ni silicide nanocrystals are shown in Fig. 3. The retention characteristics were investigated at room temperature using the constant gate voltage stress for 10 s and the charge density was estimated by C-t (*capacitance to time*) measurements.[14] When carriers are stored in the nanocrystals, the stored charges will raise the nanocrystal potential energy and increase the probability of escaping from the nanocrystal to the silicon substrate.[15] Therefore, the electron and hole densities are observed to decay exponentially with time before 1000 s, resulting in charge loss of 20% for electrons and 50% for holes. It can also be observed that hole has lower charge density than electron. Because some holes are stored in the shallow trap state of silicon oxide (SiO_x) around the nanocrystals, they are unstable and can easity escape from the shallow trap of SiO_x to the silicon substrate. However, partial carriers can be conserved and the memory window also can be retained, 1.9 V for electron density and 1.2 V for hole density, respectively. It is considered that the Ni silicide nanocrystals have larger work function than the silicon substrate. In addition, it is forecasted that the carriers that are stored in the nanocrystals can be kept for 10 y.

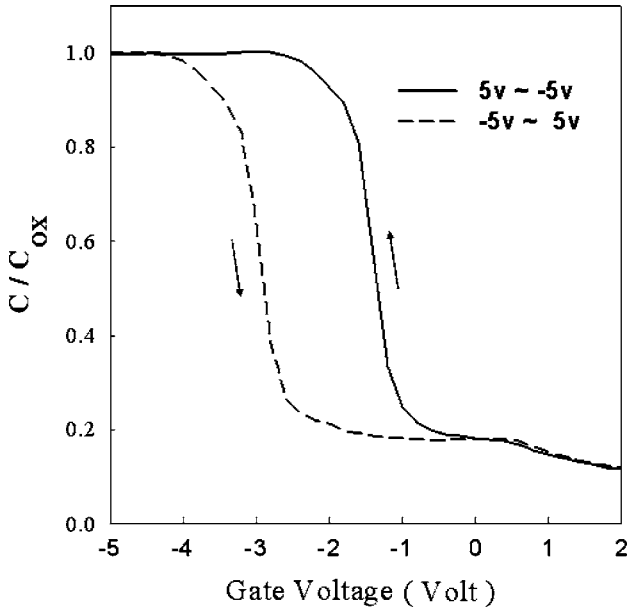

FIG. 2. Capacitance-voltage (C-V) hysteresis of the MOIOS structure after the bidirectional voltage sweeps from 5 to −5 V and from −5 to 5 V.

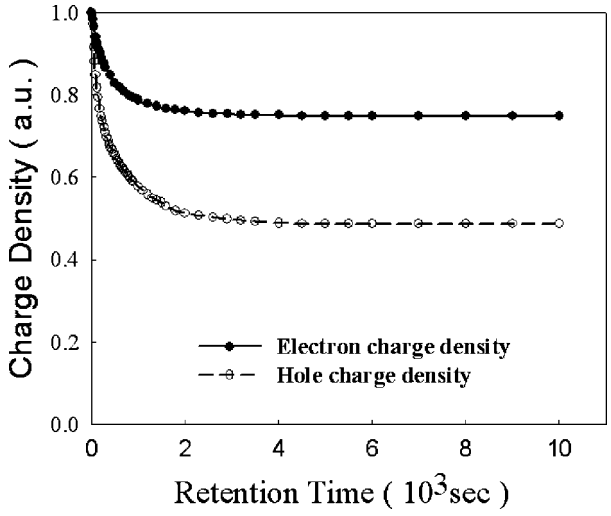

FIG. 3. Charge retention characteristics of the stacked structure with Ni silicide nanocrystals.

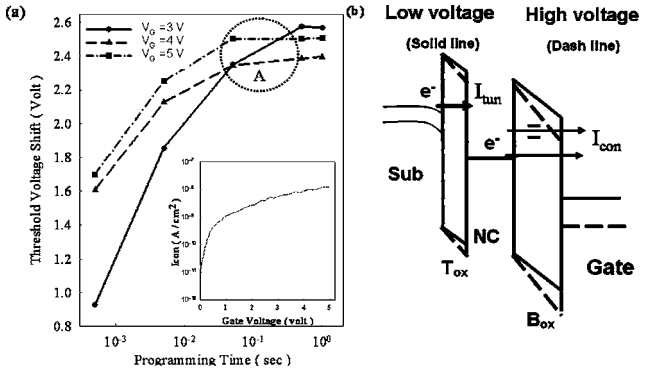

FIG. 4. (a) Programming characteristics of nanocrystal memory device at different gate programming voltages. (b) Schematic band diagram of the MOIOS structure operated at low voltage (solid line) and high voltage (dash line).

The programming characteristics of stacked Ni silicide nanocrystals are shown in Fig. 4(a). The threshold voltage shift (ΔV_{th}) increased as the programming voltage increased at the same programming duration and also increased with the increasing programming duration at the same programming voltage. However, it is found that the threshold voltages are saturated as the programming duration is longer than 50 ms at the voltages of 4 and 5 V. As compared to the 4 and 5 V programming operations, the larger memory window was found at a programming voltage of 3 V for long programming duration (as shown in region A). As analyzed theoretically in previous research,[16] there are two components of electron current flow in the nanocrystal memory structure. One is the current between the substrate and the nanocrystals (I_{tun}) and the other is between the nanocrystals and the control gate [I_{con}, as shown in the inset of Fig. 4(a)]. The threshold voltage should be saturated as I_{tun} and I_{con} are at steady state. As the programming voltage is increased, partial electrons are lost to the gate electrode via Fowler-Nordheim tunneling and the trap assisted tunneling mechanism as shown in Fig. 4(b). The trap assisted tunneling process dominates at high voltage operation for the oxidized *a*-Si serving as a blocking oxide, due to obtaining a linear relation between $\ln(I_{con})$ and gate voltage (3–5 V) by the trap assisted tunneling model.[17] The trap state generation resulted from the low temperature formation of the blocking oxide (oxidized oxygen-incorporated *a*-Si layer). A lot of charge storage centers are thereby formed in the stacked nanocrystals-embedded device structure. In contrast, the trap states in the blocking oxide cause a larger memory window at low programming voltage, which is larger than the high programming voltage for long programming duration.

In conclusion, the stacked Ni silicide nanocrystal memory was fabricated by sputtering a comix target followed by a low temperature (at 500 °C for 30 s) RTO process. A larger memory window of 1.77 V was observed after ±5 V voltage sweep. The trap states in the blocking oxide cause the larger memory effect at low voltage as the memory window is saturated at high programming voltage. The saturation phenomenon of threshold voltage was reasonably explained by a proposed mechanism. The date retention of the nanocrystal memory device is also good enough to be maintained for 10 y.

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