Low-Temperature Polycrystalline Silicon Thin-Film Flash Memory With Hafnium Silicate

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***Abstract*—In this paper, we have successfully fabricated poly-Si-oxide–nitride–oxide–silicon (SONOS)-type poly-Si-thin-film transistor (TFT) memories employing hafnium silicate as the trapping layer with low-thermal budget processing ($\leq 600\ ^{\circ}C$). It was demonstrated that the fabricated memories exhibited good performance in terms of relatively large memory window, high program/erase speed (1 ms/10 ms), long retention time ($> 10^6$ s for 20% charge loss), and 2-bit operation. Interestingly, we found that these memories depicted very unique disturbance behaviors, which are obviously distinct from those observed in the conventional SONOS-type Flash memories. We thought these specific characteristics are closely related to the presence of the inherent defects along the grain boundaries. Therefore, the elimination of the traps along the grain boundaries in the channel is an important factor for achieving high performance of the SONOS-type poly-Si-TFT Flash memory.**

***Index Terms*—Flash memory, hafnium silicate, nonvolatile memories, polycrystalline silicon thin-film transistor (poly-Si-TFT).**

I. Introduction

POLYCRYSTALLINE silicon thin-film transistors (poly-Si-TFTs) have been widely used for the application of active-matrix liquid-crystal displays [1]. Recently, with the rapid advancement of the manufacturing technologies, the extent of complexity of circuit integration has been tremendously increased. Also, owing to the low-temperature processing of the poly-Si-TFTs, the realization of integrating an entire system on top of the panel is then being rigorously pursued [2]–[6]. With inherent superior performance over their counterparts, i.e., amorphous-Si-TFTs, poly-Si-TFTs have better opportunity to achieve integration of analog- and digital-display driver circuits as well as other peripheral functions on the active-matrix substrate with enhanced display functionality, performance, and reliability. Since a system shall include the functionality of memory, great efforts shall be paid in order to successfully integrate the memories, such as EEPROM and Flash memory, directly on the panel [7]–[11]. In the memory application, the poly-Si-oxide–nitride–oxide–silicon (SONOS)-type nonvolatile memory based on discrete-storage nodes possesses great potential for achieving large memory windows, high program/erase speed, low programming voltage, low-power performance, excellent retention, and good disturb characteristics [12].

In this paper, we present the poly-Si-TFT Flash memories by using high-κ dielectric, i.e., Hf-silicate, for the trapping layer. By employing low-thermal cycle (600 °C, 24 h) for post high-κ deposition annealing and S/D activation, the proposed nonvolatile memory fabrication is fully compatible with the current mass-production TFT processing. This feature makes the realization of producing the embedded nonvolatile memories on the panel become feasible. Owing to the relatively high trap density of the Hf-silicate layer and the sufficiently large band gap offset between Hf-silicate and SiO_2, our memory devices, using Hf-silicate as the trapping layer, exhibit good characteristics, such as sufficiently large memory window, high program/erase speeds, long retention time, and good endurance. Owing to the discrete-storage capability, we also have successfully demonstrated the 2-bit operation in a single memory cell. Finally, we found that these memories displayed very unique disturbance behaviors, which are obviously distinct from those observed in the conventional SONOS-type Flash memories. We speculated that these specific characteristics are intimately linked to the presence of the inherent defects along the grain boundaries. Therefore, to effectively reduce the amount of traps along the grain boundaries in the channel is an important factor for achieving high performance of the SONOS-type poly-Si-TFT Flash memory.

II. Device Fabrication

The device cross section of the high-κ dielectric poly-Si-TFT nonvolatile memories is illustrated in Fig. 1. First, 500-nm-thick thermal oxide was grown on the Si wafers by furnace system to substitute for the glass substrate, and all the experimental devices in this paper were fabricated on thermally oxidized Si wafers. Then, a 100-nm-thick amorphous-silicon layer was deposited on thermally oxidized Si wafer by dissociation of SiH_4 gas in a low-pressure chemical-vapor deposition (LPCVD) at 550 °C. Subsequently, solid-phase crystallization was performed at 600 °C for 24 h in N_2 ambient for the phase transformation. Individual active regions were then patterned and defined. After a standard RCA cleaning, tetra-ethyl-oxy-silane (TEOS) oxides with two different thicknesses were deposited;

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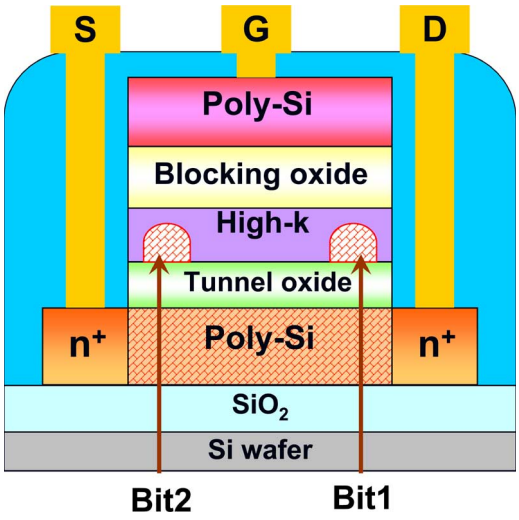

Fig. 1. Device cross section of the high-κ dielectric poly-Si-TFT nonvolatile memories and illustration of 2-bit operation.

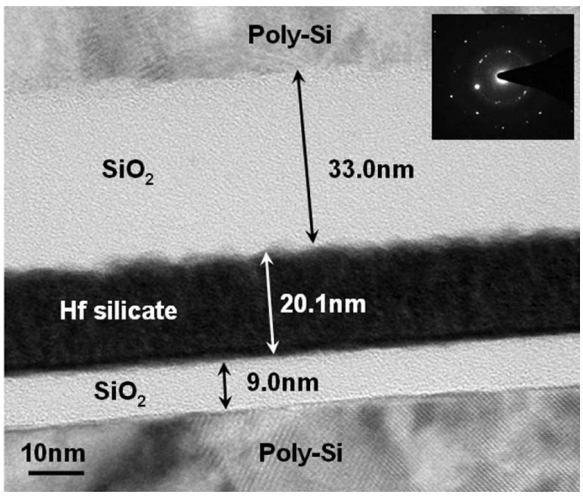

Fig. 2. Cross-sectional HRTEM image of the gate stack for the poly-Si-TFT memories with Hf-silicate trapping layer. Inset shows the corresponding diffraction pattern.

one is of around 9 nm and the other is of 20 nm. The following deposition of hafnium silicate thin films was conducted by cosputtering method. A blocking oxide of about 33 nm was then deposited by PECVD at 350 °C. A 200-nm-thick poly-Si was deposited to serve as the gate electrode by LPCVD. Then, gate electrode was patterned and the regions of source, drain, and gate were doped by a self-aligned phosphorous ion implantation at the dosage and energy of 5×10^{15} ions/cm^{-2} and 40 keV, respectively. After S/D formation, which was activated at 600 °C for 24 h, passivation, metallization, and NH_3 plasma sintering were performed to complete the fabrication of the poly-Si-TFT memories.

Fig. 2 shows the cross-sectional high-resolution transmission electron microscopy (HRTEM) image of gate stack of the poly-Si-TFT memory. The thicknesses of the tunnel oxide and blocking oxide layer were 9 and 33 nm, respectively, and the Hf-silicate trapping layer thickness was around 20 nm. The inset on the up–right corner shows the corresponding diffraction pattern. It is observed that the Hf-silicate film depicts only slight

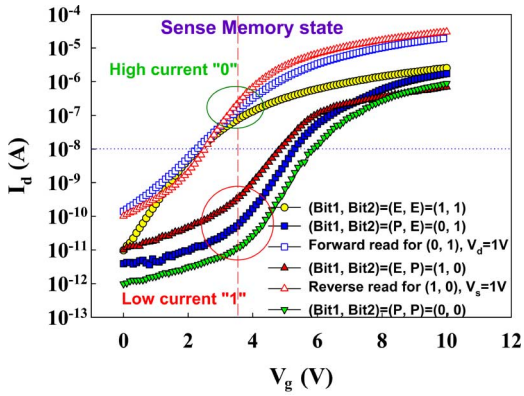

Fig. 3. I_D-V_G curves for the 2-bit operation. E stands for the erased state. P denotes the programmed state. Bit1 locates at the drain side. Bit2 locates at the source side.

TABLE I
OPERATION PRINCIPLES AND BIAS CONDITIONS UTILIZED DURING THE OPERATION OF THE POLY-SI-TFT FLASH MEMORY CELL

		Program	Erase	Read
Bit 1	V_g	12V	-10V	3V
	V_d	12V	10V	0V
	V_s	0V	0V	1V
Bit 2	V_g	12V	-10V	3V
	V_d	0V	0V	1V
	V_s	12V	10V	0V

crystallization, implying the content of Hf element is slightly rich. Hence, in order to have better thermal stability, further tuning of the composition of Hf-silicate shall be conducted [13], [14]. For the operation of our poly-Si-TFT memories, we employed channel hot-electron injection and band-to-band hot-hole injection for the programming and erasing, respectively. All devices described in this paper had dimensions of $L/W = 1/1.5$ μm. Fig. 3 demonstrates the feasibility of performing 2-bit operation in our poly-Si-TFT memories through forward-read and reverse-read scheme in a single cell [7]. From the $I_{\rm ds}-V_{\rm gs}$ curves, it is obvious that we use the forward-read to measure the $I_{\rm ds}-V_{\rm gs}$ curve of the four states; (1, 1), (1, 0), (0, 1), and (0, 0). For the (1, 0) and (0, 1) state, we can use reverse-read to detect the information stored in the programmed Bit1 and Bit2. Both Bit1 and Bit2 were programmed at the bias condition of $V_d = V_g = 12$ V with a programming time of 1 ms and erased at the bias condition of $V_d = 10$ V and $V_g = -10$ V with an erasing time of 10 ms. The read operation was achieved using a reverse-read scheme with $V_d = 1$ V and $V_g = 3.5$ V. Table I summarizes the bias conditions for 2-bit operation.

III. RESULTS AND DISCUSSION

Fig. 4 shows the programming and erasing characteristics, respectively, of the fabricated poly-Si-TFT Flash memories with two different tunnel oxide thicknesses. We programmed with the bias condition at $V_g = 12$ V and $V_d = 12$ V and erased with the bias condition at $V_g = 10$ V and $V_d = -10$ V. We observed that the memory with thinner tunnel oxide exhibited slightly improved programming speed when they were operated

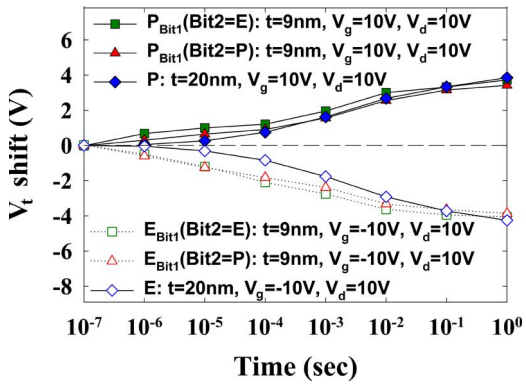

Fig. 4. Programming and erasing speed characteristics of the poly-Si-TFT memories as a function of bias condition. Programming time can be as short as 1 ms, if the window margin is set to 3 V with $V_g = V_d = 12$ V. Erasing time is about 10 ms. Bit2 $= 0$ stands for the Bit2 is in programmed state.

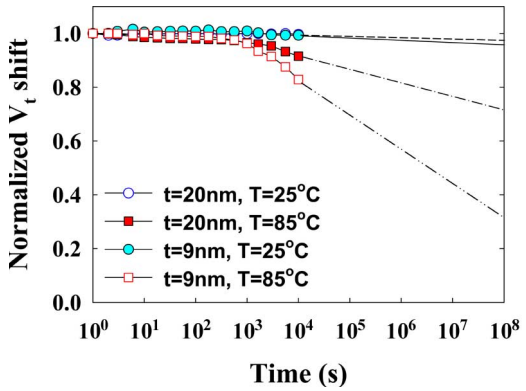

Fig. 5. Retention characteristics of the fresh poly-Si-TFT memory devices with two different tunnel oxide thicknesses at $T = 25$ °C and $T = 85$ °C.

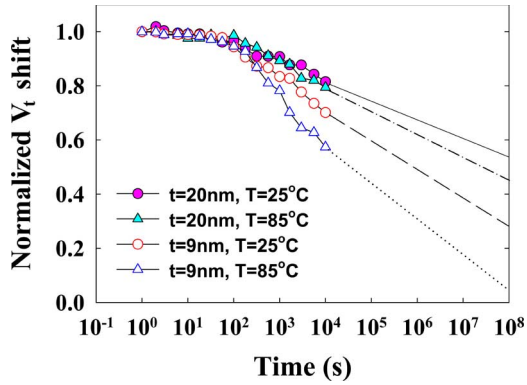

Fig. 6. Retention characteristics of the 10-k P/E cycled poly-Si-TFT memories with two different tunnel oxide thicknesses at $T = 25$ °C and $T = 85$ °C.

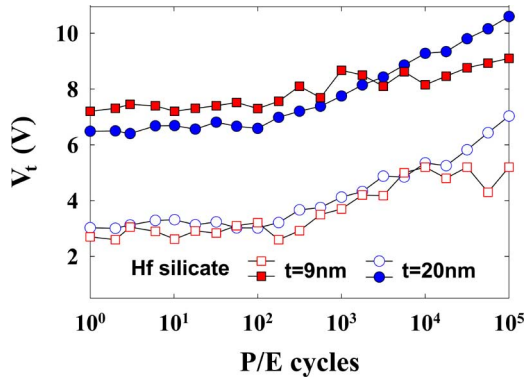

Fig. 7. Endurance characteristics of the poly-Si-TFT memories with two different tunnel oxide thicknesses.

with the short pulse widths and better erase performance. However, there was almost no difference in programming rate between two splits as if the $V_{\rm th}$ shift was set at 3 V. The tendency seems reasonable, because the larger positive field across the thinner oxide favored electron injection during channel-hot-electron programming. However, this advantage of higher injection efficiency was gradually deteriorated when the electron population became larger due to the combining effects of the repelling force and the smaller lateral acceleration field. Therefore, we think that thinner tunnel oxide is only beneficial in the erase operation but not in program operation. Fig. 5 illustrates the retention characteristic of the fresh poly-Si-TFT Flash memories with two different tunnel oxide thicknesses at different testing temperatures. For both cases, the retention times can be extrapolated up to more than 10^8 s for 10% charge loss at room temperature. Such good retention performance can be ascribed to the sufficiently deep trap energy levels in hafnium silicate [15]. However, the capability of charge storage became much worse and depicted obvious thickness dependence as the temperature increased; after 10^8 s 29% and 68% charge losses for the samples with thick and thin tunnel oxide was detected. With the testing at the third temperature (not shown), we can calculate the activation energy of the traps in the hafnium silicate for the fresh device [16]. For a given charge-loss threshold criterion (in our case, 20%), the obtained failure rate can then be extrapolated to the nominal operating condition. The extracted activation energies are 1.04 and 1.33 eV for the 9- and 20-nm samples, respectively. Obviously, these values lie in the higher ranges of those scattered values previously reported for the conventional SONOS memories [17]–[19]. Therefore, we thought that the sample with thick tunnel oxide can be employed for achieving better charge-keeping capability. Fig. 6 illustrates the retention characteristics of the 10-k P/E cycled poly-Si-TFT memory devices at $T = 25$ °C and $T = 85$ °C. As expected, the retention characteristic degraded significantly after 10-k P/E cycling. Also, its dependence on the testing temperature is basically consistent with that in the previous figure for the fresh devices. The retention got worse as the temperature increased; 56% and 70% charge losses for the samples with thick and thin tunnel oxide, respectively, were extracted by extrapolating to 10^8 s. Clearly, the memory device with thick tunnel oxide had better charge-keeping capability after 10-k P/E cycling. Therefore, in pursuit of superior performance in charge-storage capability of these new poly-Si-TFT memories, nanodots formation for increasing the retention characteristics [20], if the thermal cycle is feasible, and very high-quality tunnel oxide are highly recommended since nanodots and high-quality oxide have better charge-storage capability.

The endurance performances of the 10-k P/E cycled poly-Si-TFT memory devices are shown in Fig. 7. The programming and erasing conditions are $V_g = V_d = 12$ V for 1 ms and $V_g = -10$ V, $V_d = 10$ V for 10 ms for both samples,

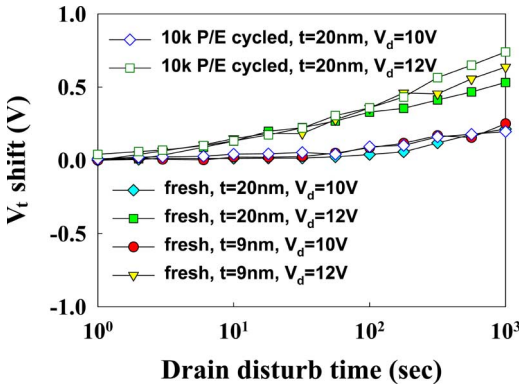

Fig. 8. Drain disturbance characteristics of the poly-Si-TFT memory devices with two different tunnel oxide thicknesses. After 1000 s at 25 °C, around 0.7 V drain disturb margin was observed.

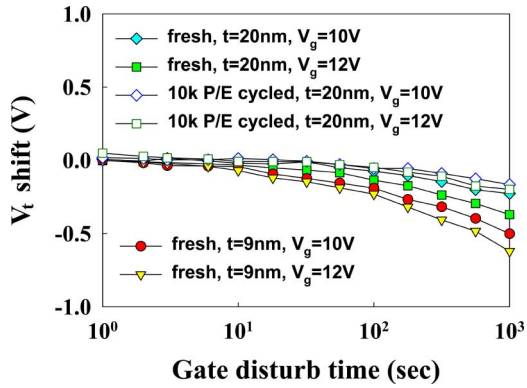

Fig. 9. Gate disturbance characteristics of the poly-Si-TFT memory devices.

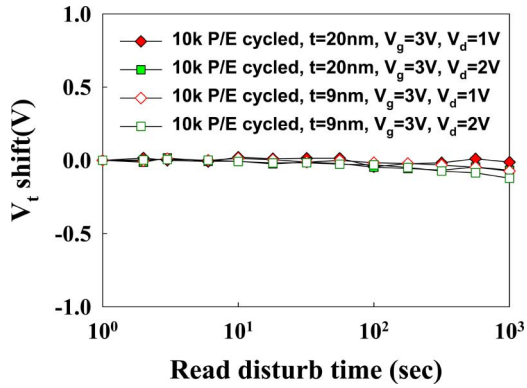

Fig. 10. Read disturbance characteristics of the poly-Si-TFT memory devices. No significant V_t shift occurred for $V_d < 1$ V, even after 1000 s at 25 °C.

respectively. We can clearly observe significant increase of $V_{\rm th}$ for both programmed and erased states after additional 10^3 P/E cycles for the memory with 20-nm tunnel oxide. This trend is believed to be intimately linked to the induced electron trapping during cycling. The origin might be due to two factors. First is the mismatch between the localized spatial distributions for the injected electrons and holes by using channel hot-electron programming and band-to-band hot-hole erasing. The uncompensated electrons will then cause the V_t to increase gradually over P/E cycling [21]. The other is the stress-induced electron traps generated in the tunnel oxide during cycling. We found that the rate of memory-window narrowing increases upon increasing P/E cycles, and the one with thick tunnel oxide had more serious memory-window closure. Thus, the tradeoff between retention and endurance characteristics shall be carefully conducted. Disturbance characteristic is a very important reliability concern for the Flash memory. Fig. 8 shows the programming drain disturbs of the poly-Si-TFT Flash memories in the programmed state. Two different drain voltages ($V_d = 10$ and 12 V, $V_g = V_s = V_{\rm sub} = 0$ V) were applied to the fresh and cycled devices. We observed that a drain disturb of $\Delta V_t \sim 0.7$ V appeared for the 10-k P/E cycled device after stressing at $V_d = 12$ V for 1000 s and, in particular, the V_t value increased as the drain disturb time increased. This phenomenon is believed to be due to the detrapping of the localized traps along the grain boundaries in the channel during drain-bias stressing [22], [23], which then make the resultant V_t shift toward positive rather than negative. Since detrapping is directly related to the extent of band bending, applying lager drain voltage corresponds to more severe band bending and induces, not surprisingly, the larger V_t shift as shown in the figure.

Fig. 9 shows the gate disturb characteristics of the poly-Si-TFT Flash memories in the erased state. Two gate voltages of 10 and 12 V were applied to the fresh and cycled memory devices with two different tunnel oxide thicknesses ($t = 9$ and 20 nm). Opposite to the drain disturbance observed in the conventional SONOS-type memory, the V_t decreased rather than increased upon the increasing gate disturb time [24]. The worst case is the fresh device with the tunnel oxide of 9 nm under 12 V stressing for 1000 s. Again, we thought these results are intimately linked to the localized traps along the grain boundaries in the channel [22], [23]. The presence of the localized traps will make turn-on voltage of the fabricated devices become higher than that of the devices with single crystalline channel, since the extra traps will have opportunity to seize some portion of induced inversion charge. With thinner tunnel oxide, more inversion charges were produced and led to more significant V_t reduction. This mechanism can also explain why the cycled memory device depicted the slightest degradation, since the generated electron traps in the tunnel oxide will result in positive V_t shift and then compensate the shift arising from the filling of defects along the grain boundaries. Therefore, to eliminate the traps along the grain boundaries in the channel is another key factor for achieving better retention of the SONOS-type Flash memory.

Fig. 10 shows the read-disturb-induced erase-state threshold voltage instability for the 10-k P/E cycled memory device. To allow 2-bit operation, the applied bitline voltage in the reverse-read scheme must be sufficiently large (> 1 V) for being able to "read-through" the trapped charge in the neighboring bit. Relatively large read bitline voltage may cause unwanted electron injection, and then, result in a significant threshold-voltage shift of the neighboring bit. For the poly-Si-TFT memory, such low drain voltage $V_d = 1$ V can be used for the 2-bit operation and is due to the depletion region induced in the undoped poly-Si body, which is considerably wide and which is able to mask the effect of the stored charge. The results clearly show that almost no read disturbance appear for the low-voltage reading operation of $V_g = 3$ V and $V_d = 1$ and 2 V in our 10-k P/E cycled memory device.

IV. Conclusion

In this paper, we have used Hf-silicate as the trapping layer for the poly-Si-TFT memory devices. By sticking to sufficiently low-thermal-budget processing, we have successfully demonstrated the feasibility of fabricating nonvolatile poly-Si-TFT Flash memories with excellent characteristics in terms of large memory windows, good speed program/erase, long retention time, and 2-bit operation. Moreover, the poly-Si grain boundary is the concerned issue about the disturbance characteristics. These poly-Si-TFT memories have good potential in realizing the embedded nonvolatile memories for the fabrication of the entire system on the panel.

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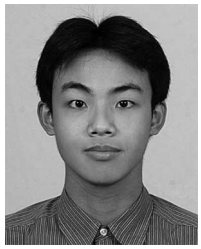

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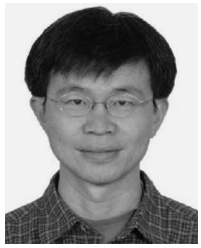

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