# Bond Pad Design With Low Capacitance in CMOS Technology for RF Applications

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***Abstract*—A new bond pad structure in CMOS technology with low capacitance for gigahertz radio frequency applications is proposed. Three kinds of inductors stacked under the pad are used in the proposed bond pad structure. Experimental results have verified that the bond pad capacitance is reduced due to the cancellation effect provided by the inductor embedded in the proposed bond pad structure. The new proposed bond pad structure is fully process-compatible to general CMOS processes without any extra process modification.**

***Index Terms*—Bond pad, capacitance, loss, radio frequency integrated circuit (RF IC).**

## I. Introduction

WITH THE advantages of high integration capability and low cost for mass production, radio frequency integrated circuits (RF ICs) operating in gigahertz frequency bands have been implemented in CMOS technology. However, the undesired parasitic capacitances at the input pads of silicon chips often limit the high-frequency performance of RF ICs. The bond pad capacitance should be minimized to mitigate the RF performance degradation. Moreover, on-chip electrostatic discharge (ESD) protection devices are also placed around the input pad, which further decrease the design budget because of the extra parasitic capacitance from the ESD protection devices [1]–[4]. The parasitic capacitance resulted from the bond pad metal, and the overlapped substrate was not reduced with the progress of CMOS technology. In some CMOS integrated RF front ends, the bond pad capacitance can be incorporated as a part of the matching network. Recently, several techniques were reported to reduce the bond pad capacitance [5]–[7]. A bond-pad structure realized with special layout patterns, which have smaller metal area and additional diffusion layers, had been demonstrated with smaller bond pad capacitance [5]. Another bond pad using depletion-insulation structure to improve crosstalk isolation and $Q$-factor had been presented [6]. Besides, a bond pad structure realized with semi-insulating porous silicon had also been reported to reduce the bond pad capacitance [7].

In this letter, a new bond pad structure with embedded inductor is proposed to reduce the bond pad capacitance. The proposed bond pad structure possesses several features. First, it is compatible to standard CMOS process without extra process modification. Second, the proposed bond pad has the same dimensions as that of the reference bond pad to maintain good bonding reliability. Third, the proposed bond pad has low parasitic capacitance, which is suitable for high-frequency applications.

Manuscript received August 1, 2006; revised October 19, 2006. This work was supported in part by the National Science Council (NSC), Taiwan, R.O.C., under Contract NSC 95-2221-E-009-290, and in part by the Faraday Technology Corporation, Taiwan, R.O.C. The review of this letter was arranged by Editor S. Kawamura.

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Digital Object Identifier 10.1109/LED.2006.887631

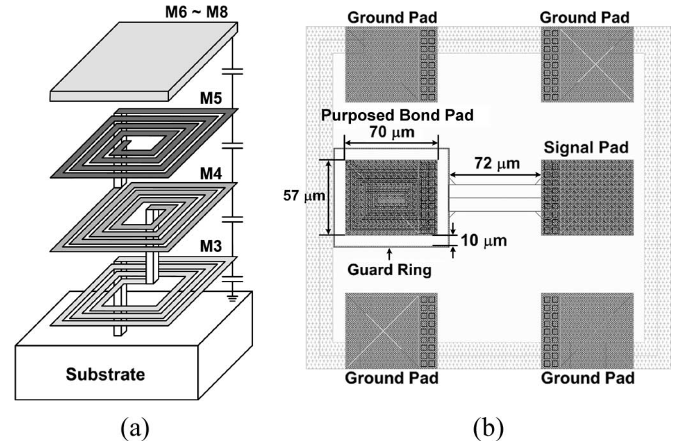


Fig. 1. (a) Proposed bond pad structure with an embedded three-layer stacked inductor in a 0.13-$\mu$m 1P8M CMOS process. (b) Layout top view of the test pattern to measure the bond pad capacitance.

## II. Proposed Bond Pad Structures

A 0.13-$\mu$m 1P8M CMOS process is used in this letter, and the typical bond pad provided by foundry is fully implemented with eight metal layers (from metal 1 to metal 8). However, the parasitic capacitance of the bottom metal layer (metal 1) and the overlapped substrate is too large for RF applications. In order to reduce the parasitic capacitance, the lower metal layers are removed in the bond pads. However, using only the top metal layer to implement the bond pads has some concerns on bonding reliability. To compromise the dilemma between parasitic capacitance and bonding reliability, the reference bond pad used in this letter is realized with only top three metal layers, which are metals 8, 7, and 6 in a 0.13-$\mu$m CMOS process.

The proposed bond pad structure with an embedded inductor is illustrated in Fig. 1(a), where a stacked inductor [8] implemented with three metal layers (metals 5, 4, and 3) is embedded under the reference bond pad. Since the inductor is implemented within the region of the bond pad, the proposed bond pad occupies the same area as the reference one. The bond pads with three kinds of inductors, which are one-layer inductor (implemented with metal 5), three-layer stacked inductor

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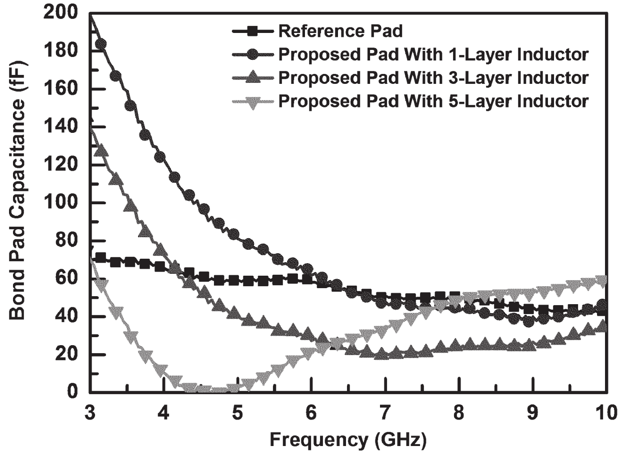


Fig. 2. Extracted bond pad capacitances among the fabricated bond pads under different frequencies.

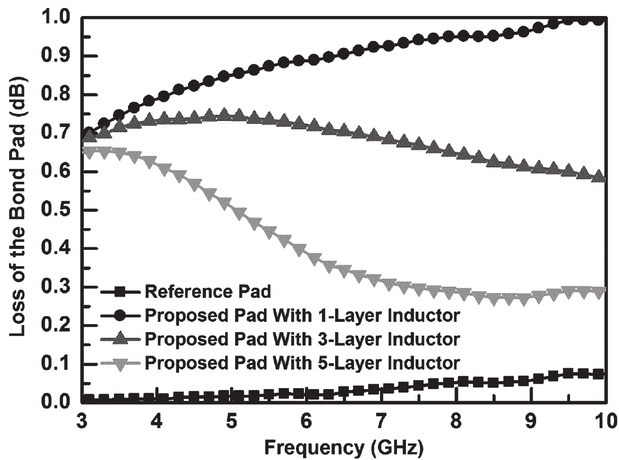


Fig. 3. Measured losses among the fabricated bond pads under different frequencies.

(implemented with metals 5, 4, and 3), and five-layer stacked inductor (implemented with metals 5, 4, 3, 2, and 1), have been designed in the experimental test chip for comparison. The inductors are drawn with the track width of 4 $\mu$m, track spacing of 1 $\mu$m, and five turns. The inductor designed in such architecture is used to increase the inductance under the prespecified region to cancel the bond pad capacitance.

Fig. 1(b) shows the layout top view of the test patterns used to measure the bond pad capacitance. Ground–signal–ground (G–S–G) pads are adopted to facilitate on-wafer measurement. The proposed bond pad occupies the same area $(70 \times 57\ \mu\text{m})$ as that of the reference bond pad. A guard ring is implemented to encircle the proposed bond pad. With the guard ring connected to the substrate, the parasitic capacitance between the bond pad and the substrate can be characterized.

## III. Experimental Results and Discussion

The proposed bond pads with one-, three-, and five-layer stacked inductors as well as the reference bond pad have been fabricated in the same silicon chip in a 0.13-$\mu$m 1P8M CMOS process. The two-port $S$-parameters of the fabricated bond pads

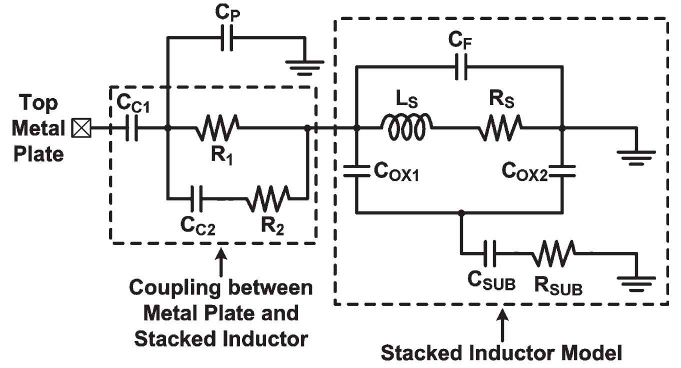


Fig. 4. Circuit model of the proposed bond pad.

were characterized by on-wafer measurement with Cascade Air Coplanar G–S–G microwave probes and the Agilent 8510C network analyzer. The measured frequency range was from 3 to 10 GHz.

The $Z$-parameters can be obtained from the conversions between two-port $S$-parameters and $Z$-parameters [9]. Then, the bond pad capacitance $(C_{\text{pad}})$ was extracted as $C_{\text{pad}} = -1/(\omega \text{Im}(\text{Z}_{11}))$, where $\text{Z}_{11}$ is the impedance seen from port 1 with port 2 open. Fig. 2 shows the extracted bond pad capacitances among the fabricated bond pads under different frequencies. As shown in Fig. 2, the reduction on the bond pad capacitance is more significant when a stacked inductor realized with more metal layers is embedded under the bond pad. With a five-layer stacked inductor in the proposed bond pad, the bond pad capacitance can be even reduced to almost 0 fF at a specific frequency band (4.3 $\sim$ 4.8 GHz). The bond pad capacitance is reduced due to the positive reactance contributed from the embedded inductor. For example, the bond pad capacitance of the proposed structure with one-, three-, and five-layer stacked inductors can be reduced 2.9%, 58.9%, and 49.3%, respectively, from the original value (the reference pad) at 6.5 GHz. With more sophisticated design on the embedded inductor, the frequency band in which the bond pad capacitance is reduced can be further extended.

The measured losses among the fabricated bond pads are shown in Fig. 3. In the loss measurement, port 1 and port 2 of the network analyzer were both connected to the top metal plate of the bond pad. The loss was obtained from the measured $S_{21}$ with the relation of $\text{Loss (dB)} = -(S_{21}(\text{dB}))$. Since the impedance of the five-layer stacked inductor is much higher than that of the one-layer inductor, the proposed pad with five-layer stacked inductor has the least loss, while the proposed pad with one-layer inductor has the most loss among the three kinds of proposed pads. From 3 to 10 GHz, the proposed bond pad with five-layer stacked inductor has a loss less than 0.65 dB. Because the inductor was connected to the substrate in the proposed bond pad structure, the proposed bond pad has more loss as compared with the reference bond pad. However, since all I/O pads need to be accompanied with ESD protection circuits, the loss of the proposed bond pad will not be the critical part at the input or output nodes because of the larger signal loss caused by the on-chip ESD protection devices. The circuit model of the proposed bond pad is shown in Fig. 4. $C_P$ represents the parasitic capacitance between the metal

plates of the bond pad and the substrate. $C_{C1}$, $C_{C2}$, $R_1$, and $R_2$ represent the coupling between the metal plates and the stacked inductor. $C_F$ represents the parasitic capacitance between the metal layers in the stacked inductor. $L_S$ and $R_S$ are the inductance and series resistance of the stacked inductor, respectively. $C_{OX1}$ and $C_{OX2}$ represent the capacitance between the stacked inductor and the substrate. $C_{\mathrm{SUB}}$ and $R_{\mathrm{SUB}}$ represent the parasitic effects of the substrate.

At 5 GHz, the capacitance of the proposed bond pad with five-layer stacked inductor is only 3.15 fF, which is quite small. Therefore, the proposed bond pad is suitable for gigahertz applications. The frequency at which the capacitance of the proposed bond pad is minimum can be adjusted by changing the dimensions of the stacked inductor and the metal plates of the bond pad. To mitigate the impact of the bond pad loss, the proposed bond pad can be codesigned with on-chip ESD protection devices. For example, the impedance isolation technique had been used to optimize the RF characteristics at the input and output nodes, which have the bond pad and ESD protection devices [10].

## IV. Conclusion

By inserting a stacked inductor under a bond pad, the proposed bond pad performs low parasitic capacitance. The experimental results have proven that the embedded inductor can be used to reduce the bond pad capacitance. The proposed low-capacitance bond pad structure, achieved by layout modification, is fully process-compatible to general CMOS processes for RF applications.

## Acknowledgment

The authors would like to thank W.-C. Wang for his valuable technical discussions. The authors would also like to thank the reviewers for their valuable suggestions to improve this letter.

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