High-Performance $SrTiO_3$ MIM Capacitors for Analog Applications

K. C. Chiang, Ching-Chien Huang, G. L. Chen, Wen Jauh Chen, H. L. Kao, Yung-Hsien Wu, Albert Chin, *Senior Member, IEEE*, and Sean P. McAlister, *Senior Member, IEEE*

***Abstract*—TaN/$SrTiO_3$/TaN capacitors with a capacitance density of 28–35 fF/μm^2 have been developed by using a high-κ ($\kappa = 147-169$) $SrTiO_3$ dielectric containing nanometer-sized microcrystals (3–10 nm). A small capacitance effective thickness was achieved by reducing the interfacial TaON using N^+ treatment on the lower TaN electrode during post-deposition annealing. The small (92 ppm/V^2) voltage coefficient of the capacitance and the 3×10^{-8} A/cm^2 leakage current at 2 V exceed the International Technology Roadmap for Semiconductors' requirements for analog capacitors at year 2018.**

***Index Terms*—Capacitor, International Technology Roadmap for Semiconductors (ITRS), metal–insulator–metal (MIM), $SrTiO_3$ (STO).**

I. Introduction

According to the International Technology Roadmap for Semiconductors (ITRS) [1], the capacitance density of future metal–insulator–metal (MIM) capacitors has to increase to help reduce chip sizes and the cost of ICs. Besides the high capacitance density ($\varepsilon_0\kappa/t_d$) and the limited thermal budget necessary for back-end integration, a low leakage current and a small voltage dependence of the capacitance ($\Delta C/C$) are also necessary for analog functions. To meet these requirements, high dielectric constant (κ) materials [2]–[19] provide the only solution, since decreasing the dielectric thickness (t_d) to increase the capacitance density degrades both the leakage current and the $\Delta C/C$ performance. Therefore, the high-κ dielectrics used in MIM capacitors have evolved from SiON ($\kappa \sim 4-7$) [3]–[5], Al_2O_3 ($\kappa = 10$) [13], HfO_2 ($\kappa \sim 22$) [7]–[11], Ta_2O_5 ($\kappa \sim 25$) [12], [15] to Nb_2O_5 ($\kappa \sim 40$) [16] or TaTiO ($\kappa \sim 45$) [17]–[19].

Manuscript received March 8, 2006; revised June 5, 2006. This work was supported in part by the National Science Council of Taiwan, R.O.C under Grant 94-2215-E-009-062. The review of this paper was arranged by Editor V. R. Rao.

K. C. Chiang, C.-C. Huang, G. L. Chen, and A. Chin are with the Nanometer Center, Department of Electronics Engineering, National Chiao-Tung University, Hsinchu 300, Taiwan, R.O.C. (e-mail: achin@cc.nctu.edu.tw).

W. J. Chen is with the Graduate Institute of Materials Engineering, National Pingtung University of Science and Technology, Pingtung 91201, Taiwan, R.O.C.

H. L. Kao is with the Department of Electronic Engineering, Chang Gung University, Tao-Yuan 333, Taiwan, R.O.C.

Y.-H. Wu is with the Department of Engineering and System Science, National Tsing-Hua University, Hsinchu 30013, Taiwan, R.O.C.

S. P. McAlister is with the National Research Council of Canada, Ottawa, ON K1A 0R6, Canada.

Digital Object Identifier 10.1109/TED.2006.881013

$SrTiO_3$ (STO) is a potential candidate to increase the κ value beyond 45. It has the well-known perovskite-type structure and has a para-electric phase above 105K and a high κ value of $\sim$ 300 at room temperature. It is an attractive candidate for DRAM [20]–[24] due to the high charge storage capacity and para-electricity (no fatigue or aging problems). To achieve the high κ value, the STO requires heat treatment at 450 °C–500 °C under an oxygen ambient for crystallization [20]–[23]. Therefore, it also requires a Pt or RuO_2 lower electrode [21] to withstand the high temperature oxidation, but the high cost and availability of noble metals pose concerns for mass production.

To address this issue, we have fabricated STO MIM capacitors on a conventional TaN electrode, where a NH_3 plasma treatment on the lower TaN has been used to improve the electrode stability and capacitance density degradation by forming interfacial TaON during the postdeposition anneal (PDA). We obtained a 28-fF/μm^2 capacitance density, a small quadratic voltage coefficient of capacitance (α) of 92 ppm/V^2, and low 3×10^{-8} A/cm^2 leakage current at 2 V. This performance meets the specifications for analog capacitors as set out by the ITRS for the year 2018.

II. Experimental Procedure

The MIM capacitors were fabricated on a 4-μm SiO_2 that had been deposited on a Si wafer. The lower capacitor electrodes were formed by depositing 0.05-μm TaN on a 1-μm Ta layer, where the thick Ta was chosen to reduce the parasitic resistance of the electrode and the TaN served as a barrier layer for the STO. After patterning the lower electrode, the TaN was treated by NH_3 plasma nitridation at 100 W to improve the lower interface. The 43- and 55-nm STO (Sr/Ti $= 1.1$) dielectric layers were then deposited using RF magnetron sputtering. This was done using a ceramic STO target in a 4:1 Ar/O_2 gas mixture at a total pressure of 10 mtorr. This was followed by 400 °C–450 °C furnace annealing for 30 min to $\sim$ 1 h under an oxygen ambient—for crystallization and quality improvement. Finally, TaN/Al was deposited and patterned to form the top capacitor electrode. Cross-sectional transmission electron microscopy (TEM) and secondary ion mass spectroscopy (SIMS) were used to study the metal interface and dielectric properties. The fabricated MIM capacitors were characterized by J–V and capacitance–voltage (C–V) measurements using an HP4156C curve tracer and HP4284A precision LCR meter, respectively.

0018-9383/$20.00 © 2006 IEEE

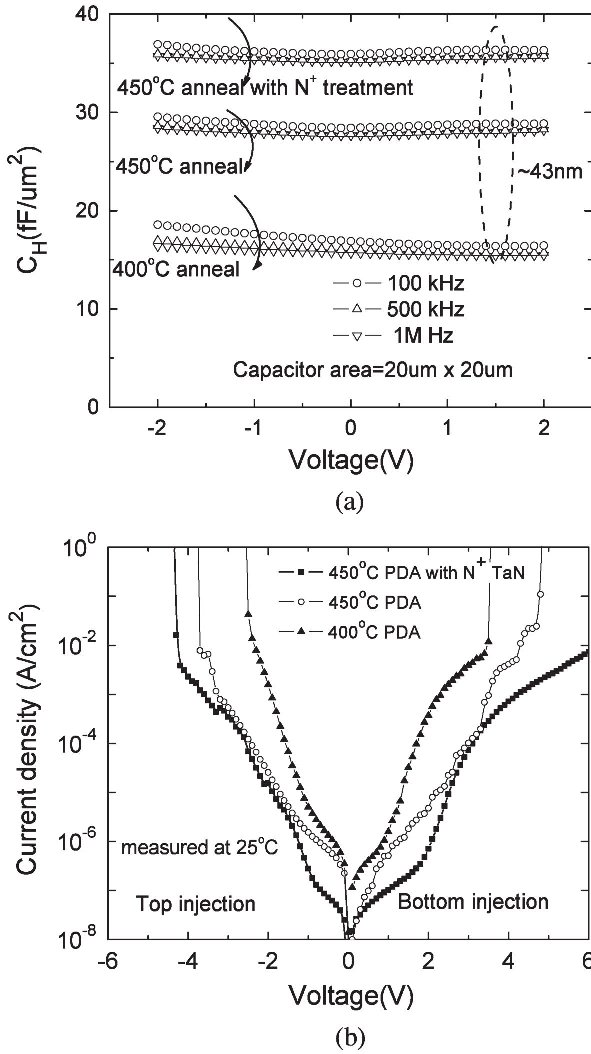


Fig. 1. (a) C–V and (b) J–V characteristics of TaN/STO/TaN MIM capacitors processed under various conditions. The 400 °C PDA yields a capacitance density of 17 fF/μm^2, which increases to 28 fF/μm^2 for a 450 °C PDA and is better with the N^+ treatment (35 fF/μm^2).

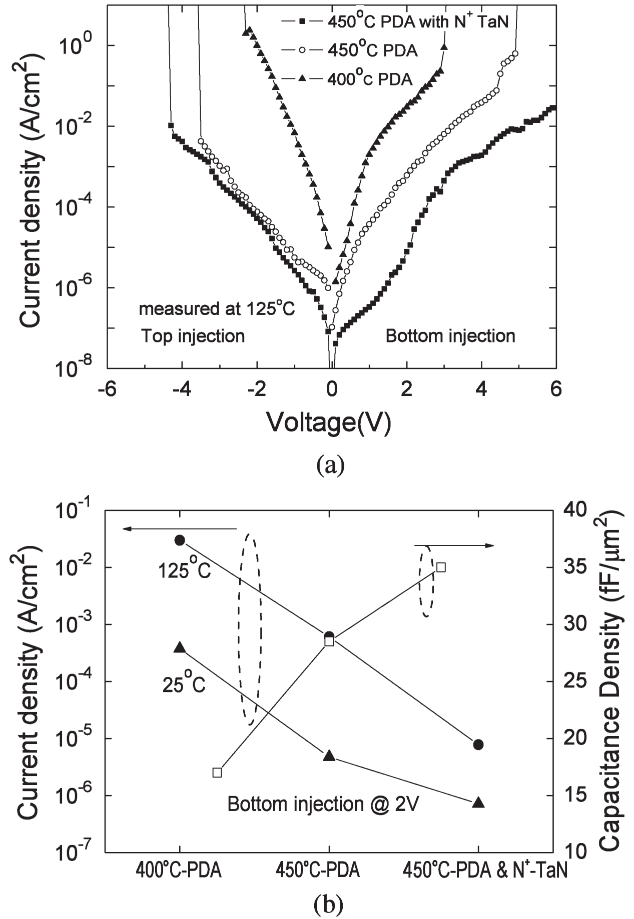


Fig. 2. (a) J–V characteristics for the devices in Fig. 1 measured at 125 °C. (b) Comparison of the C–V and J–V characteristics of TaN/STO/TaN MIM capacitors.

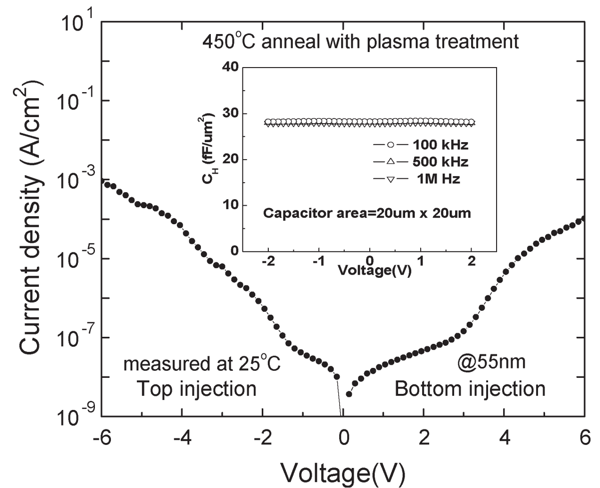


Fig. 3. J–V and C–V (insert) characteristics of an STO MIM capacitor using optimum process conditions.

III. Results and Discussion

A. Electrical J–V and C–V Characteristics

Fig. 1(a) and (b) shows the C–V and J–V characteristics of TaN/STO/TaN capacitors, respectively, which were processed differently. The capacitance density increased from 17 to 28 fF/μm^2 with increasing O_2 PDA temperature and the use of nitrogen plasma (N^+) treatment on the TaN. At the same time, better frequency dispersion, lower leakage current, and higher breakdown voltage (BV) of the MIM devices were obtained. Application of the N^+ treatment on the lower TaN improved the capacitor density from 28 to 35 fF/μm^2 and decreased the leakage current by nearly an order of magnitude at < 2 V.

Examination of the device performance at 125 °C [Fig. 2(a)] shows that N^+ treatment still improves the leakage current at positive bias. The leakage current and the capacitance density under various process conditions are summarized in Fig. 2(b). The higher O_2 PDA temperature and N^+ treatment generally improve the leakage current and capacitance density of TaN/STO/TaN capacitors.

To address the ITRS requirements for low leakage current for analog capacitors (at year 2018), we also fabricated high-performance MIM capacitors of other thicknesses. This was done in an attempt to achieve the ITRS goals of 10 fF/μm^2 density, $J/(C \cdot V) < 7$ fA/(pF $\cdot$ V), and $\alpha < 100$ ppm/V^2 [1]. Fig. 3 shows the J–V characteristics of a 28-fF/μm^2 density

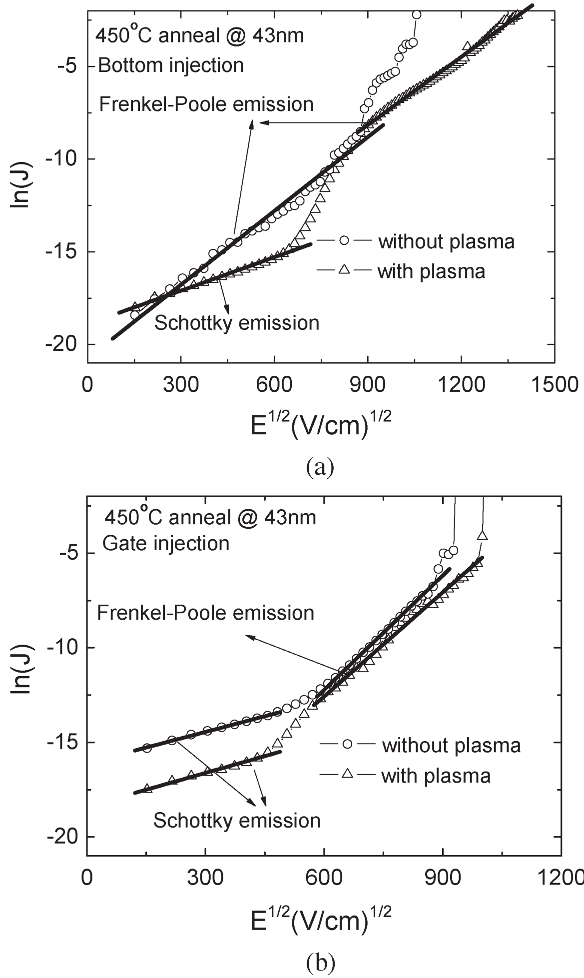


Fig. 4. Plot of $\ln(J)$ versus $E^{1/2}$ under electron injection from the (a) bottom and (b) top electrode.

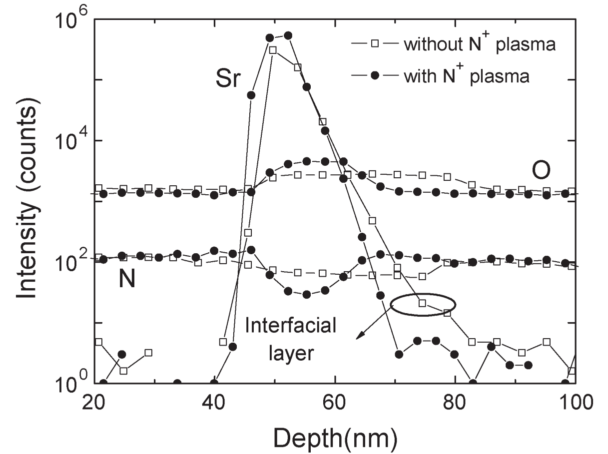


Fig. 5. SIMS profile of STO/TaN with or without N^+ treatment on the lower TaN.

capacitor (inserted figure) with a 55-nm thickness fabricated under the optimal conditions of a 450 °C PDA and N^+-treated TaN. A low leakage current of 3×10^{-8} A/cm^2 at 2 V was measured, which gives a $J/(C \cdot V)$ of 5.4 fA/(pF · V). This meets the ITRS leakage current requirement at 2018 along with 2.8 times better capacitance density. The leakage current under reverse bias (top electron injection) is markedly higher than that under positive bias (injection from the lower electrode). This may be due to the surface roughness originating from the crystallized STO. However, crystallization is needed for the STO to display a high κ value.

B. Current Conduction Mechanism

To investigate the large leakage current difference for different voltage polarities, we have plotted $\ln(J)$ versus $E^{1/2}$ in Fig. 4(a) and (b) for electrons injected from the bottom and top electrodes, respectively. A linear $\ln(J)–E^{1/2}$ relation is shown, although a strong process dependence and a different slope are observed. The different slopes in the $\ln(J)–E^{1/2}$ plot suggest different current conduction mechanisms. It is known that both Schottky emission (SE) and Frenkel–Poole (FP) conduction can give such a linear $\ln(J)–E^{1/2}$ relation with different slopes (γ) as indicated by [22]

$$J \propto \exp\left(\frac{\gamma E^{1/2} - V_b}{kT}\right) \tag{1}$$

$$\gamma = \left(\frac{e^3}{\eta\pi\varepsilon_0 K_\infty}\right)^{1/2} \tag{2}$$

where k is Boltzmann's constant, T is the temperature in kelvin, e is the electron charge, ε_0 is the permittivity in vacuum, K_∞ is the high-frequency dielectric constant $(= n^2$, where n is the refractive index), and η is a constant with its value equal to 1 or 4 for FP or SE, respectively. The different slopes γ for the SE and FP cases arise from the different energy barriers V_b, corresponding to the work function of the metal-electrode/dielectric in the SE case or the trap energy level in the dielectric for the FP case. The fits to the experimental data give slopes of 1.58×10^{-5} or 3.16×10^{-5} eV $(\mathrm{m/V})^{1/2}$ for the SE or FP mechanisms, respectively, by using $n = 2.4$ for STO [22], [26] in the above equations.

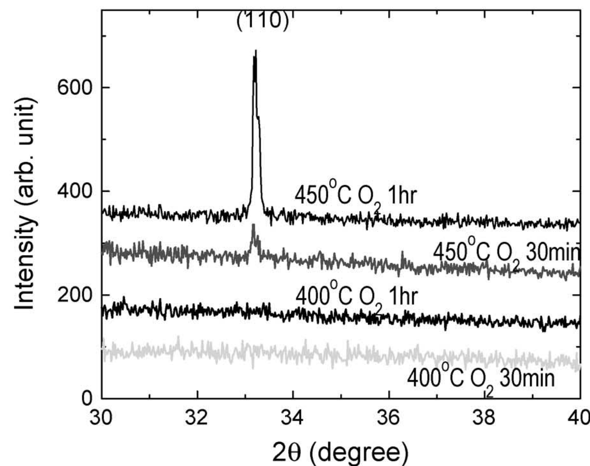
Following the good agreement between measured and calculated data [using (1)], we investigated the dependence of leakage current on process conditions and voltage polarity. For electrons injected from the top TaN electrode, the current conduction mechanism changes from SE at low electric fields to FP at higher fields. The FP-dominated high-field conduction arises because the trapped electrons can gain energy and be emitted from trapped states and contribute to the leakage current. The smaller SE current for the device with lower electrode N^+ treatment is related to the smoother STO/TaN surface, as determined by atomic force microscopy (AFM), where the STO rms roughness improved from 11.2 to 5.9 nm. For the lower electrode injection case, the current conduction mechanism depends on whether the TaN electrode had the N^+ treatment. For the N^+-treated case, the current conduction mechanism is the same as for top electrode injection, i.e., SE at low field, which changes to FP at high field. However, for the lower TaN electrode without N^+ treatment, the FP mechanism applies

at both low and high fields. These results indicate a higher trap density or deeper trap energies in STO or the STO/TaN interfacial layer when the lower TaN electrode does not have the N^+ treatment.

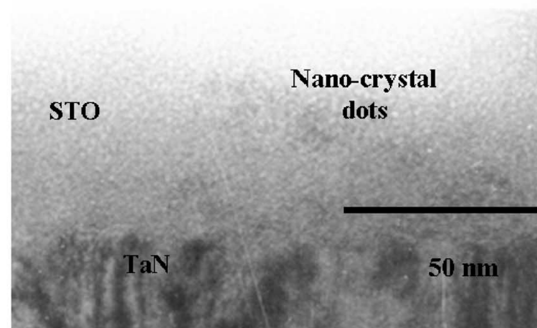
C. Material Characterization

We measured the SIMS depth profile of the devices to study the origin of the improved leakage current for the N^+-treated case. As shown in Fig. 5, even under the existing background level of SIMS system, a higher oxygen concentration can be observed in the lower TaN layer without N^+ treatment. The interfacial TaON was formed during STO oxidation annealing but degraded the capacitance effective thickness (CET), capacitance density, and overall κ value. In sharp contrast, the device with N^+ treatment on the lower TaN shows less inter-diffusion and a better interface. In addition, less nitrogen was found in the STO for the treated sample. It is important to note that such an interfacial layer is also responsible to the higher leakage current at low field, as discussed above, and may be due to the higher trap density from the oxygen deficiency as shown by SIMS. This would lead to trap-assisted FP conduction.

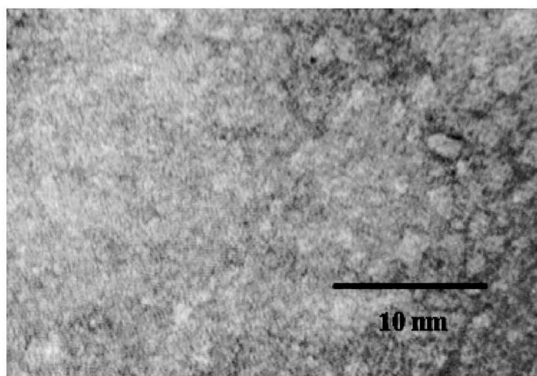
The fabricated STO/TaN was also examined by X-ray diffraction (XRD) and TEM. As shown in the XRD spectra of Fig. 6(a), the crystalline phase of STO is dependent on the PDA temperature and time. STO crystallization starts after 450 °C PDA, and the degree of crystallization (XRD intensity) increases with increasing PDA time. Because the κ value of perovskite-type STO is known to increase with increasing degree of crystallization, this result explains the larger capacitance density in Fig. 1(a) at higher PDA temperature. The crystallized STO is confirmed by the cross-sectional TEM of Fig. 6(b) and its enlargement in Fig. 6(c). At 43-nm STO thickness, a high κ value of 169 and improved lower STO/TaN interface, compared with previous work [17], were found for the 35-fF/μm^2 density device (0.99 nm CET). The microcrystals, consistent with the XRD measurements, had a grain size of 3–10 nm as indicated in the TEM image. Such micrograined STO is essential in producing thin consistent STO layers for devices [25].



(a)



(b)



(c)

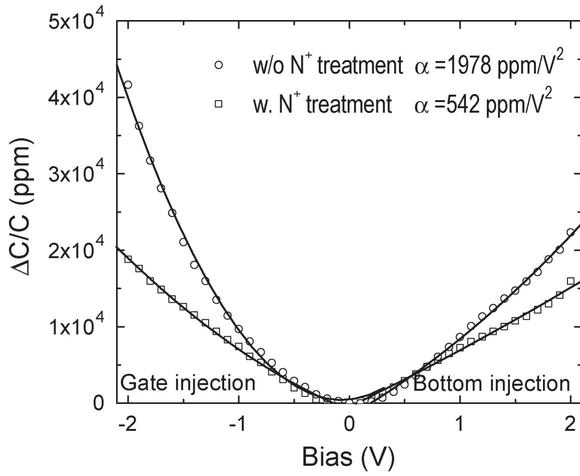
Fig. 6. (a) XRD spectra of STO after a 400 °C–450 °C O_2 PDA. Crystallization of STO was found at 450 °C O_2 PDA. (b) Cross-sectional TEM of STO/N^+-treated TaN with (c) an enlarged STO image.

D. $\Delta C/C$, α, and Temperature Coefficient of the Capacitance (TCC)

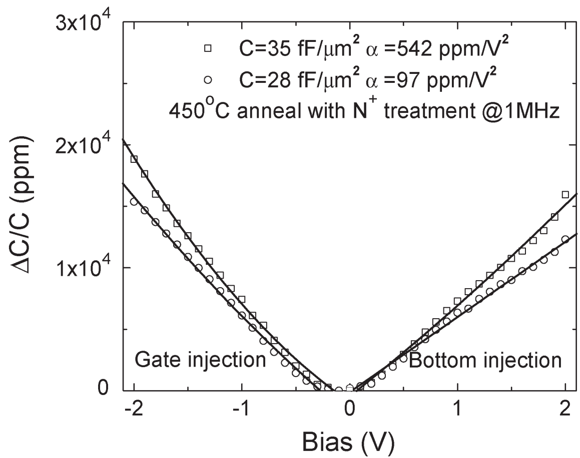
α is an important parameter of MIM capacitors for analog applications. The undesirable voltage dependence can be obtained by fitting the measured C–V characteristics with a second-order polynomial equation

$$\Delta C(V) = C_0(\alpha V^2 + \beta V) \qquad (3)$$

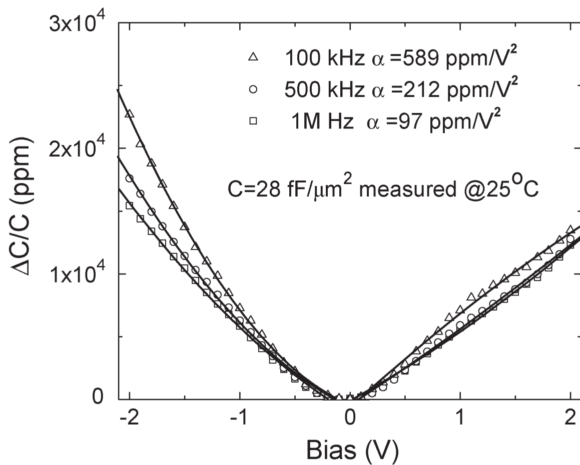
where C_0 is the capacitance at 0 V, and α and β represent the quadratic and linear voltage coefficients of capacitance, respectively. Since the effect of the linear β term can be compensated by circuit design using a differential method [27], the α term is the main factor in the voltage dependence. Fig. 7(a) and (b) shows the $\Delta C/C$–V dependence on N^+ treatment and capacitance density, respectively. Good fits to (3) were obtained in all the cases and yielded α. The N^+ treatment can dramatically reduce α from 1978 to 542 ppm/V^2 at 1 MHz. This significantly better α is consistent with the improved leakage current and interface properties shown above. An even better α was measured as the STO thickness was increased, although a trade-off of the capacitance density is needed. Under the best conditions—450 °C PDA and N^+-treated lower TaN—a small α of 92 ppm/V^2 was obtained in a 28-fF/μm^2 capacitor. This meets the ITRS specifications for year 2018 with nearly



(a)

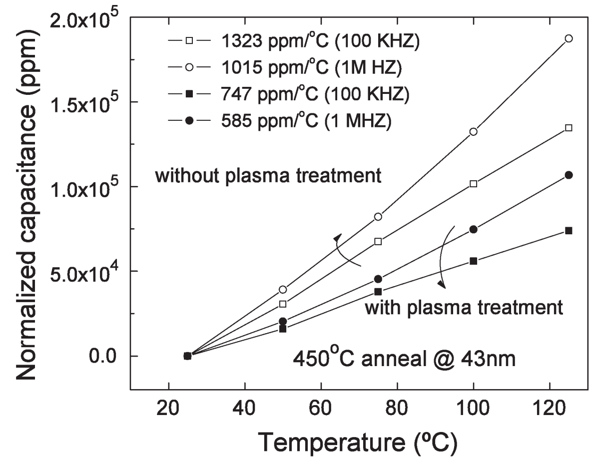


(b)

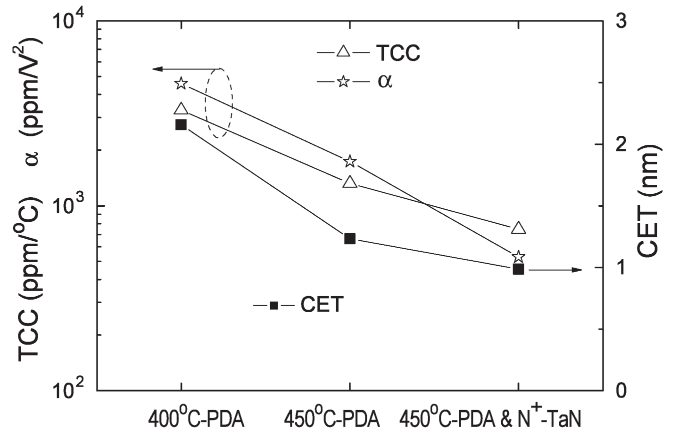


(c)

Fig. 7. $\Delta C/C$–V characteristics for STO MIM capacitors and the dependence on (a) plasma nitridation on the lower TaN and (b) different capacitance densities of 28–49 fF/μm^2. (c) Frequency dispersion of the 28-fF/μm^2 density capacitor.



(a)



(b)

Fig. 8. (a) Temperature-dependent normalized capacitance for MIM capacitors with or without plasma nitridation of the lower TaN. (b) α, TCC, and CET as a function of various treated MIM capacitors.

three times better capacitance density. The frequency dispersion of the capacitance can have a significant impact in precision analog circuit applications [28]. As shown in Fig. 7(c), significantly better frequency dispersion of the capacitance was measured for positive bias than negative bias. This is consistent with the lower leakage current in the lower electrode injection case and may be due to the better STO/TaN interface, as discussed above.

Since modern ICs usually operate at elevated temperature, TCC is important. Fig. 8(a) shows the temperature dependence of the normalized capacitance for STO MIM capacitors with and without plasma treatment. TCC increases with increasing temperature but decreases with increasing frequency [7]. It is also strongly dependent on processing conditions. As summarized in Fig. 8(b), higher PDA temperatures and N^+ treatment improved the TCC characteristics. This is similar to the α improvement, which suggests that the primary mechanism determining the TCC is also trap related.

E. Performance Comparison

Fig. 9 shows the dependence of α as a function of CET or the inverse capacitance density $(1/C)$. An exponential decrease of α with increasing CET or $1/C$ was observed for the Ta_2O_5 [12], HfO_2 [10], Tb-doped HfO_2 [8], TiTaO [18], and STO MIM capacitors. This is due to the trap-related leakage current

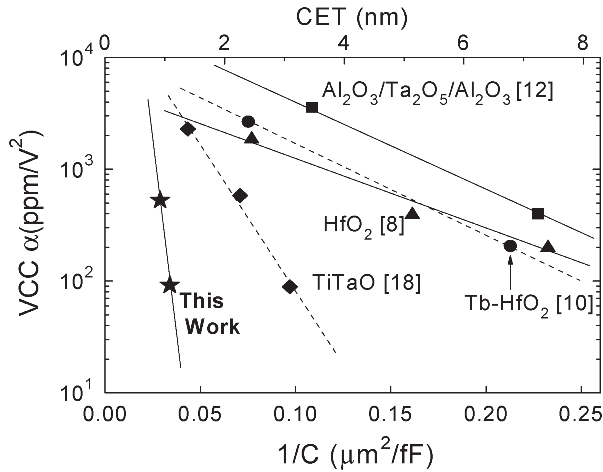


Fig. 9. $\Delta C/C{-}1/C$ plot of TaN/STO/TaN and various high-κ MIM capacitors. The exponential decrease with increasing $1/C$ is important for designing capacitors for different applications.

TABLE I
COMPARISON OF VARIOUS HIGH-κ CAPACITORS. TaN/STO/TaN CAPACITOR SHOWS THE BEST PERFORMANCE, EXCEEDING THE REQUIREMENTS OF THE ITRS FOR 2018

	ITRS @ 2018	Ta_2O_5 [12]	Tb-HfO_2 [8]	HfO_2 [10]	TiTaO [17]	This work
C Density (fF/μm^2)	10	9.2	13.3	12.8	10.3	28
J (A/cm^2)	-	2×10^{-8} (1.5V)	1×10^{-7} (2V)	8×10^{-9} (2V)	1.2×10^{-8} (2V)	3×10^{-8} (2V)
J/(C•V) (fA/[pF•V])	<7	14.5 @1.5V	38 @2V	2.9 @2V	5.8 @2V	5.4 @2V
α (ppm/V^2)	α<100	3580	2667	1990	89	92

that also has an exponential dependence on CET [7]. For the same CET or capacitance density value, the STO device has the lowest α. This is due to the high κ value of 147–169, which exceeds the $\kappa \sim 22{-}45$ values for HfO_2, Ta_2O_5, and TiTaO. The $\alpha{-}1/C$ dependence is important in choosing the required C density and also in meeting the analog specifications of a low α.

The important device parameters for the analog capacitors are summarized in Table I. Among the various high-κ capacitors, the TaN/STO/TaN capacitor shows the best performance, meeting the ITRS requirements for 2018 and with 2.8 times better capacitance density.

IV. CONCLUSION

Using micro-crystallized high-κ $SrTiO_3$ and a N^+ treatment on the lower TaN, TaN/STO/TaN capacitors show good device integrity along with 28-fF/μm^2 capacitance density, an α of 92 ppm/V^2, and leakage current of 3×10^{-8} A/cm^2 at 2 V. These data exceed the ITRS specifications for analog capacitors for 2018 and have the advantage of simple dielectric processing without requiring noble metal electrodes.

ACKNOWLEDGMENT

K. C. Chiang, C.-C. Huang, G. L. Chen, H. L. Kao, and A. Chin would like to thank Prof. R. N. Kwo and M. H. Hong of the National Tsing-Hua University.

REFERENCES

[1] *International Technology Roadmap for Semiconductors (ITRS)*, 2005. [Online]. Available: www.itrs.net

[2] C.-M. Hung, Y.-C. Ho, I.-C. Wu, and K. O, "High-Q capacitors implemented in a CMOS process for low-power wireless applications," in *Proc. IEEE MTT-S Int. Microw. Symp. Dig.*, 1998, pp. 505–511.

[3] J. A. Babcock, S. G. Balster, A. Pinto, C. Dirnecker, P. Steinmann, R. Jumpertz, and B. El-Kareh, "Analog characteristics of metal–insulator–metal capacitors using PECVD nitride dielectrics," *IEEE Electron Device Lett.*, vol. 22, no. 5, pp. 230–232, May 2001.

[4] C. H. Ng, K. W. Chew, and S. F. Chu, "Characterization and comparison of PECVD silicon nitride and silicon oxynitride dielectric for MIM capacitors," *IEEE Electron Device Lett.*, vol. 24, no. 8, pp. 506–508, Aug. 2003.

[5] L. Y. Tu, H. L. Lin, L. L. Chao, D. Wu, C. S. Tsai, C. Wang, C. F. Huang, C. H. Lin, and J. Sun, "Characterization and comparison of high-κ metal–insulator–metal (MIM) capacitors in 0.13 μm Cu BEOL for mixed-mode and RF applications," in *VLSI Symp. Tech. Dig.*, 2003, pp. 79–80.

[6] Z. Chen, L. Guo, M. Yu, and Y. Zhang, "A study of MIMIM on-chip capacitor using Cu/SiO_2 interconnect technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 12, no. 7, pp. 246–248, Jul. 2002.

[7] C. Zhu, H. Hu, X. Yu, S. J. Kim, A. Chin, M. F. Li, B. J. Cho, and D. L. Kwong, "Voltage and temperature dependence of capacitance of high-k HfO_2 MIM capacitors: A unified understanding and prediction," in *IEDM Tech. Dig.*, 2003, pp. 879–882.

[8] S. J. Kim, B. J. Cho, M.-F. Li, C. Zhu, A. Chin, and D. L. Kwong, "HfO_2 and lanthanide-doped HfO_2 MIM capacitors for RF/mixed IC applications," in *VLSI Symp. Tech. Dig.*, 2003, pp. 77–78.

[9] S. J. Kim, B. J. Cho, S. J. Ding, M.-F. Li, M. B. Yu, C. Zhu, A. Chin, and D. L. Kwong, "Engineering of voltage nonlinearity in high-κ MIM capacitor for analog/mixed-signal ICs," in *VLSI Symp. Tech. Dig.*, 2004, pp. 218–219.

[10] H. Hu, S. J. Ding, H. F. Lim, C. Zhu, M. F. Li, S. J. Kim, X. F. Yu, J. H. Chen, Y. F. Yong, B. J. Cho, D. S. H. Chan, S. C. Rustagi, M. B. Yu, C. H. Tung, A. Du, D. My, P. D. Fu, A. Chin, and D. L. Kwong, "High performance $HfO_2{-}Al_2O_3$ laminate MIM capacitors by ALD for RF and mixed signal IC applications," in *IEDM Tech. Dig.*, 2003, pp. 879–882.

[11] S. J. Kim, B. J. Cho, M.-F. Li, C. Zhu, A. Chin, and D. L. Kwong, "Lanthanide (Tb)-doped HfO_2 for high density MIM capacitors," *IEEE Electron Device Lett.*, vol. 24, no. 7, pp. 442–444, Jul. 2003.

[12] T. Ishikawa, D. Kodama, Y. Matsui, M. Hiratani, T. Furusawa, and D. Hisamoto, "High-capacitance $Cu/Ta_2O_5/Cu$ MIM structure for SoC applications featuring a single-mask add-on process," in *IEDM Tech. Dig.*, 2002, pp. 940–942.

[13] S. B. Chen, J. H. Lai, K. T. Chan, A. Chin, J. C. Hsieh, and J. Liu, "Frequency-dependent capacitance reduction in high-κ $AlTiO_x$ and Al_2O_3 gate dielectrics from IF to RF frequency range," *IEEE Electron Device Lett.*, vol. 23, no. 4, pp. 203–205, Apr. 2002.

[14] C. H. Huang, M. Y. Yang, A. Chin, C. X. Zhu, M. F. Li, and D. L. Kwong, "High density RF MIM capacitors using High-κ $AlTaO_x$ dielectrics," in *Proc. IEEE MTT-S Int. Microw. Symp. Dig.*, 2003, vol. 1, pp. 507–510.

[15] M. Y. Yang, C. H. Huang, A. Chin, C. Zhu, B. J. Cho, M. F. Li, and D. L. Kwong, "Very high density RF MIM capacitors (17 fF/μm^2) using high-κ Al_2O_3 doped Ta_2O_5 dielectrics," *IEEE Microw. Wireless Comp. Lett.*, vol. 13, no. 10, pp. 431–433, Oct. 2003.

[16] S. J. Kim, B. J. Cho, M. B. Yu, M.-F. Li, Y.-Z. Xiong, C. Zhu, A. Chin, and D. L. Kwong, "High capacitance density ($>$ 17 fF/μm^2) Nb_2O_5—Based MIM capacitors for future RF IC applications," in *VLSI Symp. Tech. Dig.*, 2005, pp. 56–57.

[17] K. C. Chiang, C. H. Lai, A. Chin, T. J. Wang, H. F. Chiu, J. R. Chen, S. P. McAlister, and C. C. Chi, "Very high density (23 fF/μm^2) RF MIM capacitors using high-κ TiTaO as the dielectric," *IEEE Electron Device Lett.*, vol. 26, no. 10, pp. 728–730, Oct. 2005.

[18] K. C. Chiang, A. Chin, C. H. Lai, W. J. Chen, C. F. Cheng, B. F. Hung, and C. C. Liao, "Very high-κ and high density TiTaO MIM capacitors for analog and RF applications," in *VLSI Symp. Tech. Dig.*, 2005, pp. 62–63.

[19] K. C. Chiang, C. C. Huang, A. Chin, W. J. Chen, S. P. McAlister, H. F. Chiu, J. R. Chen, and C. C. Chi, "High-κ Ir/TiTaO/TaN capacitors suitable for analog IC applications," *IEEE Electron Device Lett.*, vol. 26, no. 7, pp. 504–506, Jul. 2005.
[20] J. Nakahira, M. Kiyotoshi, S. Yamazaki, M. Nakabayashi, S. Niwa, K. Tsunoda, J. Lin, A. Shimada, M. Izuha, T. Aoyama, H. Tomita, K. Eguchi, and K. Hieda, "Low temperature ($< 500\ ^\circ$C) $SrTiO_3$ capacitor process technology for embedded DRAM," in *VLSI Symp. Tech. Dig.*, 2000, pp. 104–105.
[21] P.-Y. Lesaicherre, S. Yamamichi, H. Yamaguchi, K. Takemura, H. Watanabe, K. Tokashiki, K. Satoh, T. Sakuma, M. Yoshida, S. Ohnishi, K. Nakajima, K. Shibahara, Y. Miyasaka, and H. Ono, "A gbit-scale DRAM stacked capacitor technology with ECR MOCVD $SrTiO_3$ and RIE patterned RuO_2/TiN storage nodes," in *IEDM Tech. Dig.*, 1994, pp. 831–834.
[22] C.-J. Peng, H. Hu, and S. B. Krupanidhi, "Electrical properties of strontium titanate thin films by multi-ion-beam reactive sputtering technique," *Appl. Phys. Lett.*, vol. 63, no. 23, pp. 1038–1040, Aug. 1993.
[23] S. W. Jiang, Q. Y. Zhang, Y. R. Li, Y. Zhang, X. F. Sun, and B. Jiang, "Structural characteristics of $SrTiO_3$ thin films processed by rapid thermal annealing," *J. Cryst. Growth*, vol. 274, no. 3/4, pp. 500–505, Feb. 2005.
[24] S. Yamamichi, T. Sakuma, K. Takemura, and Y. Miyasaka, "$SrTiO_3$ thin film preparation by ion beam sputtering and its dielectric properties," *Jpn. J. Appl. Phys.*, vol. 30, no. 9B, pp. 2193–2196, Sep. 1991.
[25] J. L. Cousins and D. E. Kotecki, "Simulation of the variability in microelectronic capacitors having polycrystalline dielectrics," *IEEE Electron Device Lett.*, vol. 23, no. 5, pp. 267–269, May 2002.
[26] F. Gervais, *Handbook of Optical Constants of Solids* α, E. D. Palik, Ed. New York: Academic, 1991, p. 1035.
[27] K.-S. Tan, S. Kiriake, M. de Wit, J. W. Fattaruso, C.-Y. Tsay, W. E. Matthews, and R. K. Hester, "Error correction techniques for high-performance differential A/D converters," *IEEE J. Solid-State Circuits*, vol. 25, no. 6, pp. 1318–1327, Dec. 1990.
[28] J. A. Babcock, S. G. Balster, A. Pinto, C. Dirnecker, P. Steinmann, R. Jumpertz, and B. El-Kareh, "Analog characteristics of metal–insulator–metal capacitors using PECVD nitride dielectrics," *IEEE Electron Device Lett.*, vol. 22, no. 5, pp. 230–232, May 2001.

K. C. Chiang received the B.S. degree in materials science and engineers and the M.S. degree from the National Chiao-Tung University, Hsinchu, Taiwan, R.O.C., in 2002 and 2004, respectively. He is currently working toward the Ph.D. degree at the Department of Electronics Engineering, National Chiao-Tung University.

His current research interests include high-κ materials for CMOS gate dielectrics and metal–insulator–metal capacitor applications.

Ching-Chien Huang was born in Kaohsiung, Taiwan, R.O.C., on October 18, 1982. He received the B.S. degree from the Electrical Engineering Department, National Sun Yat-Sen University, Kaohsiung, Taiwan, in 2004. He is currently working toward the Ph.D. degree at the Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan.

His current research interests include "Si electronic device technology" and "CMOS RF IC technology."

G. L. Chen received the B.S. degree in electrical engineering from the National Sun Yat-Sen University, Kaohsiung, Taiwan, R.O.C., in 2005. He is currently working toward the M.S. degree at the Department of Electronics Engineering, National Chiao-Tung University, Hsinchu, Taiwan, R.O.C.

His current research interest is in nonvolatile random access memory.

Wen Jauh Chen was born in Kaohsiung, Taiwan, R.O.C., on December 1, 1958. He received the B.S. degree in chemical engineering from Feng Chia University, Taichung, Taiwan, in 1983, the M.S. degree from the Graduate Institute of Materials Engineering, National Taiwan University, Taipei, Taiwan, R.O.C., in 1985, and the Ph.D. degree from the Department of Materials Science and Engineering, National Tsing Hua University, Hsinchu, Taiwan, R.O.C., in 1991.

From 1985 to 1986, he was with the Industrial Technology Research Institute, Hsinchu. From 1998 to 1999, he was with the National Center for Electron Microscopy, Lawrence Berkeley Laboratory, Berkeley, CA. Since 1992, he has been with the Department of Materials Science and Engineering, National Formosa University, Yunlin, Taiwan, R.O.C. He is currently a Professor with the National Pingtung University of Science and Technology, Pingtung, Taiwan, R.O.C. His research interests include silicide, diffusion barriers, and electronless plating.

H. L. Kao was born in Taipei, Taiwan, R.O.C. She received the B.S. degree in electrical engineering from Chang-Gung University, Tao-Yuan, Taiwan, R.O.C., in 1998, and the M.S. and Ph.D. degrees from the Department of Electronics Engineering, National Chiao-Tung University, Hsinchu, Taiwan, R.O.C., in 2000 and 2006, respectively.

In 2006, she joined the Department of Electronic Engineering, Chang Gung University. Her research interests include microwave and RF active devices.

Yung-Hsien Wu received the B.S. degree from the National Tsing-Hua University, Hsinchu, Taiwan, R.O.C., in 1996, and the Ph.D. degree in electronics engineering from the National Chiao-Tung University, Hsinchu, in 2000.

In 2000, he joined ProMOS Technologies, where he was engaged in advanced process development and assessment with major focus on DRAM and Flash memory. In 2005, he joined the Department of Engineering and System Science, National Tsing-Hua University, as an Assistant Professor. He has been granted 16 patents in his professional field in ProMOS Technologies. His current area of research interests include advanced process development for DRAM and nonvolatile memory, high-κ material for CMOS application, and Ge MOSFET fabrication and electrical characterization.

Albert Chin (SM'94) received the Ph.D. degree from the Department of Electrical Engineering, University of Michigan, Ann Arbor, in 1989.

He was with AT&T-Bell Labs from 1989 to 1990, General Electric-Electronic Lab from 1990 to 1992, and the Semiconductor Process and Device Center, Texas Instruments Incorporated from 1996 to 1997. He is currently a Professor with the National Chiao Tung University (NCTU), Hsinchu, Taiwan, R.O.C., the Deputy Director of the Nanometer Center, University System of Taiwan, NCTU, and a Visiting Professor at Si Nano Device Lab, National University of Singapore, Singapore. He has published more than 250 technical papers and presentations. His research interests include Si very large scale integration (VLSI), III–Vs, and RF devices. He invented the three-dimensional (3-D) IC integration to solve the power consumption and extend the VLSI scaling, Ge-on-insulator (GOI), high-κ Al_2O_3 and $LaAlO_3$ gate dielectrics, $\pm$5V operated metal-gate/high-κ/AlGaN/oxide metal–oxide–nitride–oxide–semiconductor memory device, resonant cavity photo-detector, and high mobility strain-compensated HEMT, etc. His works have been cited by high-quality International Electron Device Meeting (IEDM) and VLSI symposia papers from IC fabrications, universities, and *EETimes*, and currently in pilot runs at IC fabrications. He also developed the very high resistivity Si using an ion implantation process, generated traps, and much improved RF device performance close to GaAs has been realized up to 100 GHz. He is now working on 3-D IC, GOI, high-κ, metal gate, RF Si, nano-CMOS, and memory technologies. He has given invited talks at the IEDM and other conferences in the U.S., Europe, Japan, Korea (i.e., Samsung Electronics), etc.

Sean P. McAlister (SM'02) was born in Durban, South Africa. He received the M.Sc. degree from the University of Natal, Natal, South Africa, in 1968, and the Ph.D. degree in physics from Cambridge University, Cambridge, U.K., in 1971.

Following four years with Simon Fraser University, Vancouver, BC, Canada, he joined the National Research Council (NRC) of Canada, Ottawa, ON, in 1975. He has been involved in the fields of low-temperature physics, magnetism, and semiconductor materials and devices. He is a Principal Research Officer with the Institute for Microstructural Sciences, NRC, and leads efforts in device physics. His interests are in the design, simulation, fabrication, and characterization of electronic and optoelectronic devices.