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Comparison of InGaAs MOSFETs with germanium-on-insulator CMOS

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Abstract

High mobility channel materials such as Ge and compound semiconductors (CS) show promise for future generation MOSFETs. The challenge is to integrate these materials with a Si substrate and create good interfaces in the devices. Here we show dislocation-free CSOI and Ge-on-insulator (GOI) devices with good characteristics. The InAlAs/InGaAs/InAlAs-OI on Si MESFETs shows a mobility of 8100 $cm^2/V s$. To reduce the leakage current an Al_2O_3/InGaAs MOSFET was fabricated. Good 451 $cm^2/V s$ mobility was obtained, higher than the 340 $cm^2/V s$ of GOI MOSFETs. However the marginally better mobility than GOI and 18X lower mobility than MESFETs indicate that the soft phonon scattering, high-κ interface scattering and process variations are challenges for CS MOSFETs. In contrast, the GOI CMOS provides a simpler process and significantly higher electron and hole mobilities than its Si counterparts.

Keywords: Compound semiconductor FETs; Germanium-on-insulator; InGaAs MOSFET

1. Introduction

To continue current VLSI scaling trends, high-κ dielectrics and metal-gates [1–7] have to be integrated into CMOS to reduce the large leakage current and DC power consumption. However, the mobility degradation in metal-gate/high-κ/Si CMOSFETs is a challenge. This mobility degradation is due to the ionic nature of the high-κ dielectric, which leads to additional soft-phonon scattering. One method to overcome this problem is to use strained-Si [4]; but this compromises the mobility enhancement, compared with the currently used poly-Si/SiON/strained-Si. A high mobility results in high transistor drive current, and is a key factor for achieving high circuit speeds. Thus it is desirable to improve the mobility beyond that of strained-Si devices. One candidate is Ge which shows significantly higher electron and hole mobilities compared with strained-Si. In this case, a Ge-on-insulator (GOI) structure is needed to reduce the transistor's off-state leakage current which arises from the small energy band gap of Ge [8–13]. III–V MOSFETs have the potential of providing even higher electron mobilities. However, the technology challenge is to integrate III–V material with Si and

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form good interfaces in the MOSFET. Here we show the integration of a III–V material on Si, thus creating a compound semiconductor (CS) on-insulator (CSOI) device, using a process similar to that of our previous low-temperature wafer-bonded GOI [8–13]. The high electron mobility transistor (HEMT) [14–16] InAlAs/InGaAs/InAlAs-OI on Si showed a dislocation-free structure and an 8100 $cm^2/V\,s$ electron mobility. For comparison we fabricated an Al_2O_3/InGaAs MOSFET, which gave a significantly lower mobility than the InAlAs/InGaAs HEMTs. However, the mobility value was higher than that of GOI devices [9]. The mobility improvement was limited by soft-phonon and interface scattering.

2. Experimental procedure

The first goal was to integrate the III–V material onto Si by forming a wafer-bonded CSOI structure, as shown in the process of Fig. 1. An inverted InAlAs/InGaAs/InAlAs HEMT structure was first grown on InP by molecular beam epitaxy (MBE) [14–16]. Then a SiO_2 layer was deposited on top of the InAlAs and the target Si wafer. To enhance the wafer-bonding at low temperatures an O_2^+ exposure was used to activate the SiO_2 surfaces, and the bonding was performed at 400 °C [8–12]. Then the InP substrate was thinned down followed by selective etching of the InP and InAlAs. InGaAs is a good etch stop when using an HCl-based solution, compared with InP and InAlAs. To fabricate a CSOI HEMT, the top n^+ InGaAs contact layer over the gate was recess-etched to the InAlAs, where the gate electrode was formed by a Ti/Au Schottky contact. Then the source–drain contacts were formed by NiGeAu deposition [16].

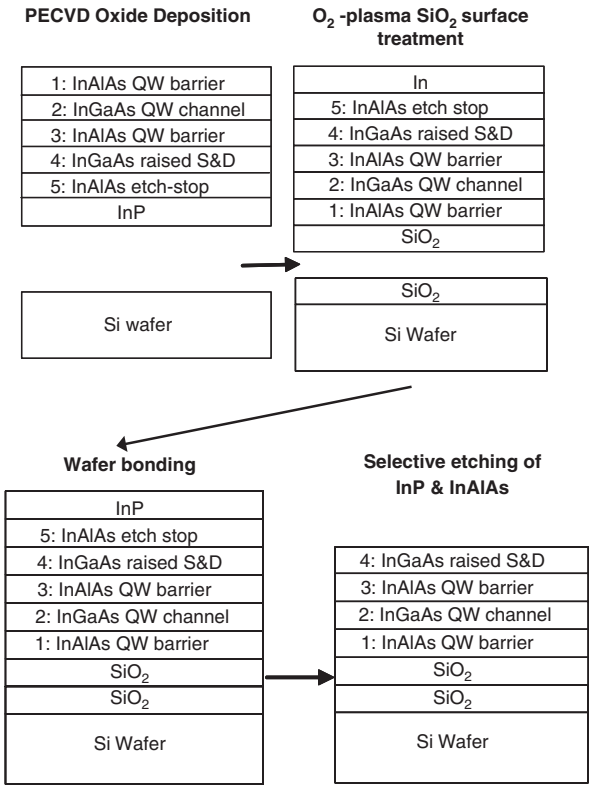

Fig. 1. Schematic of the process used to form the InAlAs/InGaAs/InAlAs-on-insulator structure.

A high-κ/III–V MOSFET was also investigated in this study [17]. We used MBE to grow the 20 nm-InGaAs/300 nm-InAlAs quantum-well (QW) structure on an InP substrate. Then the Al_2O_3 gate dielectric was deposited by RF sputtering from an Al_2O_3 source. To study the Al_2O_3/InGaAs interface properties, the InGaAs surface with or without in situ atomic Al layer coverage was investigated before exposing the InGaAs to air. The Al-gate/Al_2O_3/InGaAs/InAlAs MOSFET was fabricated by gate patterning, self-aligned Al/Yb deposition, and 400 °C rapid thermal annealing (RTA) to form the Schottky source–drain (SSD) contacts [18–20]. Such SSD contacts for InGaAs can avoid the difficult challenge of n^+ ion implantation activation for source–drain contacts, as used in conventional CMOSFET fabrication.

3. Results and discussion

3.1. InAlAs/InGaAs/InAlAs-OI transistor

An InAlAs/InGaAs/InAlAs-OI device was examined by cross-sectional transmission electron microscopy (TEM), as shown in Fig. 2(a), where no dislocations were seen at the resolution shown—this is important for high-yield IC fabrication. The white line in the middle of the SiO_2 layer is due to the O_2-plasma treatment, which is important for low temperature (400 °C) wafer-bonding and good mechanical strength. The CSOI design, which uses an inverted HEMT layer structure, is shown in Fig. 2(b), and consists of an InAlAs barrier layer, two-dimensional (2D) planar n^+ Si doping layer, InAlAs top QW barrier, InGaAs QW channel, and InAlAs bottom QW barrier on the SiO_2/Si substrate.

Fig. 3 shows the I_d– V_d characteristics of a 1.1 μm InAlAs/InGaAs/InAlAs CSOI transistor. For comparison, data for a 0.35 μm SiO_2/Si MOSFET are

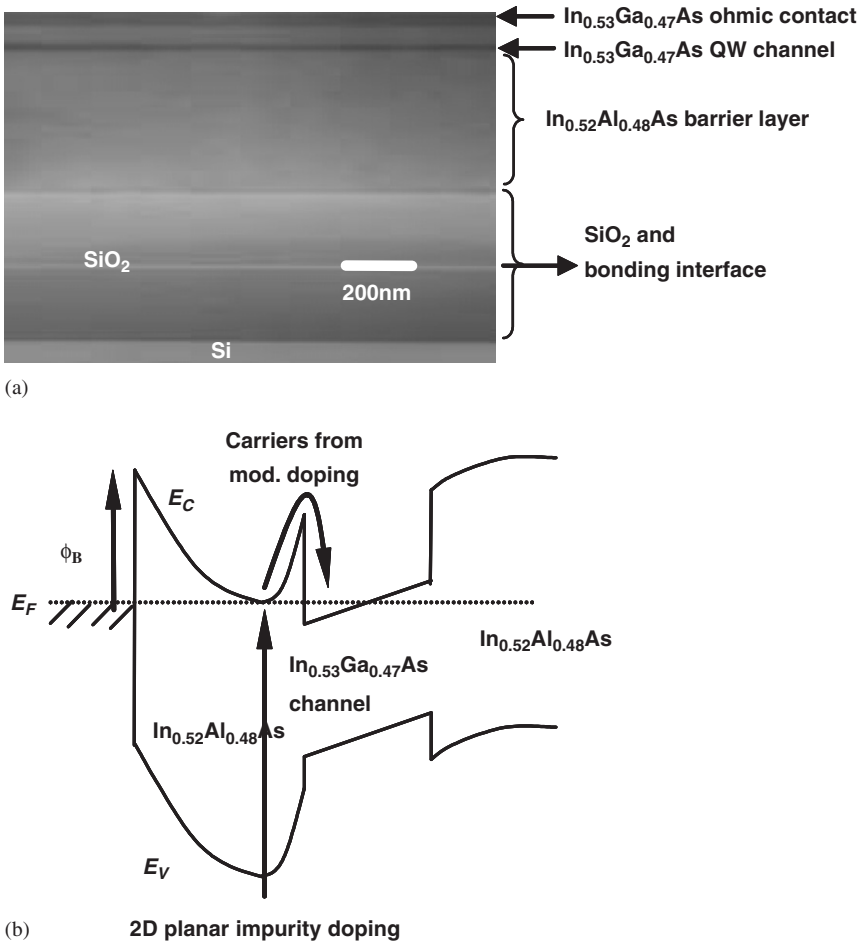

Fig. 2. Cross-sectional TEM and band diagram of the InAlAs/InGaAs/InAlAs FET structure. The middle InGaAs provides the channel, confined by InAlAs barriers. The upper InGaAs in the gate region was etched before depositing the metal gate.

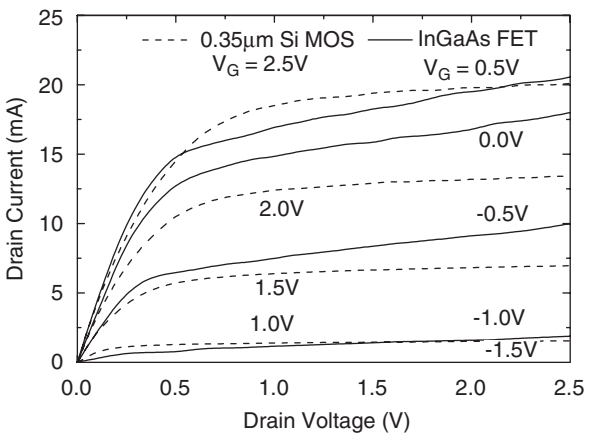

Fig. 3. Comparison of the I_d–V_d characteristics of InAlAs/$In_{0.53}Ga_{0.47}As$ CSOI MESFETs on Si (1.1 μm × 50 μm) with 0.35 μm Si MOSFETs.

included. A high drive current of 0.41 mA/μm was measured, which is close to that for a 0.35 μm SiO_2/Si MOSFET. Such a high drive current in the CSOI HEMT is due to the high electron mobility of 8100 $cm^2/V\,s$, which was determined using Hall measurements. The carrier density was $2.2 \times 10^{12}\,cm^{-2}$. The mobility value is nearly an order of magnitude higher than that for conventional Si and strained-Si devices.

3.2. Metal-gate/high-κ Al_2O_3/InGaAs MOSFET

It is well known that HEMTs or MESFETs are unsuitable for VLSI circuits due to their large gate leakage current. Therefore, a high-κ/InGaAs MOSFET structure is preferred over a HEMT design. Fig. 4 shows the I_d–V_d characteristics of an Al-gate/high-κ Al_2O_3/InGaAs QW MOSFET.

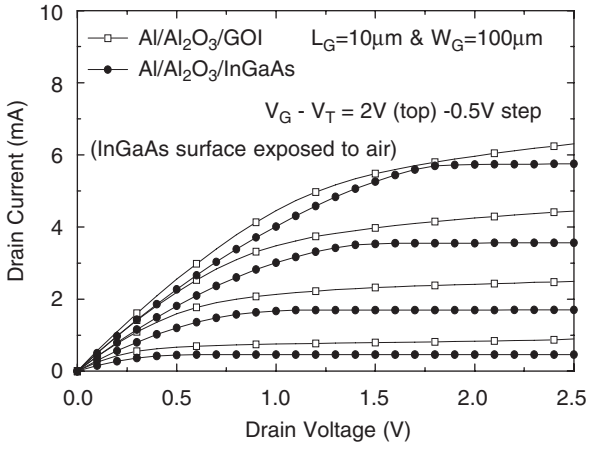

Fig. 4. I_d–V_d characteristics of $Al/Al_2O_3/InGaAs$ MOSFETs on insulating InAlAs/InP, with the InGaAs surface exposed to air.

For comparison, the I_d–V_d data from an Al_2O_3/GOI device is also shown [9]. Unfortunately, the drive current of the $Al/Al_2O_3/InGaAs$ nMOSFET is even less than that of an $Al/Al_2O_3/GOI$ transistor. It is known from MBE studies that the native oxides of $InGaO_3$ and As_2O_3 on InGaAs have weak bond strengths, requiring desorption temperatures of only ~500 °C. Therefore, the poor mobility of the $Al/Al_2O_3/InGaAs$ transistor may be due to these interfacial native oxides beneath the Al_2O_3 gate dielectric, as shown in the schematic diagram in Fig. 5. Such a weakly bonded poor-quality oxide may give a high concentration of interface states by forming dangling bonds. This can limit III–V MOSFET development.

To overcome this problem the top InGaAs surface was covered by an in situ deposited Al layer a few atoms thick, which was converted to Al_2O_3 after air exposure, and during subsequent Al_2O_3 sputtering under O_2^+ conditions. Fig. 6 shows the I_d–V_d characteristics of $Al_2O_3/InGaAs$ MOSFETs with an in situ covered InGaAs surface. Significantly improved drain current is shown—better than the Al_2O_3/GOI and Al_2O_3/Si MOSFETs.

Such a drive current improvement is due to the higher electron mobility, as shown in Fig. 7. The mobility of the $Al_2O_3/InGaAs$ transistor, with an improved interface, was 451 $cm^2/V\,s$, which is 1.3 times higher than for an Al_2O_3/GOI MOSFET, and 2.5 times higher than that for the Al_2O_3/Si device. However, this mobility in $Al_2O_3/InGaAs$ MOSFET is still ~18 times lower than that of the HEMT, indicating that the soft-phonon and interface

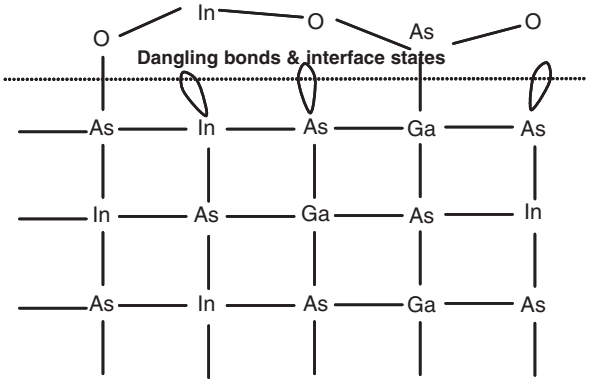

Fig. 5. Schematic diagram of III–V oxide on InGaAs. Unlike SiO_2/Si, more dangling bonds may be formed with the weak $InGaO_3$ and As_2O_3 oxide on the InGaAs.

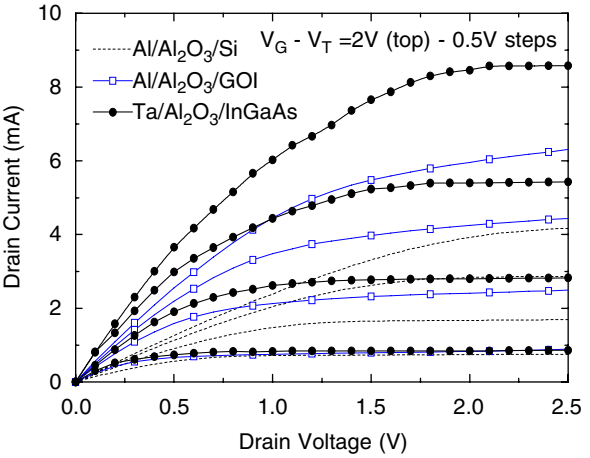

Fig. 6. I_d–V_d characteristics of $Al/Al_2O_3/InGaAs$ UTB MOSFETs on insulating InAlAs/InP, with an in situ covered Al_2O_3 on the InGaAs.

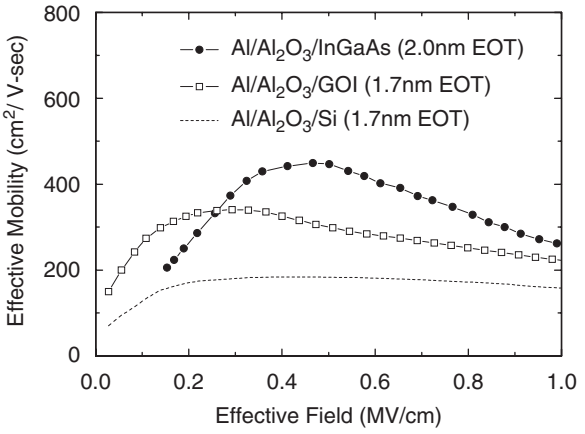

Fig. 7. Electron mobility of an $Al_2O_3/InGaAs$ MOSFET compared with Si and GOI devices.

scattering are still limiting factors for the Al_2O_3/InGaAs MOSFETs, even through the interface was covered by in situ deposited Al and converted into Al_2O_3.

4. Conclusions

We have fabricated defect-free InAlAs/InGaAs/InAlAs-OI on Si, and high drive current CSOI HEMTs with a high 8100 $cm^2/V s$ mobility. The Al_2O_3/InGaAs MOSFET with an in situ interface treatment gave 1.3 or 2.5 times higher mobility than that of Al_2O_3/GOI or Al_2O_3/Si MOSFETs, respectively, but an inferior mobility compared with the HEMT structure. This suggests that the soft-phonon and interface scattering are the mechanisms limiting the performance.

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