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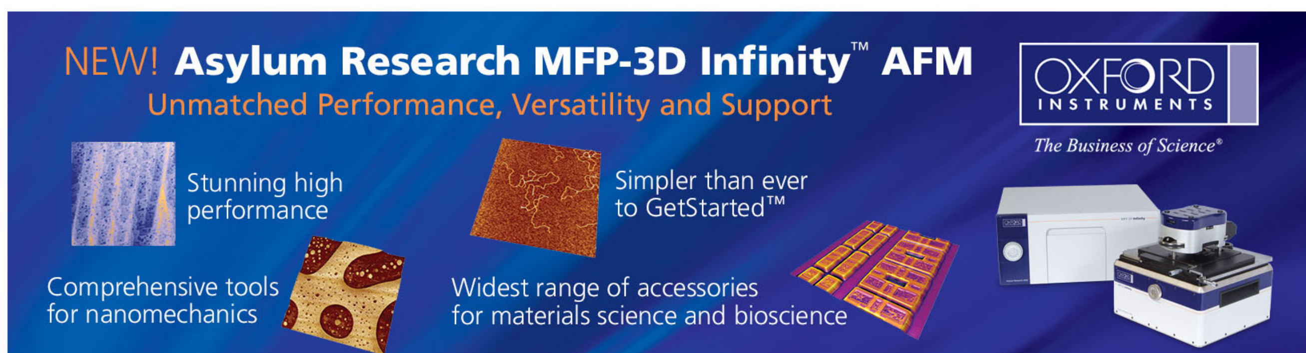

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Formation of germanium nanocrystals embedded in silicon-oxygen-nitride layer

Chun-Hao Tu
Institute of Electronics, National Chiao Tung University, Hsin-Chu, Taiwan 300, Republic of China

Ting-Chang Chang[a)]
Department of Physics, National Sun Yat-Sen University, Kaohsiung, Taiwan, Republic of China and Institute of Electro-Optical Engineering, National Sun Yat-Sen University, Kaohsiung, Taiwan, Republic of China and Center for Nanoscience and Nanotechnology, National Sun Yat-Sen University, Kaohsiung, Taiwan 804, Republic of China

Po-Tsun Liu
Department of Photonics, National Chiao Tung University, Hsin-Chu, Taiwan 300, Republic of China and Display Institute, National Chiao Tung University, Hsin-Chu, Taiwan 300, Republic of China

Hsin-Chou Liu, Chia-Chou Tsai, Li-Ting Chang, Tseung-Yuan Tseng, Simon M. Sze, and Chun-Yen Chang
Institute of Electronics, National Chiao Tung University, Hsin-Chu, Taiwan 300, Republic of China

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The formation of germanium nanocrystals embedded in silicon-oxygen nitride with distributed charge storage elements is proposed in this work. A large memory window is observed due to isolated Ge nanocrystals in the SiON gate stack layer. The Ge nanocrystals were nucleated after high temperature oxidized SiGeN layer. The nonvolatile memory with the Ge nanocrystals embedded in SiON stack layer exhibits 4 V threshold voltage shift under 10 V write operation. Also, the manufacture technology using the sequent high-temperature oxidation of the *a*-Si layer acting as the blocking oxide is proposed to enhance the performance of nonvolatile memory devices. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2227059]

In the past few years, the portable electronic devices have significantly impacted the market of consumer electronics. Because of the low working voltage and nonvolatility, the selection of storage media for most portable electronic devices is the flash memory which almost bases on the structure of the continuous floating gate[1,2] (FG). To date, the stacked-gate FG device structure continues to be the most prevailing nonvolatile-memory implementation, and is widely used in both independent and embedded memories. The invention of FG memory impacts more than the replacement of magnetic-core memory, and creates a moment of portable electronic systems. Despite a huge achievement in commercializing, conventional FG devices have some drawbacks.[2] The most prominent one is that once there is a charge leakage path (resulting from P/E-cycle degradation) in gate oxide, all the charges stored in the floating gate will leak away from this one single path because charges are stored in continuous energy level (conduction band) in FG. Nanocrystal memories have been presented in the mid-90s as a possible alternative to conventional FG nonvolatile memory devices, by allowing further decrease in the tunnel oxide. In a nanocrystal nonvolatile memory device, charge is not stored on a continues FG poly-Si layer, but instead on a layer of discrete, mutually isolated, crystalline nanocrystals or dots. Also, the nanocrystal memory device can avoid the charge leakage and lower the power consumption when tunneling oxide is thinner.[3–5]

The self-assembling of silicon or germanium nanocrystals embedded in SiO_2 layers has been widely studied, and strong memory effects in metal-oxide semiconductor (MOS) devices were reported.[3,6,7] Recently, different charge storage elements have been studied to achieve the robust distributed charge storage.[8–13] In this contribution, the germanium-incorporated silicon nitride (SiGeN) was investigated to be a self-assembling layer. The self-assembling layer of SiGeN, fabricated by the directly depositing using plasma enhanced chemical vapor deposition (PECVD) system. The following *a*-Si was also deposited in one chamber system by using PECVD. The sequent thermal oxidation was performed in thermal furnace at 900 °C to form blocking oxide layer and nucleate Ge nanocrystals. The structure with Ge embedded SiON layer exhibits obvious charge-trapping memory effects under electrical measurements. Also, material analysis techniques such as Raman spectroscopy and transmission electron microscopy (TEM) were utilized to observe the Ge nanocrystals nucleation in the oxidized SiGeN film.

Figure 1 exhibits the process flow in this work. First, a 5-nm-thick thermal oxide was grown as the tunnel oxide on *p*-type Si substrate by dry oxidation in an atmospheric pressure chemical vapor deposition (APCVD) furnace. Subsequently, a 20 nm amorphous silicon germanium nitride layer

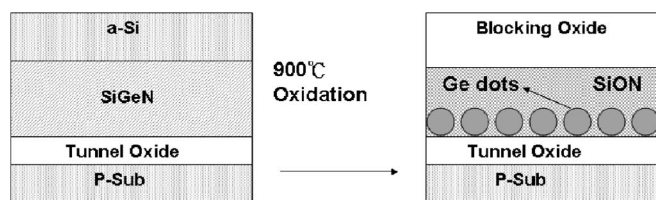

FIG. 1. The process flow proposed in this work.

[a)]Electronic mail: tcchang@mail.phys.nsysu.edu.tw

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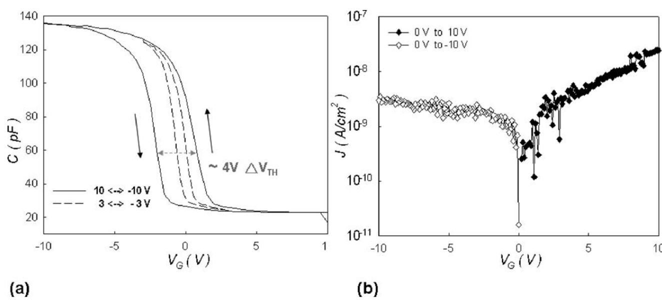

FIG. 2. (a) The capacitance-voltage (C-V) hysteresis of the MOIOS structure. The electrical C-V measurements are performed by bidirectional voltage sweeping from (1) from 10–(−10) V and (−10)–10 V; (2) from 3–(−3) V and (−3)–3 V. (b) The current density measurement by voltage sweeping from (1) 0–10 V and (2) 0–(−10) V.

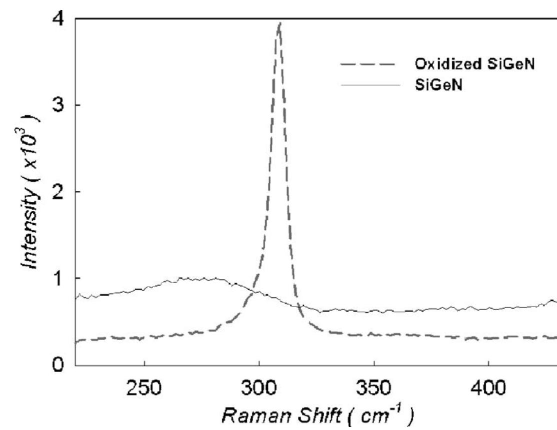

FIG. 3. Raman spectra of the SiGeN with a top capping a-Si layer, before and after the thermal oxidation process.

was deposited by PECVD on the tunnel oxide, followed by deposition of 20 nm amorphous silicon. The oxidation process was performed to fabricate the oxygen-incorporated SiO_2 served as blocking oxide, and the oxidation temperature was 900 °C. Furthermore, the SiGeN layer is also oxidized to nucleate the Ge nanocrystals during the blocking oxide formation. Afterward, a steam densification at 900 °C was also performed for 180 s to densify the blocking oxide. The deposition of the SiGeN film was kept at 200 °C in a low pressure of 0.6 mTorr with precursors of SiH_4 [20 SCCM (SCCM denotes cubic centimeter per minute at STP)], GeH_4 (5 SCCM), NH_3 (30 SCCM), and N_2 (500 SCCM) and plasma power of 20 W. The low pressure of 0.6 mTorr during deposition leads the mean free path of electrons to be increased and to improve the uniformity of the thin film. The deposition conditions of a-Si film, such as temperature and pressure, were the same as that of the SiGeN film deposition. Next, the high temperature thermal oxidation was performed in the thermal furnace in oxygen ambient. The sequent steam oxidation was performed to improve the quality of oxidized a-Si layer as the blocking oxide. Finally, the Al gate was patterned and sintered to form a metal-oxide-insulator-oxide-silicon (MOIOS) structure with the insulator combined the Ge nanocrystals.

The Ge nanocrystals embedded SiON layer of a MOIOS memory device is utilized to capture the injected carriers from the channel, which causes a variation in the threshold voltage of the memory device. Figures 2(a) and 2(b) show the capacitance-voltage (C-V) hysteresis and the current-voltage (I-V) characteristics of the MOIOS structure, respectively. The electrical C-V measurements were performed by the bidirectional voltage sweeping. The sweeping conditions were split as follows, (I) operated from 10 to −10 V, and reversely, (II) from 3 to −3 V and reversely. It is clearly shown in Fig. 2(a) that the threshold voltage shift (memory window ΔV_t) of the MOIOS structure is prominent for 900 °C oxidation. When the device is programmed, the electrons directly tunnel from the Si substrate through the tunnel oxide, and are trapped in the forbidden gap of Ge nanocrystals in the SiON layer. For the erasion, the holes may tunnel from the valence band of the Si substrate and recombine with the electrons trapped in the Ge nanocrystals in SiON layer. The blocking oxide is utilized to prevent the carriers of gate electrode from injecting into the charge-trapping layer by Fowler-Nordheim (FN) tunneling. The threshold voltage shift after the 10 V programming operation is 4 V for the Ge nanocrystals embedded in SiON memory device with a-Si layer layer oxidized at 900 °C. The large threshold voltage shift of memory device with oxidized a-Si film as blocking oxide layer is attributed to the presence of Ge nanocrystals in the SiON film. When electrons are captured in the Ge nanocrystals of the SiON film, a large threshold voltage shift is shown for a memory device. The leakage current in the MOIOS structure is shown in Fig. 2(b). It is tolerable for MOIOS structure with Ge nanocrystals embedded SiON layer to avoid the storaged charge leaking to gate.

Raman spectra of the SiGeN stack film followed by an oxidation process are schematically shown in Fig. 3. The crystalline phase for Ge is not found for as-deposited SiGeN layer using PECVD system. However, the Ge–Ge bonds are present in the SiGeN film after thermal oxidation. As a result of the fact that Si easily combines with oxygen first to form SiO_2,[13] the Ge will be nucleated after the thermal oxidation. The signal of Ge–Ge bonding is clearly found after the thermal oxidation, as shown in Fig. 3. The Ge nanocrystals in SiGeN layer are self-assembling after high temperature thermal oxidation. The nucleated Ge nanocrystals are as shown in Fig. 4. Hence, memory windows were formed after being programmed for the oxidized proposed material SiGeN in this experiment.

For the SiO_2 originated from oxidized a-Si film, there are dangling bonds or defects existing in the bulk and at the

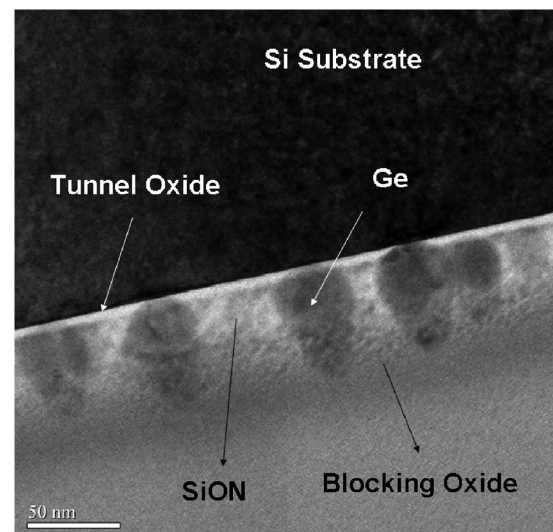

FIG. 4. The TEM analysis of thermal oxidized SiGeN layer.

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interface between SiGeN and SiO_2 layers. The electrons trapped near the channel will dominate the threshold voltage significantly than those far from the channel. The proposed Ge nanocrystals embedded in SiON stack layer with high-temperature oxidized *a*-Si layer, therefore, contributes both larger memory window and the additional blocking oxide deposition for the nonvolatile memory application promisingly.

In conclusion, the technology to easily form Ge nanocrystals embedded SiON stack film with both distributed storage elements and upside blocking oxide has been demonstrated for memory application. Memory windows after programming were resulted from the Ge nanocrystals embedded in SiON layer. The exhibition of memory windows after programming is resulted from the the formation of Ge nanocrystals in SiON layer. The material of SiGeN severed as self-assembling layer was proposed and performed in this study.

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