A Novel Transient Characterization Technique to Investigate Trap Properties in HfSiON Gate Dielectric MOSFETs—From Single Electron Emission to PBTI Recovery Transient

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***Abstract*—A positive bias temperature instability (PBTI) recovery transient technique is presented to investigate trap properties in HfSiON as high-k gate dielectric in nMOSFETs. Both large- and small-area nMOSFETs are characterized. In a large-area device, the post-PBTI drain current exhibits a recovery transient and follows logarithmic time dependence. In a small-area device, individual trapped electron emission from HfSiON gate dielectric, which is manifested by a staircase-like drain current evolution with time, is observed during recovery. By measuring the temperature and gate voltage dependence of trapped electron emission times, the physical mechanism for PBTI recovery is developed. An analytical model based on thermally assisted tunneling can successfully reproduce measured transient characteristics. In addition, HfSiON trap properties, such as trap density and activation energy, are characterized by this method.**

***Index Terms*—HfSiON, high-k trap properties, positive bias temperature instability (PBTI) recovery transient, single electron emission, thermally assisted tunneling.**

I. Introduction

THE AGGRESSIVE CMOS device scaling has been reaching the physical limit of conventional SiO_2 MOSFETs as a result of significant direct tunneling current through ultrathin oxides [1]. The resultant intolerable standby power consumption has made further oxide scaling impractical. To resolve this dilemma, high-permittivity (high-k) materials have emerged as a post-SiO_2 solution [2]. Among the candidates, Hf-based materials are most promising, and considerable efforts have been devoted to their film compositions [3], [4], process optimization [5], [6], as well as reliability assessment and analysis [7]–[9]. Recently, HfSiON has been successfully integrated into CMOS devices as gate dielectric for low-power applications with good reliability, comparable mobility (as SiO_2), and greatly reduced gate leakage [6].

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Several reliability issues for high-k gate dielectrics are being studied, including threshold voltage (V_t) instability [10], [11], charge trapping [9], [12], degradation [13], [14], and breakdown [8], [14], and [15]. Pantisano *et al.* reported that V_t instability in high-k gate dielectric CMOS is mainly controlled by the dynamics of electron charging/discharging in preexisting high-k bulk defects [10]. Young *et al.* concluded that fast electron trapping is a significant source of observed device dc performance degradation [11]. Shanware *et al.* found that charge trapping in HfSiON exhibits logarithmic time dependence [9]. Crupi *et al.* [13] and Degraeve *et al.* [14] indicated that traps at shallow and deep energies are respectively responsible for V_t instability and stress-induced leakage current (SILC). Moreover, high-k bulk trap density is demonstrated to strongly correlate to yield in terms of dielectric breakdown [8]. Thermochemical breakdown with a leakage current acceleration model was proposed to explain high-k dielectric breakdown [15].

Unlike SiO_2 gate dielectric CMOS, where negative bias temperature instability (NBTI) in pMOSFETs dictates device lifetime [16], high-k CMOS lifetime is believed to be limited by positive bias temperature instability (PBTI) in nMOSFETs [7], [12]. Similar to NBTI effects in conventional SiO_2 devices, high-k-induced PBTI degradation (charge trapping) and recovery (charge detrapping) are both considered to be important in determining high-k device lifetime [12], [19]. Conventionally, BTI characterization is carried out by periodically interrupting stress to measure electrical parameters, introducing a delay between stress and measurement, which may give rise to an imprecise or even incorrect result [17]–[20]. Recently, two-frequency charge pumping (CP) measurement has been utilized to characterize high-k trap properties [8], [14]. However, the CP measurement still has three drawbacks. 1) The CP current may be too small to be measured in small-size devices at a lower frequency. 2) Due to the mixture of interface and high-k traps, the two-frequency CP method may not be viable when high-k trap density is comparable to or even less than interface trap density. 3) CP alone cannot provide detailed description for high-k trap behavior such as trap activation energy.

In this paper, we develop a novel transient characterization technique to explore high-k trap properties by measuring the poststress recovery drain current transient in large- and small-area devices. In small-area devices, single-charge phenomenon

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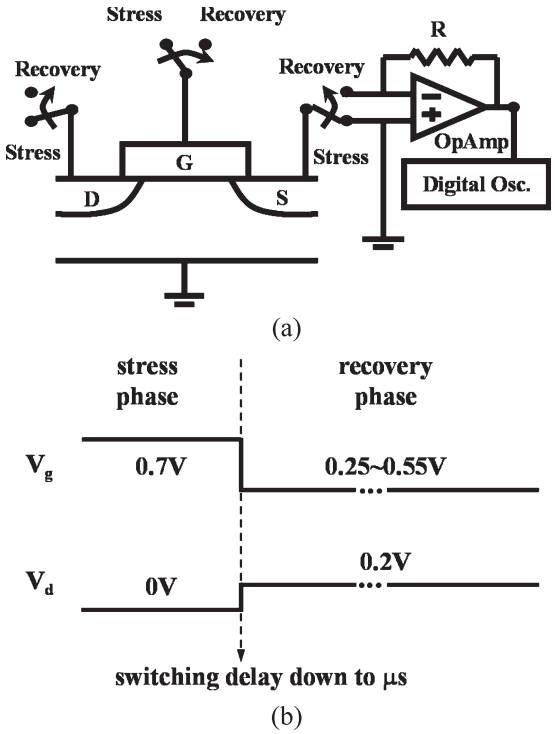

Fig. 1. (a) Schematic diagram for PBTI recovery transient measurement. High-speed switches minimize the transition delay down to the microsecond range between stress and recovery. (b) Waveforms applied to the gate and drain during stress and recovery phases.

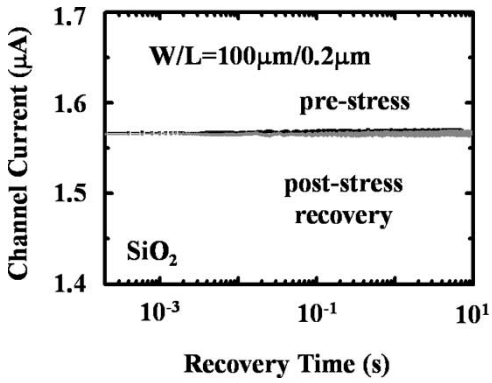

Fig. 2. Evolutions of drain current before and after stress in a MOSFET with SiO_2 as gate dielectric, measured by the experimental setup in Fig. 1.

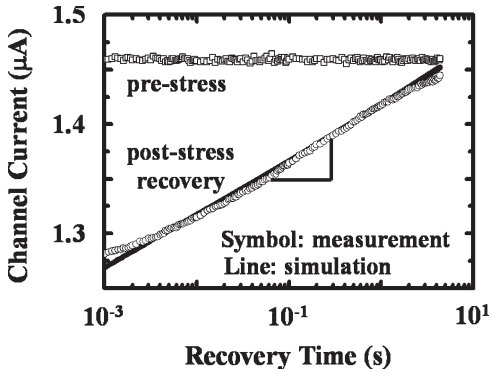

Fig. 3. Temporal evolutions of drain current before and after stress in a large-area high-k gate dielectric nMOSFET. $V_g = 0.7$ V, 0.2 s for stress and $V_g/V_d = 0.3$ V/0.2 V for recovery. The device dimension is $W/L = 100\ \mu\text{m}/0.08\ \mu\text{m}$. The symbols represent measurement data, and the line is the calculation result from (11).

is observed. Based on the temperature and voltage dependence of the single-charge effects, an analytical model for PBTI recovery is developed and high-k trap parameters are extracted. The model is further verified by comparison with measured transient characteristics in a large-area device.

II. PBTI Transient Measurement

The devices used in this paper are nMOSFETs with a polysilicon electrode and a bilayered gate dielectric stack consisting of HfSiON and an interfacial SiO_2 layer (IL). The gate width is 100 μm and 0.16 μm, and the gate length ranges from 80 to 220 nm. Detailed fabrication process and device characteristics can be found in [6] and [7]. The devices are first subjected to a positive gate bias (V_g) stress, and then "recover" at a lower V_g. In the "stress phase," electrons in the inversion channel are injected and trapped into preexisting high-k gate dielectric traps, whereas in the "recovery phase," the trapped charges escape via thermally assisted tunneling (TAT). The evolution of the recovery drain current (I_d) is monitored by a special measurement setup, as shown in Fig. 1(a). A conventional "sense-after-stress" method introduces a delay between phase transitions. This delay, as has been reported in literature for both NBTI in SiO_2 and PBTI in high k, leads to inaccurate experimental results [12], [17]–[20]. Thus, in our measurement setup [19], [20], a computer-controlled system including high-speed switches, an operational amplifier, and a digital oscilloscope is used to monitor I_d. The delay between stress and recovery is minimized down to the microsecond range. The sampling rate is 10^4 readings per second. Fig. 1(b) depicts the waveforms applied on gate and drain during stress and recovery. The system was tested on MOSFETs with SiO_2 as gate dielectric and stable current–time characteristic was obtained (Fig. 2), ensuring that the system introduces no spurious transient effect.

A. Recovery Transient in Large-Area Devices

The recovery transient of the drain current at $V_g/V_d = 0.3/0.2$ V in a large-area $(100\ \mu\text{m} \times 0.08\ \mu\text{m})$ nMOSFET is shown in Fig. 3 after stress at $V_g = 0.7$ V for 0.2 s. The prestress drain current is also plotted for comparison. The poststress I_d increases with a logarithmic time dependence for about four decades of time from 1 ms to 10 s and is saturated at a level close to the prestress one, suggesting full recovery for the chosen stress condition. Note that conventional measurement (for example, by Agilent 4156), which usually takes a few seconds between stress and recovery phase transition, is unable to measure the initial transient in the millisecond range in Fig. 3 and may significantly underestimate the magnitude of the transient effect. We repeat the same measurement (stress and recovery) on a SiO_2 control sample. The result is shown in Fig. 2, and no transient effect is noticed. This comparison implies that the observed transient should arise from the high-k gate dielectric rather than from the interfacial oxide layer.

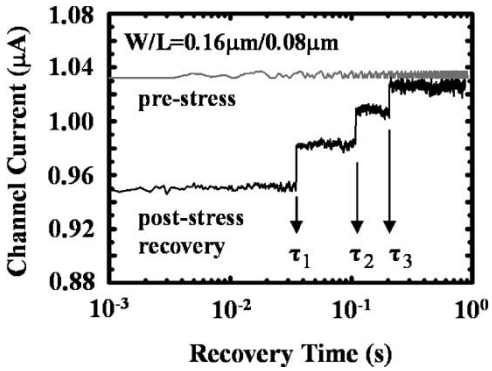

Fig. 4. Recovery drain current transients before and after stress in a small-area device. Bias conditions for stress and recovery are exactly the same as in Fig. 3. The device dimension is $W/L = 0.16\ \mu\text{m}/0.08\ \mu\text{m}$. Each current jump is attributed to single trapped charge escape from high-k gate dielectric. Only three electrons are trapped during stress. The emission time of the three trapped electrons is denoted as τ_1, τ_2, and τ_3.

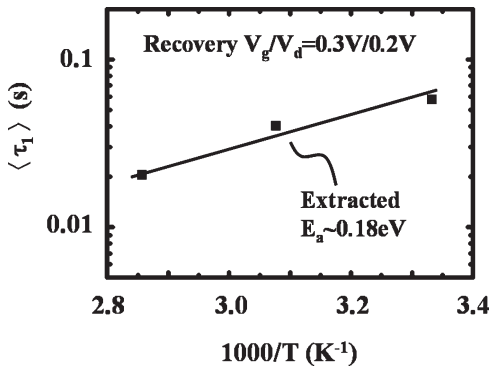

Fig. 5. Temperature dependence of $\langle\tau_1\rangle$. The activation energy extracted from the Arrhenius plot is 0.18 eV. Each data point is an average of ten readings.

B. Single Electron Emission in Small-Area Devices

We performed the same experiment (identical stress and recovery condition) on a small-area device ($W/L = 0.16\ \mu\text{m}/0.08\ \mu\text{m}$) where only a few traps are present. The recovery I_d, interestingly, exhibits a staircase-like evolution, as shown in Fig. 4. The poststress drain current returns to the prestress level, suggesting again full recovery. Each current jump in Fig. 4 is believed to be due to single electron emission from traps in HfSiON gate dielectric. Here, only three electrons are trapped in the measured device during stress. In Fig. 4, individual electron emission times τ_1, τ_2, and τ_3 can be clearly defined by this technique. We further explore the dependence of electron emission times on recovery gate voltage and temperature. We take an average of the electron emission times from ten measurements on the same device by repeated stress and recovery. Fig. 5 shows the temperature dependence of τ_1. The extracted activation energy (E_a) from the Arrhenius plot is about 0.18 eV. Fig. 6 shows the gate voltage dependence of the first two electron emission times. Both τ_1 and τ_2 increase with recovery V_g.

III. Results and Discussion

A. Trapped Charge Emission Model

Three possible paths for electron detrapping are illustrated in the energy band diagram in Fig. 7, namely: (a) Frenkel–Poole

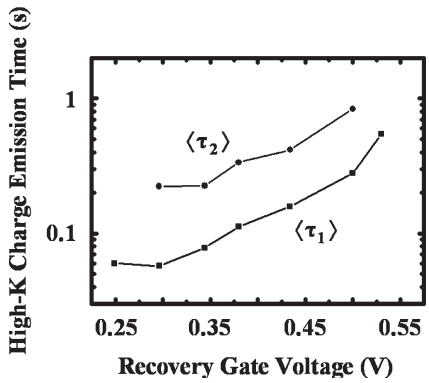

Fig. 6. Dependence of trapped electron emission time on recovery gate voltage. Ten measurements are made for each recovery V_g to take average.

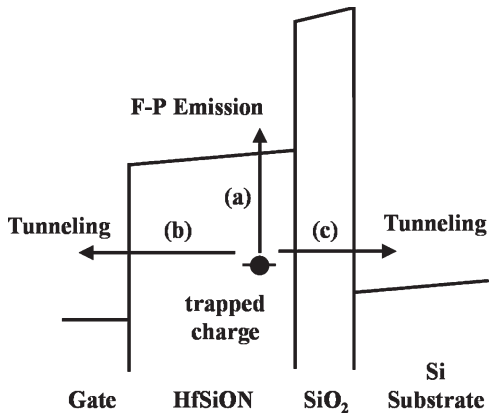

Fig. 7. Energy band diagram illustrating possible paths for trapped charge emission: (a) F–P emission. (b) Tunneling to the gate. (c) Tunneling to the Si substrate.

(F–P) emission; (b) Shockley-Read-Hall (SRH)-like TAT to the gate electrode; and (c) TAT to the Si substrate. The detrapping path (a) is ruled out, because the activation energy E_a for F–P emission should be about the trap energy (>1 eV) and the measured E_a is only 0.18 eV. Path (b) is also excluded, because a larger (more positive) recovery V_g would accelerate detrapping, giving a shorter charge emission time. The measured τ versus V_g is just opposite (Fig. 6). As a result, (c) is identified as the dominant path of trapped charge emission. Moreover, the temperature effect implies the role of thermal process in the charge tunneling process. As a result, an analytical model based on TAT is developed with the energy band diagram and trap distance illustrated in Fig. 8. According to the WKB approximation, the trapped charge emission time is formulated as

$$\tau_i^{-1} = \upsilon \exp(-\alpha_{\text{ox}} T_{\text{ox}}) \exp(-\alpha_k x_i) \tag{1}$$

where

$$\upsilon = N_C(1 - f_c)\upsilon_{\text{th}}\sigma_0 \exp\left(-\frac{E_a}{kT}\right) \tag{1a}$$

$$\alpha_{\text{ox}} = \frac{2\sqrt{2m^*_{\text{ox}} q(E_t + \Phi_B)}}{\hbar}$$

$$\alpha_k = \frac{2\sqrt{2m^*_k q E_t}}{\hbar}. \tag{1b}$$

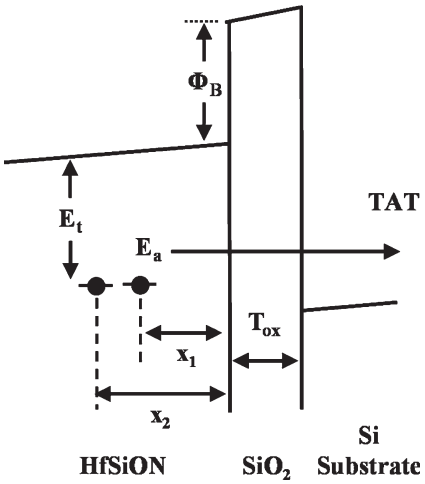

Fig. 8. Schematic representation of the band diagram in recovery phase and trap positions. E_a is the activation energy for SRH-like TAT.

The prefactor ν in (1) is a lumped parameter, often referred to as the "attempt-to-escape frequency," and is expressed in (1a), where N_C is the effective density-of-state in Si conduction band, f_c is the Fermi–Dirac (FD) distribution function in Si substrate at the energy aligned to the trapped charge, $N_C(1-f_c)$ is the amount of available states in Si substrate for outtunneling electrons from high-k traps, and σ_0 and E_a are the trap cross section and the activation energy, respectively. Other variables have their usual definitions. The FD distribution (f_c) is a function of V_g in recovery. A smaller recovery V_g leads to a smaller channel electron density, or a smaller f_c, and thus, a shorter electron emission time. As the recovery V_g reduces below the threshold voltage, f_c approaches zero, and thus, the electron emission time becomes independent of V_g, as shown in Fig. 6. The electron nearest to the interface of Si substrate will be the first for detrapping. In order to exclude the temperature effect resulting from the FD distribution, we chose a small recovery $V_g(\leq 0.3V)$, i.e., $f_c \sim 0$, in the measurement of trap activation energy E_a in Fig. 5.

B. High-k Bulk Trap Density

The high-k trap density (N_t) can be evaluated through the proposed analytical model. By comparing

$$\tau_1 = \upsilon^{-1} \exp(\alpha_{\rm ox} T_{\rm ox}) \exp(\alpha_k x_1) \tag{2a}$$

$$\tau_2 = \upsilon^{-1} \exp(\alpha_{\rm ox} T_{\rm ox}) \exp(\alpha_k x_2) \tag{2b}$$

we obtain

$$\frac{\tau_2}{\tau_1} = \exp\left[\alpha_k (x_2 - x_1)\right]. \tag{3}$$

Assuming the high-k traps have a uniform distribution in space, the high-k trap density is readily calculated as

$$N_t = \frac{1}{WL(x_2 - x_1)} = \frac{\alpha_k}{WL \ln\left(\frac{\tau_2}{\tau_1}\right)}. \tag{4}$$

Equation (3) predicts that the ratio of emission times (τ_2/τ_1) is only related to the physical distance between trap sites. Fig. 9

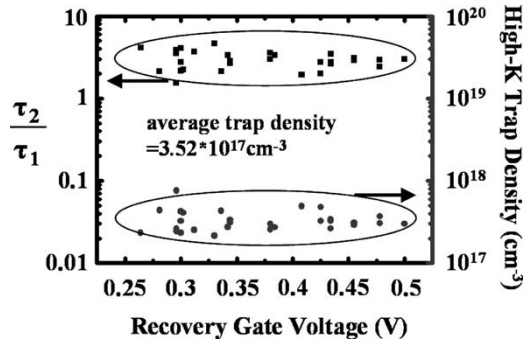

Fig. 9. Ratio of τ_2 to τ_1 versus gate voltage in the recovery phase. Note that τ_2/τ_1 remains almost unchanged with respect to V_g, as predicted by (3). The extracted high-k trap density is 3.5×10^{17} cm^{-3}, or equivalently, 8.8×10^{11} cm^{-2}.

indeed shows that τ_2/τ_1 (ten readings of each V_g on the same device; ten devices measured) is constant and is independent of recovery V_g. For measurement convenience, we chose certain fixed recovery currents rather than recovery voltages in Fig. 9, thus, leading to scattered data points as a result of threshold voltage variation. An average τ_2/τ_1 of 3.4 is obtained, corresponding to an average high-k trap density of $N_t = 3.5 \times 10^{17}$ cm^{-3} (assuming $m_k^* = 0.18$ m$_0$ [21]), or equivalently, an area density of 8.8×10^{10} cm^{-2}.

It should be pointed out that in the analysis above, we assume single trap energy. This assumption is reasonable, as the trap energy range corresponding to stress $V_g(= 0.7$ V) and recovery $V_g(= 0.3$ V) is very small. Only traps in this small energy range are charged and discharged in the measurement above. For a larger stress V_g, the injected electrons may fill high-k traps at different positions and energies. We will discuss this issue later.

C. Modeling of PBTI Recovery Transient in a Large-Area Device

In a large-area device, the high-k charge detrapping rate is given by

$$Q(x,t) = Q(x,0) \exp\left[\frac{-t}{\tau(x)}\right] \tag{5}$$

where $Q(x,t) = qN_t(x,t)$ is the time-dependent trapped charge density and τ(x) is described in (1). The threshold voltage shift ΔV_t induced by trapped electron emission is written as

$$\begin{aligned}\Delta V_t(t) &= -\sum_i \frac{\Delta Q(x_i,t)}{C(x_i)} \\ &= -\sum_i \frac{qN_t(x_i,0)}{\varepsilon_{\rm HK}} (T_{\rm HK} - x_i) \left[1 - \exp\left(\frac{-t}{\tau_i}\right)\right]\end{aligned} \tag{6}$$

where C(x_i) is the corresponding capacitance for trapped charges located at x_i from high-k/IL interface and $\varepsilon_{\rm HK}$ and $T_{\rm HK}$ are permittivity and physical thickness of the high-k layer,

respectively. For a large amount of trapped charges, the summation in (6) is substituted by an integration written as

$$\Delta V_t(t) = -\int \frac{qN_t(x,0)}{\varepsilon_{\rm HK}}(T_{\rm HK}-x)\left\{1-\exp\left[\frac{-t}{\tau(x)}\right]\right\}dx \tag{7}$$

where $\tau(x) = A\exp(\alpha_k x)$ and $A = [N_C(1-f_c)\nu_{\rm th}\sigma_0 \times \exp(-E_a/kT)]^{-1}\exp(\alpha_{\rm ox}t_{\rm ox})$. Because the double exponential $\exp[-t/\tau(x)] = \exp[(-t/A)\exp(-\alpha_k x)]$ in the integrand changes abruptly from 0 to 1 around $x = (\alpha_k)^{-1}\ln(t/A)$, it can be approximated by a step function written as

$$\exp\left[\left(-\frac{t}{A}\right)\exp(-\alpha_k x)\right] = \begin{cases} 0 & \text{for } x \le (\alpha_k)^{-1}\ln\left(\frac{t}{A}\right) \\ 1 & \text{for } x \ge (\alpha_k)^{-1}\ln\left(\frac{t}{A}\right) \end{cases}. \tag{8}$$

This approximation translates into a "clear-cut" picture; after time t, electrons with emission times shorter than t are completely detrapped while all of the rest remain trapped. Therefore, (7) is further simplified as

$$\Delta V_t(t) \approx -\frac{qN_t}{\varepsilon_{\rm HK}}\int_0^{(\alpha_k)^{-1}\ln\left(\frac{t}{A}\right)} (T_{\rm HK}-x)dx. \tag{9}$$

The time window of interest for modeling is four decades as shown in Fig. 3. According to (3), the time span is equivalent to a physical distance of around 10 Å in high k, or an equivalent oxide thickness (EOT) of 2 Å. Therefore, the term $T_{\rm HK}-x$ in (9) is approximated as a constant, or $\overline{x_{\rm eff}}$, and (9) reduces to

$$\Delta V_t(t) \approx -\frac{qN_t\overline{x_{\rm eff}}}{\varepsilon_{\rm HK}\alpha_k}\ln\left(\frac{t}{A}\right). \tag{10}$$

The corresponding recovery drain current evolution in the measurement interval can be written as

$$\Delta I_d(t) \propto \frac{qG_mN_t\overline{x_{\rm eff}}}{\varepsilon_{\rm HK}\alpha_k}\ln\left(\frac{t}{A}\right) \tag{11}$$

where $G_m(=dI/dV)$ is the transconductance. Using the extracted N_t and E_a from a small device, the simulated recovery transient from (11) is shown in Fig. 3 and is in good agreement with the measured result. Equation (11) also reveals that the recovery slope in Fig. 3 is linearly proportional to the high-k trapped charge density.

As mentioned earlier, the injected electrons may fill different energy traps at a larger stress V_g. In this case, the trap energy distribution should be taken into account, and (11) is modified as

$$\Delta I_d(t) \propto \left(\int_{\Delta E}\frac{qG_mN_t(E_t)\overline{x_{\rm eff}}}{\varepsilon_{\rm HK}\alpha_k(E_t)}dE_t\right)\ln(t) \tag{12}$$

where ΔE represents the energy range of trapped charges. Equation (12) shows that at a larger stress V_g, the recovery transient still follows logarithmic time dependence but has a larger slope because of a larger ΔE. Fig. 10 shows the measured recovery transients for two stress V_g. As expected, the larger stress V_g exhibits a larger slope.

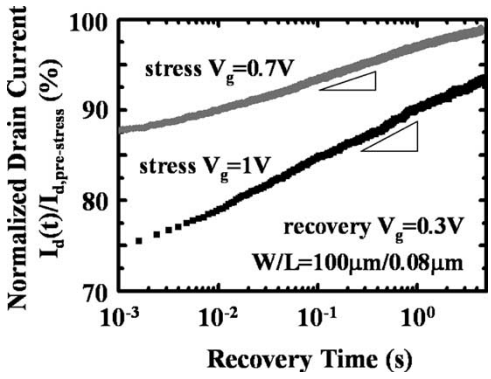

Fig. 10. Normalized drain current evolution with recovery time for two stress V_g (0.7 and 1 V). The V_g in the recovery phase is 0.3 V.

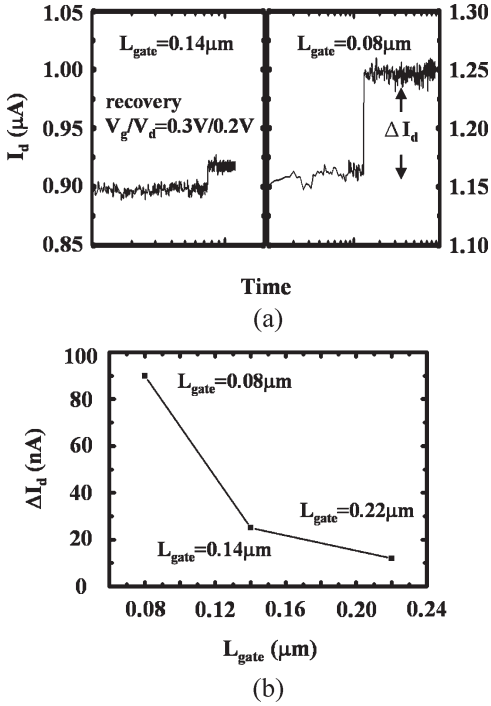

Fig. 11. (a) Comparison of the current jump amplitude for $L_{\rm gate} = 0.14$ μm and $L_{\rm gate} = 0.08$ μm. Both devices are subject to identical stress and recovery conditions. (b) Amplitude of the current jump versus $L_{\rm gate}$.

Finally, the authors would like to remark that we chose a very short stress time (0.2 s) in this paper, because the purpose of this paper is to characterize the preexisting traps in HfSiON gate dielectric. For a longer stress time and a larger stress V_g, additional high-k traps will be generated. The PBTI stress-induced high-k trap creation will be explored in our future publication.

D. Gate Length Effect

The single-charge effect is investigated on devices with different gate lengths, i.e., 0.08, 0.14, and 0.22 μm. Fig. 11 shows that the quantized feature in the recovery transient is still

observable for all the three lengths. However, the amplitude of the drain current step (ΔI_d) decreases with increasing gate length. This trend is consistent with the Random Telegraph Signal theory [22] and implies that the impact of the trapped electron in the high-k dielectric spreads over the entire channel.

IV. Conclusion

A novel transient measurement technique is proposed for characterizing high-k gate dielectric traps in HfSiON nMOSFETs. The quantized feature in recovery current evolution due to single-charge detrapping is observed for the first time in a small-area device. An SRH-like TAT model for high-k trapped charge emission is developed. Our model can well explain the measured electric field and temperature dependence of single-charge emission times. Our model also reveals that the recovery drain current transient in large-size devices should follow logarithmic time dependence. The high-k trap density can be extracted from charge emission times in a small device or from the drain current recovery slope in a large device. For trap activation energy, single-charge emission measurement is necessary, because the transient slope in a large device does not contain the activation energy. The proposed technique for single-charge effect characterization can provide insight into trap properties in high-k gate dielectrics in nanoscale CMOS device development.

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