# High-Performance Metal-Induced Lateral-Crystallization Polysilicon Thin-Film Transistors With Multiple Nanowire Channels and Multiple Gates

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***Abstract*—In this study, pattern-dependent nickel (Ni) metal-induced lateral-crystallization (Ni-MILC) polysilicon thin-film transistors (poly-Si TFTs) with ten nanowire channels and multigate structure were fabricated and characterized. Experimental results reveal that applying ten nanowire channels improves the performance of an Ni-MILC poly-Si TFT, which thus has a higher ON current, a lower leakage current, and a lower threshold voltage ($V_{\rm th}$) than single-channel TFTs. Furthermore, the experimental results reveal that combining the multigate structure and ten nanowire channels further enhances the entire performance of Ni-MILC TFTs, which thus have a low leakage current, a high ON/OFF ratio, a low $V_{\rm th}$, a steep subthreshold swing, and kink-free output characteristics. The multigate structure with ten-nanowire-channel Ni-MILC TFTs has a few poly-Si grain boundary defects, a low lateral electrical field, and a gate-channel shortening effect, all of which are associated with such high-performance characteristics.**

***Index Terms*—Metal-induced lateral-crystallization (MILC), multigate, nanowire, thin-film transistor (TFT).**

## I. Introduction

HIGH-PERFORMANCE thin-film transistors (TFTs) fabricated on a polysilicon film formed by metal-induced lateral crystallization (MILC) using Ni have attracted much interest because of their potential use in three-dimensional circuit technology [1], liquid crystal display (LCD) drivers, and system-on-panel (SOP) applications [2]. It is a low-cost batch process that yields superior polysilicon (poly-Si) films. However, the applications of Ni-MILC poly-Si TFTs remain limited, because the grain boundaries of poly-Si in the channel region substantially degrade performance. The electrical characteristics of the TFTs can be improved by reducing the number of defects in the poly-Si grain boundaries in the channel, and poly-Si TFTs with several multichannel have been reported to effectively reduce grain boundary defects [3], [4]. The Ni-MILC poly-Si TFT suffers from severe leakage current because of Ni contamination during MILC annealing [2], [5], [6], which is directly related to the lateral electrical field in the drain depletion region in the off-state. This is another major limitation of Ni-MILC poly-Si TFT applications. According to previous reports, the poly-Si TFT's adopted multigate structure can effectively reduce leakage current, thus addressing this leakage issue [7].

This study develops a single-gate structure with a single channel, a single-gate structure with ten nanowire channels, and three different multigate numbers with ten nanowire channels in the Ni-MILC poly-Si TFT to study their performance. The device simulation results are also performed to investigate the relationship between the electrical field and leakage current of multigate-structure TFTs.

TABLE I
DEVICE DIMENSIONS OF ALL PROPOSED Ni-MILC POLY-Si TFTs. ALL DEVICES HAVE THE SAME ACTIVE CHANNEL THICKNESS OF 50 nm AND GATE TEOS-OXIDE THICKNESS OF 50 nm

| Device name | Gate number | Each gate length (L) | Total length ($L_{tot}$) | Channel number | Each width (W) | Total width ($W_{tot}$) |
|---|---|---|---|---|---|---|
| G1S1 | 1 | 5 um | 5 um | 1 | 1 um | 1 um |
| G1M10 | 1 | 5 um | 5 um | 10 | 84 nm | 0.84 um |
| G2M10 | 2 | 2.5 um | 5 um | 10 | 84 nm | 0.84 um |
| G3M10 | 3 | 1.7 um | 5 um | 10 | 84 nm | 0.84 um |
| G2M10 | 4 | 1.25 um | 5 um | 10 | 84 nm | 0.84 um |

## II. Device Sturcture, Simulation, and Fabricaion

In this study, a series of Ni-MILC poly-Si TFTs were fabricated as listed in Table I: one with a single-gate length of 5 $\mu$m and a single-channel width of 1 $\mu$m (G1S1), one with a single-gate length of 5 $\mu$m and ten strips of 84-nm wire channels (G1M10), one with two gate, each gate having a length of 2.5 $\mu$m and ten strips of 84-nm wire channels (G2M10), one with three gates, each gate having a length of 1.7 $\mu$m and ten strips of 84-nm wire channels (G3M10), one with four gate, each gate having a length of 1.25 $\mu$m and ten strips of 84-nm

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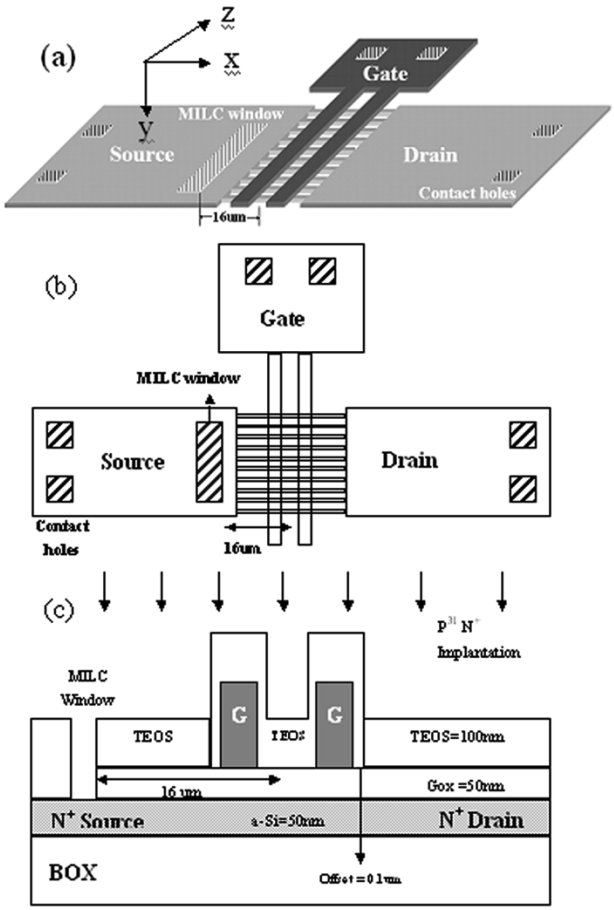


Fig. 1. (a) Schematic plot of a G2M10 Ni-MILC poly-Si TFT with source, drain, nanowire channels, an Ni-MILC seeding window, and a dual-gate structure. (b) Top-view plot of the G2M10 Ni-MILC poly-Si TFT. (c) Cross-sectional view of the Ni-MILC poly-Si TFT, which was a conventional top-gate, self-aligned offset MOSFET structure.

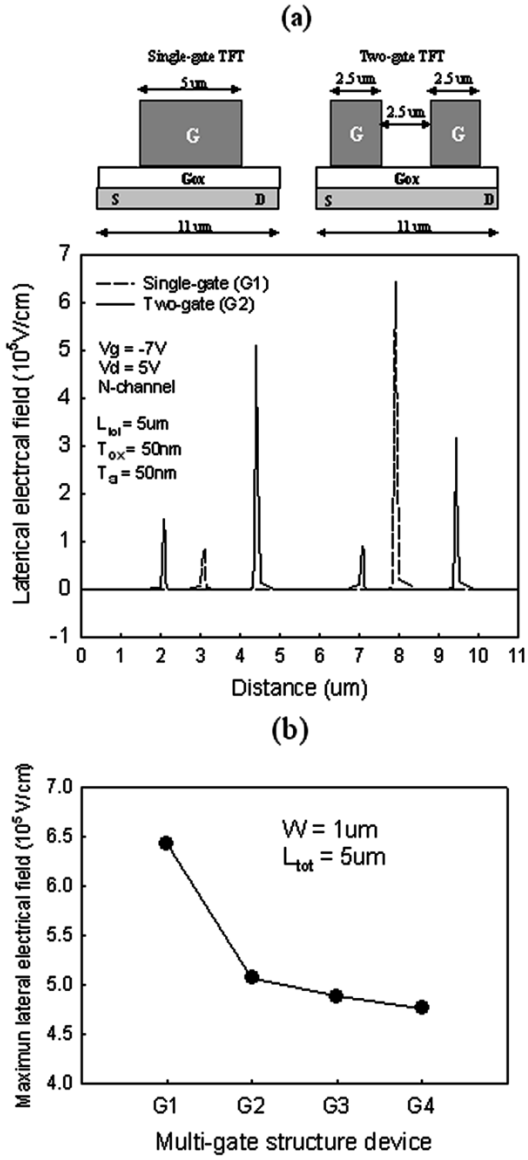


Fig. 2. (a) Off-state electrical field simulation results of single-gate and dual-gate poly-Si TFT by ISE TCAD v. 7 (a 2-D device simulator). (b) The peak lateral electrical file $(E_m)$ versus different gate-number TFT structures.

wire channels (G4M10). Fig. 1(a) presents the schematic plot of the G2M10 Ni-MILC poly-Si TFT with source, drain, nanowire channels, an Ni-MILC seeding window, and a dual-gate structure. Fig. 1(b) presents the top view of the G2M10 Ni-MILC poly-Si TFT. Fig. 1(c) presents the cross-sectional view of the Ni-MILC poly-Si TFT, with a conventional top dual-gate, self-aligned offset MOSFET structure with critical device dimensions. As the anomalous off-current (leakage current) in the poly-Si TFTs is related to the lateral electrical field in the channel, Fig. 2(a) presents the simulation results obtained using an ISE TCAD 2-D device simulator DESSIS of the lateral electrical field of the single-gate (G1) and dual-gate (G2) TFTs with the same device dimension and bias condition. The peak lateral electrical field $(E_m)$ of the dual-gate TFT is lower than that of the single-gate TFT, indicating that the dual-gate (G2) structure effectively reduces the leakage current of poly-Si TFTs. Fig. 2(b) presents $E_m$ versus different gate-number TFT structures. The $E_m$ is decreasing with increasing gate number.

The 6-in p-type single-crystal silicon wafers were coated with 400-nm-thick $SiO_2$ as the starting materials. An undoped 50-nm-thick amorphous-Si (a-Si) layer was deposited by low-pressure chemical vapor deposition (LPCVD) at 550 °C. Then, the active islands, including source, drain, and ten nanowire channels were patterned by electron beam lithography (EBL) and transferred by reactive ion etching (RIE). After defining the active region, the 50-nm-thick tetra-ethyl-ortho-silicate oxide (TEOS-$SiO_2$) was deposited by LPCVD as the gate insulator. Then, 150-nm-thick undoped poly-Si films were deposited immediately on the gate oxide by LPCVD. The poly-Si layers were patterned by EBL and transferred by RIE to define the gate electrode. After gate formation, a 100-nm-thick TEOS-$SiO_2$ layer as passivation layer was deposited by LPCVD. The poly-Si gate sidewall TEOS-$SiO_2$ was formed as a self-aligned offset spacer with a width of 0.1 $\mu$m, as shown in Fig. 1(b). Then, the MILC seeding window and contact holes were patterned by EBL and transferred by RIE in the same mask process. Then, a thin 10-nm-thick nickel (Ni) layer was deposited by physical vapor deposition (PVD). The MILC crystallization was carried out at 550 °C for 48 h in an $N_2$ ambient. After annealing, the unreacted nickel on passivative TEOS-$SiO_2$ was removed by an $H_2SO_4$ solution at 120 °C for 10 min. Phosphorus ions at a dose of $5 \times 10^{15}$ cm$^{-2}$ were implanted through the passivative

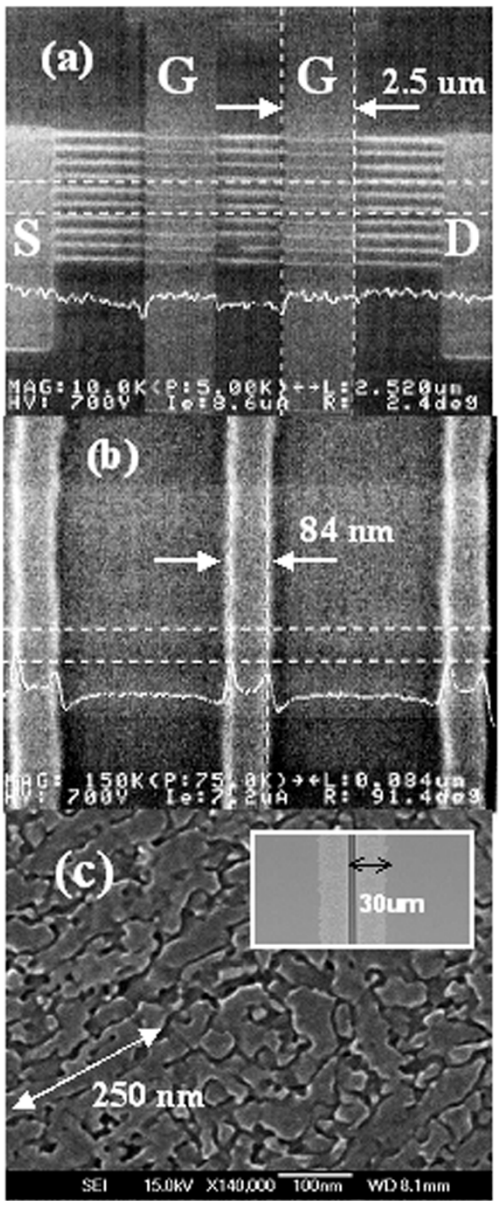


Fig. 3. (a) SEM photograph of the active pattern with the source, drain, ten nanowire channels, and dual-gate structure. (b) SEM photograph of the magnified area of multiple nanowire channels. Each nanowire has a width of 84 nm. (c) SEM photograph of the Ni-MILC poly-Si grain structure. The average poly-Si lateral grain size is approximately 250 nm. The inset optical microscopy photograph depicts an MILC with length of 30 $\mu$m.

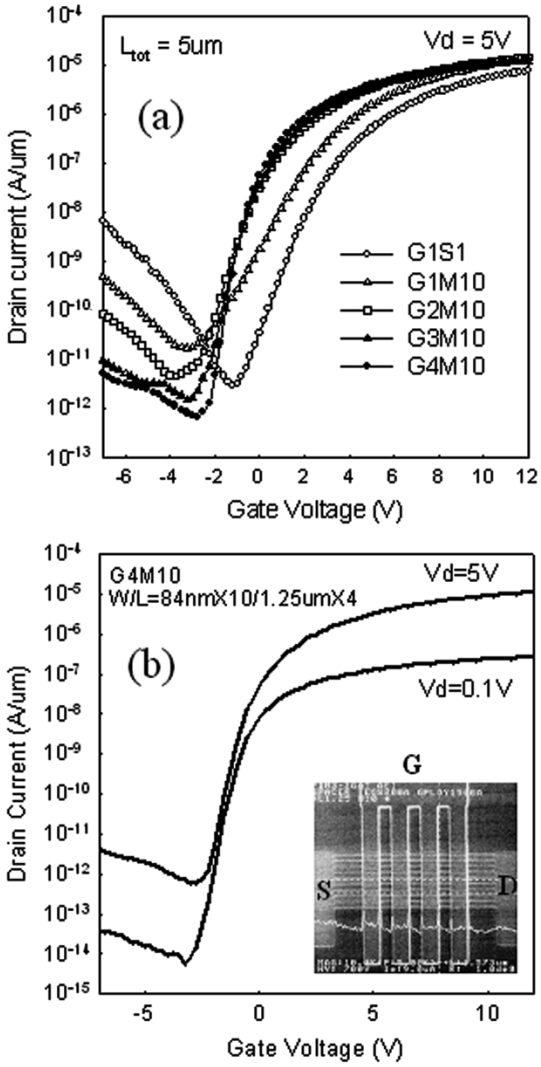


Fig. 4. (a) Comparison of $I_d - V_g$ transfer characteristics of all proposed Ni-MILC poly-Si TFTs with the same device length ($L_{\rm tot}$) of 5 $\mu$m. (b) Transfer curve of G4M10 TFT with linear and saturation regions. The inset SEM photograph shows the G4M10 TFT active region.

TEOS-$SiO_2$ to form the n+ gate, source/drain regions, and the self-aligned offset region in the same process step, as shown in Fig. 1(b). Then, the dopants were activated by rapid thermal annealing (RTA) at 850 °C for 30 s. The 300-nm-thick aluminum (Al) layer was deposited by physical vapor deposition (PVD) and patterned for source, drain, and gate metal pads. In this study, no other H or $NH_3$ plasma passivation was performed. This allowed the intrinsic behavior of the devices to be compared and studied.

## III. Results and Discussion

Fig. 3(a) shows a scanning electron microscopy (SEM) photograph of the G2M10 Ni-MILC TFT active pattern with the source, the drain, ten nanowire channels, and dual-gate structure. Each dual-gate length is 2.5 $\mu$m. Fig. 3(b) shows SEM photographs of the magnified area of multiple nanowire channels. The width of each nanowire is 84 nm. Fig. 3(c) shows SEM photographs of the Ni-MILC poly-Si grain structure. The average poly-Si lateral grain size is approximately 250 nm. The inset optical microscopy photograph depicts an MILC length of 30 $\mu$m, which is longer than 16 $\mu$m [see Fig. 1(a)] to ensure that the whole active channel was crystallized by the MILC process.

Fig. 4(a) compares typical transfer curves of all proposed Ni-MILC poly-Si TFTs. First, comparing the single-gate, the single-channel (G1S1), and the ten-nanowire-channel (G1M10) TFTs reveals that the G1M10 has a higher ON current, a lower leakage current, and a lower threshold voltage than the G1S1 TFT. These data indicate that the multiple-nanowire-channel TFTs have fewer defects at the grain boundaries. For the G1M10 TFT, during the MILC process, its nanowire width of 84 nm strongly limited the growth of poly-Si grains in the $z$-direction [see Fig. 1(a)] than did the single-channel G1S1 TFT. Therefore, the poly-Si grains tended to grow laterally in the $x$-direction, becoming large to reduce the grain boundary defects. In our previous report [8], the poly-Si grain enhancement effect was

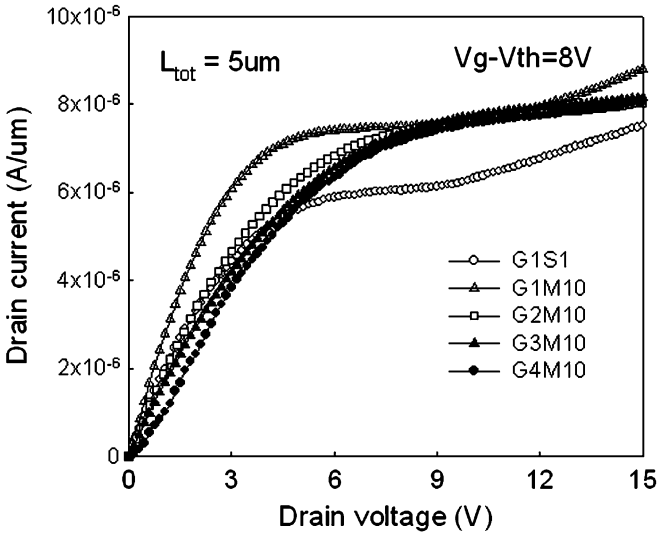


Fig. 5. Comparison of $I_d - V_d$ output characteristics of all proposed Ni-MILC poly-Si TFTs with the same device length $(L_{\rm tot})$ of 5 $\mu$m.

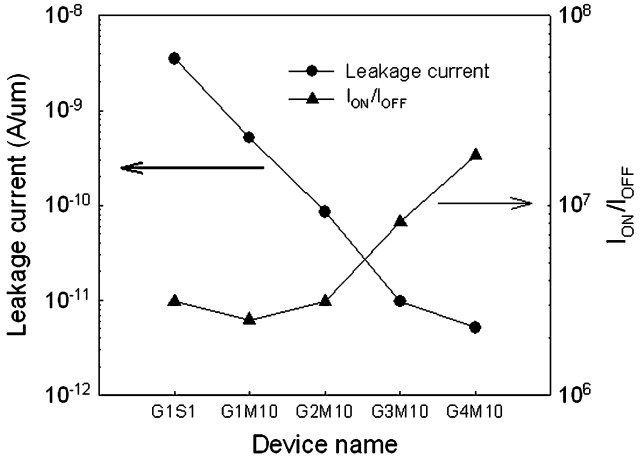


Fig. 6. Leakage current and ON/OFF ratio versus all proposed TFTs, operated in the saturation regime ($V_d = 5$ V).

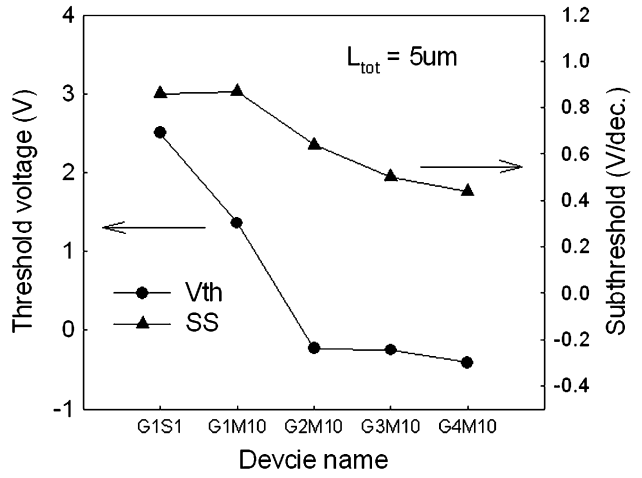


Fig. 7. Threshold voltage and subthreshold swing versus all proposed TFTs, operated in the saturation regime ($V_d = 5$ V).

significant as the channel width was less than the poly-Si grain size. However, both G1S1 and G1M10 exhibit severe leakage current and large subthreshold swing (SS). Second, comparing the single-gate (G1M10) and multigate (G2M10, G3M10, and G4M10) TFTs with the same ten-nanowire-channel Ni-MILC poly-Si TFTs reveals that the electrical performance is significantly improved as the multigate number increases Fig. 4(b) presents the transfer curve of G4M10 TFT with linear and saturation regions. The inset SEM photograph shows the G4M10 TFT active region. The G4M10 outperforms the other TFTs, having a low leakage current, a high ON/OFF ratio $(>10^7)$, a low $V_{\rm th}$, a steep SS, and near-free drain-induced barrier lowering (DIBL).

Fig. 5 compares the output curves of all proposed Ni-MILC poly-Si TFTs with the same gate length of 5 $\mu$m. The kink effect associated with multigate (i.e., G2M10, G3M10, and G4M10) TFTs is suppressed relative to those of the other TFTs (i.e., G1S1 and G1M10). Accordingly, the multigate structure effectively reduces the lateral electrical field [see Fig. 2(b)], thus reducing the impaction ionization in the active channel of the Ni-MILC poly-Si TFTs.

Fig. 6 presents the leakage current and ON/OFF ratio versus different structure of the Ni-MILC TFTs. The leakage current is defined as the drain current at $V_d = 5$ V and $V_g = -7$ V, and the ON/OFF ratio is defined as the maximum drain current value of $I_{\rm ON}/I_{\rm OFF}$ at $V_d = 5$ V. For a single-gate TFT, nanowire channels (G1M10) can be applied to yield a low leakage current by reducing the number of defects at the poly-Si grain boundaries below the number in a single-channel TFT (G1S1). Additionally, comparing single-gate (G1M10) and multigate (i.e., G2M10, G3M10, and G4M10) TFTs with the same ten-nanowire-channel Ni-MILC poly-Si TFTs reveals that the leakage current decreases and the ON/OFF ratio increases as with the number of multigate increasing. The G4M10 TFT has the lowest leakage current of $5.12\times 10^{-12}$ A and the highest ON/OFF ratio of $1.81 \times 10^7$. These findings reveal that the multigate structure can reduce the peak lateral electrical field in the drain depletion region. Therefore, the leakage current that arises from the field emission of carriers through the poly-Si grain traps and the number of defects associated with Ni contamination was reduced. This finding is consistent with the simulated value of the lateral electrical field of multigate TFTs in Fig. 2(b).

Fig. 7 plots the $V_{\rm th}$ and SS versus the structure of the TFTs. $V_{\rm th}$ is defined as the gate voltage to yield a normalized drain current $Id/(W/L)$ equal to $10^{-7}$ A at $V_d = 5$ V. Comparing the G1S1 and G1M0 TFTs reveals that the ten-nanowire-channel structure has a lower $V_{\rm th}$, indicating that the ten-nanowire-channel structure has fewer defects at the poly-Si grain boundaries than the single-channel structure. Moreover, the multigate structure is associated with an even lower $V_{\rm th}$, and the G4M10 has the lowest $V_{\rm th}$ of $-0.41$ V. The results reveal that the multigate structure exhibits channel-length-shortening effect for easy turn-on of the TFT. The effective channel length $(L_{\rm eff})$ decreases as the number of multigate increases ($L_{\rm eff} = L_{\rm tot} - 2n \times \Delta L$, where $n$ is the number of multigate and $\Delta L$ is the overlap of the source/drain dopant region and the gate. The SS specifies the capacity of the transistor to switch. These results reveal that the SS declines as the number of multigate increases, and the G4M10 has the lowest SS of 0.44 V/dec. For the same channel, the length-shortening effect is responsible for the lowering the SS.

Fig. 8 plots a series of G1M10 TFT transfer curves after various hot-carrier stress conditions with 1000 second. Until the extreme hot-carrier stress conditions of $V_d = 45$ V and $V_g =$

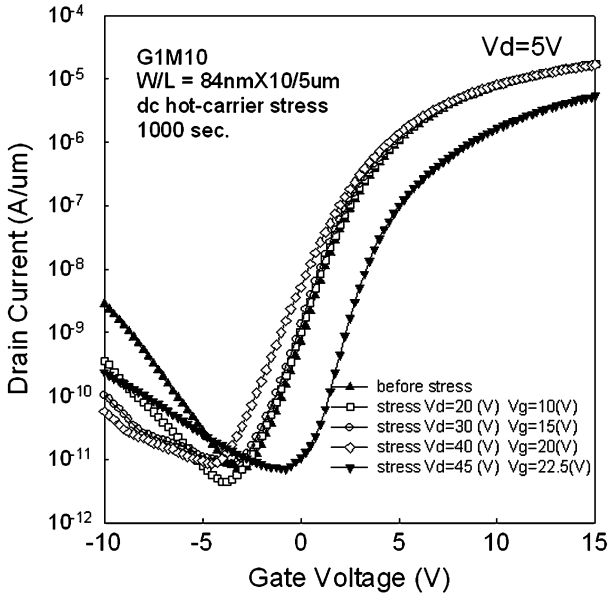


Fig. 8. Series of G1M10 TFT transfer curves after different hot-carrier stress condition with a 1000-s duration.

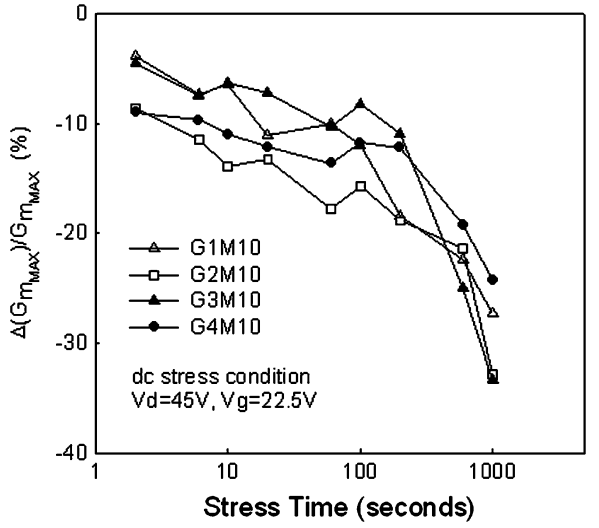


Fig. 9. Maximum transconductance $G_m$ degradation versus dc hot-carrier time with all ten-nanowire-channel TFTs, extracted in the saturation regime ($V_d = 5$ V).

22.5 V are reached; only the transfer curve of G1M10 TFT shows degradation. The results indicate that the ten-nanowire-channel structure of the Ni-MILC TFT supports excellent hot-carrier immunity and potential use in high-voltage applications. The similar hot-carrier stress results are also found in other multigate Ni-MILC TFTs with ten nanowire channels. Fig. 9 plots the maximum transconductance $(G_m)$ degradation with dc hot-carrier time of all ten-nanowire TFTs. These results reveal that the all Ni-MILC TFTs with ten nanowires have similar $G_m$ degradation. However, the G4M10 still has lighter $G_m$ degradation than other TFTs due to its lowest lateral electrical field. Fig. 10 plots the ON/OFF ratio degradation with dc hot-carrier time of all ten-nanowire TFTs. These results reveal that the degradation of ON/OFF ratio improves with the gate number increasing. Again, the multigate structure can reduce the peak lateral electrical field, which is responsible for this degradation of the ON/OFF-ratio improvement. In brief, combining the

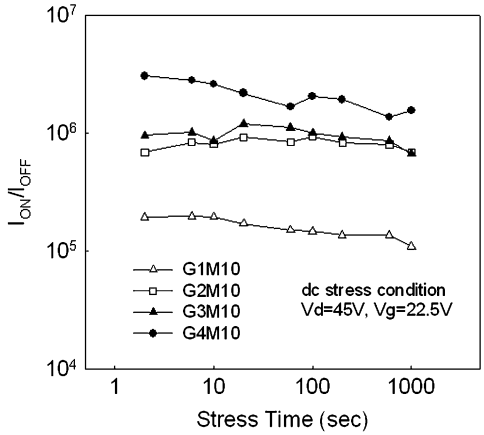


Fig. 10. ON/OFF ratio versus dc hot-carrier time with all ten-nanowire-channel TFTs, extracted in the saturation regime ($V_d = 5$ V).

multigate structure and ten nanowire channels can effectively enhance the entire performance of Ni-MILC TFTs. Obviously, the device performance can be further improved by declining the gate length before the short-channel effect occurrence. However, according to this study, the multigate number is properly within 2 to 4 because, the more gate number increases, the more additional parasitic resistance will be generated between each gate. The additional parasitic resistance will reduce the device performance.

## IV. Conclusion

Experimental results show that applying ten nanowire channels enhances the performance of Ni-MILC poly-Si TFTs because the nanowire shape increases the poly-Si lateral length to reduce the number of defects at the poly-Si grain boundaries. Moreover, combining the multigate structure can effectively reduce the lateral electrical field while further enhancing the TFT performance, including a lower leakage current, a higher ON/OFF ratio, a lower $V_{\rm th}$, and a lower SS than for a single-gate TFT. In output characteristics, the multigate with a ten-nanowire TFT can reduce the kink effect. These novel multichannel and multigate Ni-MILC poly-Si TFTs involve no additional processes, making them highly suitable for high-performance MILC poly-Si TFT applications.

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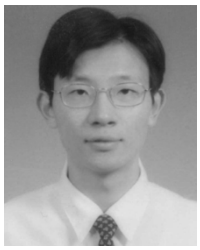

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