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Performance and potential of germanium on insulator field-effect transistors

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The performance of field-effect transistors may be improved by increasing the channel mobility. Strained Si can accomplish this but Ge is another option. Here we show data for germanium-on-insulator (GOI) devices and also describe the simple bonding process which was used in the device fabrication. The GOI devices show better mobilities than their Si counterparts. We also show data for some metal-gate/high-κ dielectric devices on a GOI layer fabricated on a processed Si wafer. Here the GOI structure and processing does not alter the underlying Si devices and yet gives devices whose mobilities exceed those of Si devices. Simulations support the view that the improved performance results from the mobility enhancement and that the performance should also hold for submicron devices. © *2006 American Vacuum Society.* [DOI: 10.1116/1.2167978]

I. INTRODUCTION

Early transistors used germanium but they were soon overtaken by those based on silicon. Now, as scaling of silicon devices progresses into the sub-100 nm regime, issues related to the degradation of the drive current and power consumption are significant. The performance of the silicon devices can be improved by increasing the channel mobility—this may be accomplished with strained silicon.[1] Germanium field-effect transistors (FETs) by themselves are promising devices but conventional FETs on Ge have only recently[2] been demonstrated. However, germanium-on-insulator[3] (GOI) devices offer high mobilities, and their low process temperature means that they are compatible with metal-gate and high-κ dielectrics, technologies now being incorporated into Si technology. GOI devices have been demonstrated by wafer bonding[3,4] and other approaches.[5–7] They may also be integrated on top of silicon devices to create a three-dimensional structure which can help address the power consumption issue.[8]

In this article we describe the fabrication process for these devices, results for GOI devices where the underlying substrate is Si and a processed Si wafer, and estimate the performance of submicron device using simulations. Some of the challenges associated with Ge will also be discussed. Simulations confirm that the improved performance results from the enhanced mobility.

II. EXPERIMENTAL DETAILS

Before fabricating devices the GOI bonding process had to be performed. Using chemical-vapor deposition 80 nm SiO_2 was deposited on Ge and Si wafers, then the GOI wafer was formed by bonding the SiO_2/Ge and SiO_2/Si at 500 °C for 10 h. The process is restricted by the low melting temperature of Ge (938 °C), which is more difficult than high-temperature (~1000 °C) thermally bonded silicon on insulator (SOI). To enhance the bonding at such low temperatures, an O_2 plasma treatment was needed to activate the SiO_2 surface before bonding[3] and a constant pressure was applied during the bonding. The steps are shown schematically in Fig. 1(a). A transmission electron microscopy (TEM) cross-sectional micrograph of the bonded wafers [Fig. 1(b)] shows the bonded interface clearly. After an etch-back process, 400 nm SiO_2 was deposited on the top Ge for isolation. Then the p^+ source and drain were formed by a B^+ implant and followed by a 500 °C furnace anneal. The Al_2O_3 gate dielectric was formed on the Ge surface and followed by 400 °C annealing. To reduce gate depletion, an Al gate was used. For comparison, Al_2O_3/Si *p*-type metal-oxide-semiconductor field-effect transistors (*p*-MOSFETs) were also fabricated on Si.

We also fabricated devices on a wafer which had been processed in a foundry using a single-poly/6-metal (1P6M) process. In this case a similar device fabrication process was followed—the aim here was to examine the effects of the GOI process on the underlying devices on the Si. The process details followed those described by Yu *et al.*[3]

III. RESULTS AND DISCUSSION

In Fig. 2 we show a comparison of the drain characteristics of 10 μm gate length *p*-FETs made on a GOI wafer with those on a standard Si wafer. Not only does the GOI device have better turn-on behavior but the saturated currents are higher for the same bias. The *C-V* characteristics of the Al_2O_3 gate dielectric on GOI and Si gave a κ value of 9 and equivalent oxide thickness of 1.7 nm. These data lead to an estimate of the hole mobility, shown in Fig. 3, which shows that the GOI device is not only better than the Si-based de-

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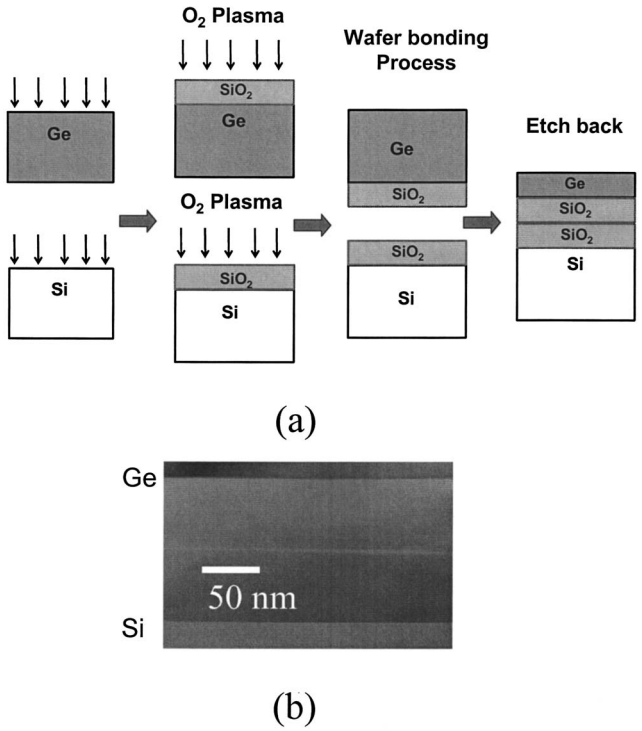

FIG. 1. (a) Schematic diagram of the process used to create the GOI wafers. (b) TEM cross section of a GOI wafer showing the two semiconductor layers and the SiO_2 oxide layers and bonded interface.

vice but that the mobility exceeds the universal hole mobility. The reason for this is unclear. It is possible that the process produced some strain in the Ge channel which would help improve the mobility.

The GOI devices were fabricated using processes compatible with those commonly used in Si technology. This suggests that they can be fabricated on preprocessed Si wafers to create high performance devices on top of devices made using a standard Si process. In Fig. 4 we show drain *I-V* characteristics for the underlying Si FETs, before and after the thermal treatment associated with fabricating the GOI devices. There is essentially no change in the characteristics. This observation ensures that the GOI process for devices fabricated on top of the Si wafer does not lead to degradation of the performance of the Si devices underneath. In this way high performance GOI devices can be integrated into Si technology. There are a few advantages to this—one important advantage is that one can effectively create a three-dimensional structure, reducing the average length of the interconnects. This potentially helps address an important looming issue in Si technology—that of power dissipation and delay in the increasingly dense interconnects in circuits which operate at increasingly high frequencies.

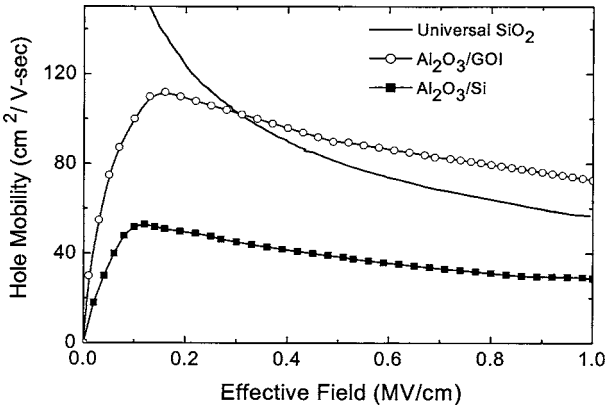

FIG. 3. Hole mobility derived from the dc data for devices of Fig. 2.

In Fig. 5 we show the drain characteristics for *n*- and *p*-FETs fabricated on the GOI structure over Si and on Si. Here the devices had high-κ $LaAlO_3$ as the gate dielectric, which was deposited from a κ=25.1 $LaAlO_3$ source, and IrO_2 or IrO_2–Hf gates. The devices were fabricated on ⟨110⟩ Ge, along with reference devices on ⟨110⟩ Si. For comparison purposes only two gate-bias characteristics are shown. In both *n*- and *p*-type devices the GOI devices show better dc currents and better turn-on features. This is due to the improvements in the mobility that the Ge provides. In Fig. 6 the derived hole mobilities are displayed for the ⟨110⟩ GOI and Si data of Fig. 5 and also for ⟨100⟩ GOI devices. The GOI

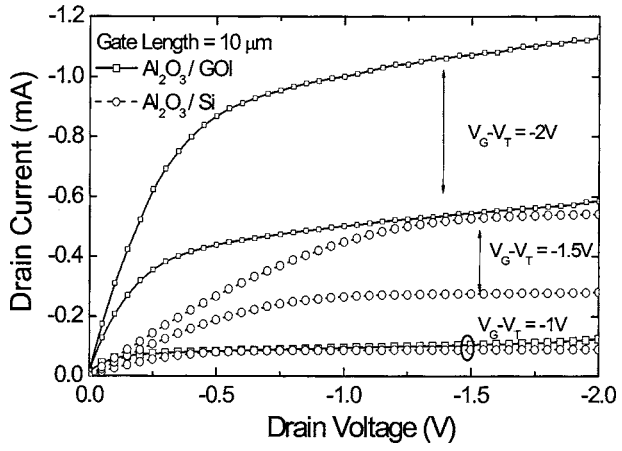

FIG. 2. Comparison of the I_D-V_D drain characteristics for GOI and Si *p*-FET devices, where Al_2O_3 was used as the gate dielectric.

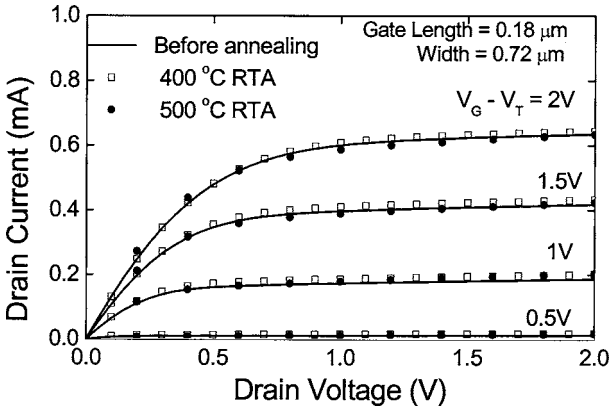

FIG. 4. Drain characteristics (I_D-V_D) for 0.18 mm Si devices before and after being subjected to the thermal budget associated with the GOI device fabrication. Almost no change is shown in the characteristics.

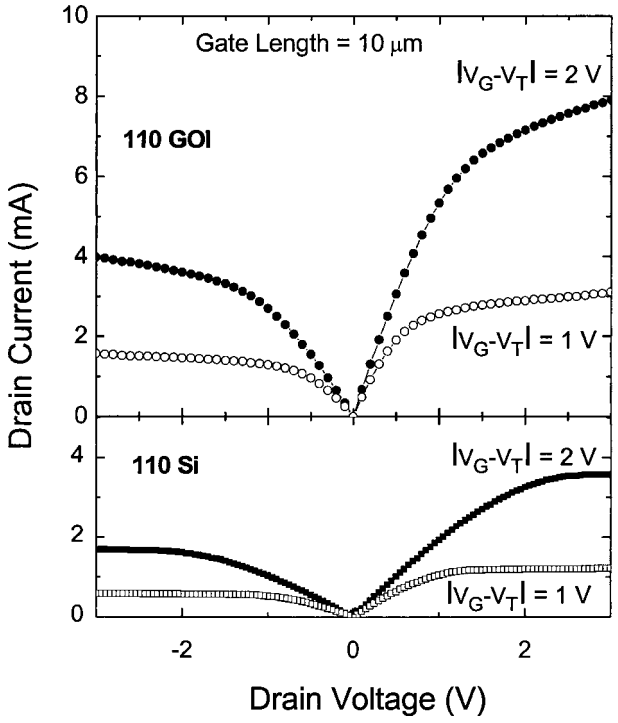

FIG. 5. I_D-V_D drain characteristics for $IrO_2(Hf)/LaAlO_3$ p- and n-FETs on ⟨110⟩ GOI and ⟨110⟩ Si wafers.

devices show mobilities exceeding those of reference Si devices and the universal mobility curve, for nearly the complete range of effective electric fields.

The peak electron and hole mobilities of 203 and 67 $cm^2/V\,s$ in $IrO_2(Hf)/LaAlO_3/Si$ complementary metal-oxide semiconductor (CMOS) are comparable with the best metal-gate/HfO_2/Si data.[9] The good hole mobility may result from the good match of both the gate oxide and high-κ oxide, and that it is an excellent metal- and O_2-diffusion barrier. For the $IrO_2(Hf)/LaAlO_3$ GOI devices fabricated above Si devices, the peak electron and hole mobilities were 389 and 234 $cm^2/V\,s$. These values are close to the universal electron mobility and 2.5 times higher than the universal hole mobility at 1 MV/cm effective field.

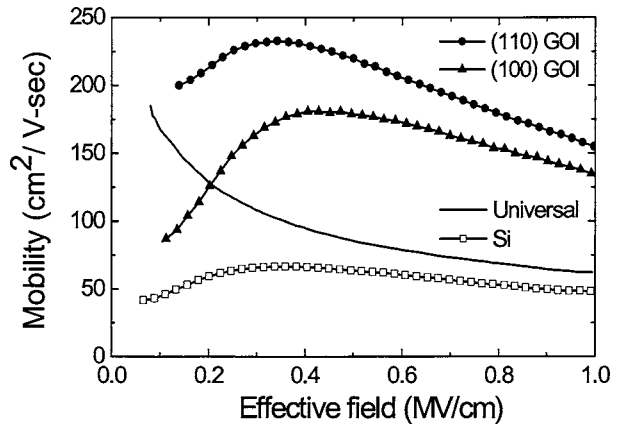

FIG. 6. Hole mobility derived from the dc data for the $IrO_2(Hf)/LaAlO_3$ devices of Fig. 5.

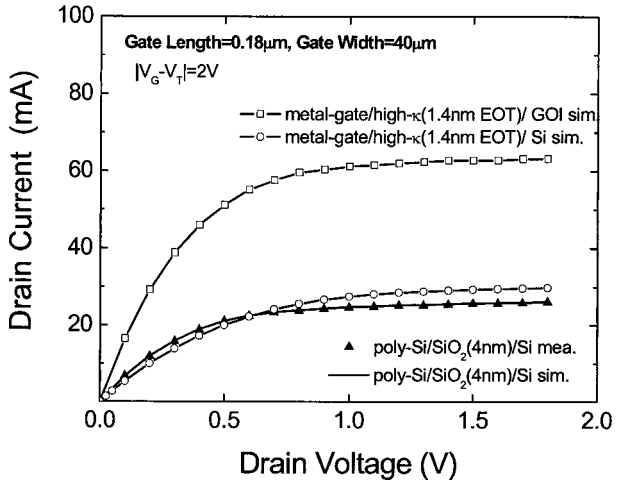

FIG. 7. Simulated I_D-V_D drain characteristics for 0.18 μm metal-gate/high-κ GOI and Si n-FETs, compared with standard Si devices.

The FETs, discussed above, are long-channel devices. Simulating GOI devices with short channel lengths is important to see whether the improvements over standard devices hold, and also for predicting the device rf performance. To accomplish this we first calibrated T-Supreme and Medici simulators with results for standard multifingered 0.18 m Si MOSFETs, obtained from a foundry. The dc characteristics of the long-channel metal-gate/high-κ/GOI MOSFETs, such as those in Fig. 5, were simulated. This produced a good match of the measured and simulated mobility data in the medium to high effective field region, confirming that the improved performance of the GOI devices arises from the mobility enhancement. After achieving a good match with the large devices we then simulated scaled 0.18 μm metal-gate/high-κ/GOI MOSFETs. These results are shown in Fig. 7. They suggest that the scaled GOI devices should show better performance than both Si/SiO_2 and metal-gate/high-κ Si devices. Of added interest is the rf performance, as represented by figures of merit such as f_T and the minimum noise figure. The GOI devices are also better in this case, but a detailed discussion of this work is beyond the scope of the current work and will be discussed elsewhere.[10]

One issue of concern is the leakage current below cut-off. For instance, we found that it can be only three to four orders of magnitude less than the maximum drain current—this is much worse than for Si devices. This is not unexpected and arises, as can be confirmed by simulations, from the small E_G of Ge, especially in the drain junction depletion region. The suppression of the leakage current can be achieved by using ultrathin body (UTB) GOI (Ref. 11) similar to Si MOSFETs in the UTB SOI case. In addition, proper device design can reduce the off-state leakage current by more than an order of magnitude from that obtained from the Medici simulations.

The potential of GOI is not just as electronic devices where they offer mobilities that are better than those in Si but

also as photodetectors.[12] They should be useful in optical interconnects where their bandwidth, speed, and efficiency all exceed those of Si-based detectors.[12] As has been emphasized here the fabrication of these devices is compatible with Si technology, since it is a low thermal budget process. An obvious drawback of these photodetectors, as with their electronic counterparts, is the magnitude of the band gap which leads to a dark current greater than desired, in the same way that it poses a challenge for the FET leakage current.

IV. CONCLUSIONS

We have fabricated germanium-on-insulator devices and shown that they show dc characteristics better then those of reference Si devices. The improvements result from the improved mobilites in Ge. However, because Ge has a smaller band gap than Si, the leakage current is not as good as standard Si devices. The GOI devices can be integrated onto other structures, such as a processed Si wafer, without altering the underlying Si device characteristics. This creates an integrated three-dimensional (3D) structure of active devices. By using simulations we have shown that submicron devices should also show the improved characteristics.

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