Design of ESD Protection Diodes With Embedded SCR for Differential LNA in a 65-nm CMOS Process

Chun-Yu Lin, *Member, IEEE*, and Mei-Lian Fan

***Abstract*—The pin-to-pin electrostatic discharge (ESD) issue for a differential low-noise amplifier (LNA) was studied in this work. A new design of ESD protection diodes with an embedded silicon-controlled rectifier (SCR) was proposed to protect the gigahertz differential LNA. The proposed ESD protection design was modified from the conventional ESD protection design without adding any extra device. The SCR path was established directly from one differential input pad to the other differential input pad so the pin-to-pin ESD robustness can be improved. This design had been verified in a 65-nm CMOS process. Besides, this design had been further applied to a 24-GHz LNA in the same 65-nm CMOS process. Experimental results had shown that the proposed ESD protection design for the differential LNA can achieve excellent ESD robustness and good RF performances.**

***Index Terms*—Differential low-noise amplifier (LNA), diode, electrostatic discharge (ESD), RF, silicon-controlled rectifier (SCR).**

I. Introduction

NANOSCALE CMOS technologies have been used to implement RF integrated circuits (ICs) with the advantages of scaling-down feature size, low power consumption, high integration capability, improving high-frequency characteristics, and low cost for mass production [1]. In an RF receiver, the low-noise amplifier (LNA) plays an important role because it is the first stage in the RF receiver. A differential configuration is used for LNA design because the advantages of common-mode noise rejection, less sensitivity to substrate noise, supply noise, and bond-wire inductance variation [2]–[4]. In addition, the differential output signals of the differential LNA can be directly connected to the differential inputs of the double balanced mixer [5].

The RF circuits realized in CMOS technologies are susceptible to electrostatic discharge (ESD) events, which may damage the IC products [6]. The LNA is usually connected to the external of the RF receiver chip. Therefore, on-chip ESD protection circuits must be added at the first stage of the RF receiver.

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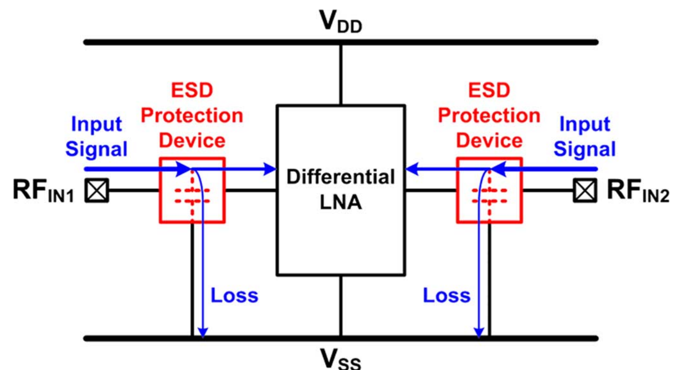

Fig. 1. Differential LNA with ESD protection devices.

As shown in Fig. 1, the ESD protection circuits are added to the input pads of the differential LNA ($\mathrm{RF_{IN1}}$ and $\mathrm{RF_{IN2}}$) against ESD damages. Several ESD protection designs have been reported for the RF LNA [7]–[12], including the differential LNA. Parasitic capacitance of the ESD protection device is one of the most important design considerations for a gigahertz differential LNA. A typical specification for a gigahertz RF circuit on human-body-model (HBM) ESD robustness and the maximum parasitic capacitance of the ESD protection device are 2 kV and 200 fF, respectively [13], [14]. If we consider the type of circuit designed, frequency of operation, quality factor, and acceptable reflection coefficient for the circuit, the parasitic capacitance may be more strictly limited.

In the ESD-test standards, there are several ESD-test pin combinations. Besides the positive-to-V_{DD} (PD), positive-to-V_{SS} (PS), negative-to-V_{DD} (ND), and negative-to-V_{SS} (NS) ESD tests, the pin-to-pin ESD test is also specified to evaluate ESD robustness of the differential input pads. Under the pin-to-pin ESD test, one input pad is stressed with the other input pad relatively grounded, while all the other pads including all V_{DD} and V_{SS} pads are floating [15]. The conventional ESD protection design with dual diodes has been generally used for gigahertz differential LNAs [3], as shown in Fig. 2(a). Under pin1-to-pin2 ESD stresses, the ESD current will be discharged through the D_{P1}, V_{DD} bus, power-rail ESD clamp circuit, V_{SS} bus, and D_{N2}. The pin-to-pin ESD stress was the most critical ESD event for the differential input pads since the pin-to-pin ESD current path is longer than PD, PS, ND, or NS ESD current paths. To adapt some applications, the ESD protection design with stacked diodes has also been used [16], as shown in Fig. 2(b). The optimization on layout style of stacked diodes has been studied to achieve lower turn-on resistance, lower parasitic capacitance, and higher ESD robustness [17]. However,

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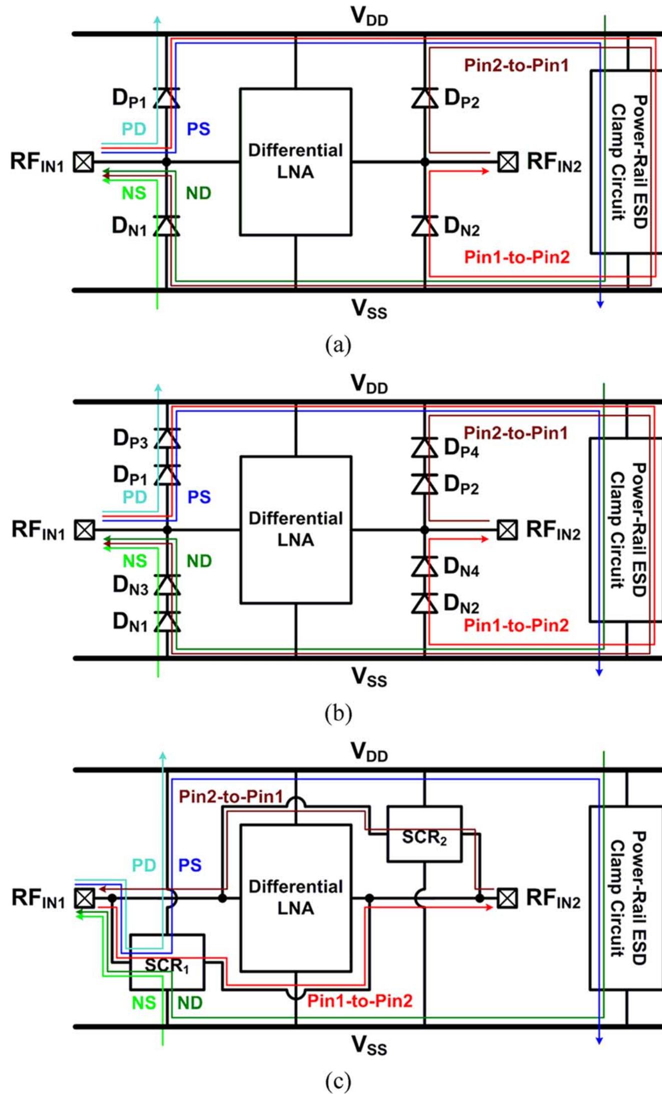

Fig. 2. Differential LNA with conventional ESD protection design of: (a) dual diodes, (b) stacked diodes, and (c) cross-coupled SCR.

the pin-to-pin ESD stress was still critical in the ESD protection design with stacked diodes. The silicon-controlled rectifier (SCR) has been reported to be useful for ESD protection with low parasitic capacitance, fast enough turn-on speed, and high ESD robustness [18]. The ESD protection design with a dual SCR has been presented to improve the pin-to-pin ESD robustness [7] because the clamping voltage of the SCR is much lower than that of the diode under ESD stress. To further reduce the voltage drop under pin-to-pin ESD stress, the ESD protection design with a cross-coupled SCR has been presented [8], as shown in Fig. 2(c). Under pin-to-pin ESD stresses, the ESD current will be discharged through SCR_1 or SCR_2. In this design, the trigger circuit of the SCR is needed to enhance the turn-on speed of the SCR under ESD stress. The cross-coupled SCR and power-rail ESD clamp circuit need to be co-designed; therefore, this ESD protection design may be hard for an RF circuit designer to apply ESD protection in the gigahertz differential LNA.

In this work, a novel ESD protection design by using ESD protection diodes with an embedded SCR is proposed for effective ESD protection in the gigahertz differential LNA. All

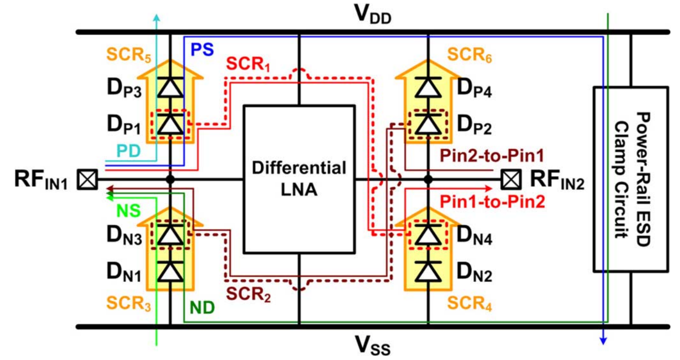

Fig. 3. Proposed ESD protection design.

the components used in the proposed design are embedded in a compact cell. The proposed ESD protection design in this paper is suitable for an RF circuit designer in order for them to easily apply ESD protection in the gigahertz differential LNA.

II. Proposed ESD Protection Design

The new proposed ESD protection design utilizes stacked diodes with an embedded SCR, as shown in Fig. 3. Similar to the ESD protection design with stacked diodes in Fig. 2(b), eight diodes are used in the proposed design. Without adding an extra device, the proposed design combines P+/N-well diodes ($D_{\mathrm{P1}}, D_{\mathrm{P2}}, D_{\mathrm{N1}}$, and D_{N2}) and P-well/N+ diodes ($D_{\mathrm{P3}}, D_{\mathrm{P4}}, D_{\mathrm{N3}}$, and D_{N4}) to form the embedded P+/N-well/P-well/N+ SCR paths ($\mathrm{SCR}_3, \mathrm{SCR}_4, \mathrm{SCR}_5$, and SCR_6) by using layout skill. Besides, by putting D_{P1} and D_{N4} (D_{P2} and D_{N3}) together in the layout, another embedded SCR_1 (SCR_2) exists. To implement this design, the layout top view and the device cross-sectional view of the proposed ESD protection design are shown in Figs. 4 and 5. The ESD current paths along the A–A' direction include $D_{\mathrm{P3}}, D_{\mathrm{P1}}, D_{\mathrm{N4}}, D_{\mathrm{N2}}$, and the parasitic stacked diodes from $\mathrm{RF}_{\mathrm{IN1}}$ to $\mathrm{RF}_{\mathrm{IN2}}$. The ESD current paths along the B–B' direction include $\mathrm{SCR}_5, \mathrm{SCR}_1$, and SCR_4. Similarly, the ESD current paths along the C–C' direction include $D_{\mathrm{N1}}, D_{\mathrm{N3}}, D_{\mathrm{P2}}, D_{\mathrm{P4}}$, and the parasitic stacked diodes from $\mathrm{RF}_{\mathrm{IN2}}$ to $\mathrm{RF}_{\mathrm{IN1}}$, and those along the D–D' direction include $\mathrm{SCR}_3, \mathrm{SCR}_2$, and SCR_6.

The width of diode path (T) is equal to twice the width of t in Fig. 4, and the width of the SCR path (W) is the sum of all segments of w_1 and w_2. In the beginning of the ESD stress, the diode paths will turn on to discharge the initial currents and then the SCR paths will take over to discharge the primary currents. The diode path also plays the role of the trigger circuit of the SCR device to enhance its turn-on speed [19], [20]. Since the primary ESD currents are designed to be discharged through the SCR paths, the distance from anode to cathode of the SCR (D) is wished to be minimized. The turn-on resistance of the SCR can be lowered by using this layout style.

As PD ESD stress on the $\mathrm{RF}_{\mathrm{IN1}}$ pad, the ESD current will be discharged by the forward-biased stacked diodes (D_{P1} and D_{P3}) with embedded SCR_5. During PS ESD stress on the $\mathrm{RF}_{\mathrm{IN1}}$ pad, the ESD current will be discharged through D_{P1} and D_{P3} with embedded SCR_5 and the power-rail ESD clamp circuit. As NS ESD stress on the $\mathrm{RF}_{\mathrm{IN1}}$ pad, the ESD current will be discharged by D_{N1} and D_{N3} with embedded SCR_3.

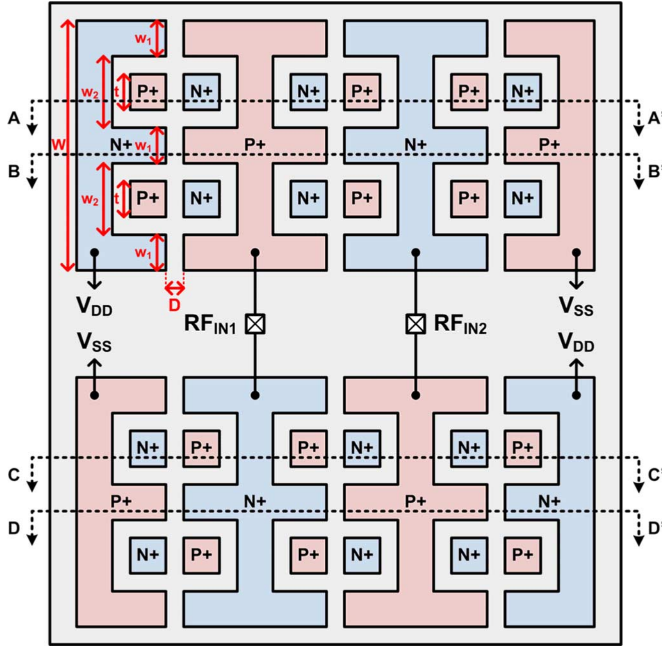

Fig. 4. Layout top view of proposed ESD protection design.

During ND ESD stress on the $\mathrm{RF_{IN1}}$ pad, the ESD current will be discharged through the power-rail ESD clamp circuit and D_{N1} and D_{N3} with embedded $\mathrm{SCR_3}$. As pin-to-pin ESD stress from $\mathrm{RF_{IN1}}$ to $\mathrm{RF_{IN2}}$ (pin1-to-pin2), the ESD current can be discharged by the parasitic stacked diodes with embedded $\mathrm{SCR_1}$. During pin-to-pin ESD stress from $\mathrm{RF_{IN2}}$ to $\mathrm{RF_{IN1}}$ (pin2-to-pin1), the ESD current can be discharged by the other parasitic stacked diodes with embedded $\mathrm{SCR_2}$. Compared with the conventional ESD protection designs, the proposed ESD protection design provides the whole chip ESD protection for all ESD-test pin combinations with the lowest clamping voltage. Therefore, the proposed ESD protection design is expected to have better ESD robustness.

To verify the proposed design in a silicon chip, a 65-nm CMOS process is used in this work. The width of the SCR path (W) is selected to be 40 μm, which is estimated to pass 2-kV HBM ESD tests. The widths of the diode path (T) are selected to be $W/2, W/4$, or $W/8$. The distance from anode to cathode of SCR (D) is 0.32 μm. For comparison purposes, the ESD protection designs with dual diodes and stacked diodes are also implemented in the same 65-nm CMOS process. In each test circuit, the dimensions of diodes and power-rail ESD protection circuits are all identical. All these dimensions of test circuits are listed in Table I. These test circuits are arranged with a four-port ground–signal–ground–signal–ground (G–S–G–S–G) style in the layout to facilitate the on-wafer RF measurement.

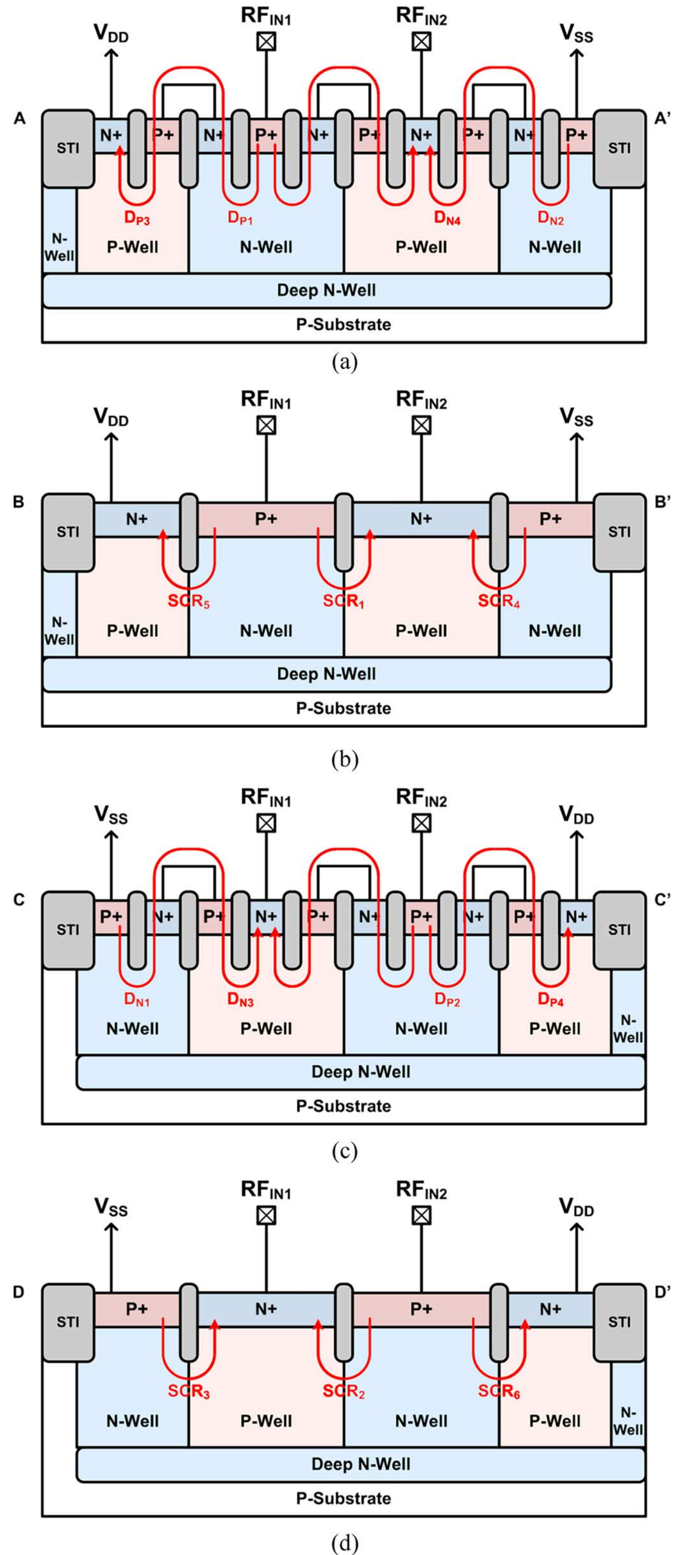

Fig. 5. Cross-sectional view of proposed ESD protection design along: (a)A–A', (b) B–B', (c) C–C', and (d) D–D'.

III. Experimental Results of Test Circuit

A. Parasitic Capacitance and Insertion Loss

With the on-wafer measurement, the four-port S-parameters of the test circuits were measured by using the vector network analyzer. The source and load resistances to the test circuits are kept at 50 Ω. The parasitic capacitance can be extracted from the S-parameters. In order to extract the intrinsic characteristics of the test circuits in high frequencies, the parasitic effects of the G–S–G–S–G pads have been removed by using the de-embedding technique.

TABLE I
DESIGN PARAMETERS AND MEASUREMENT RESULTS OF TEST CIRCUITS

Structure	W (μm)	T (μm)	D (μm)	C @ 24 GHz (fF)	PD HBM (kV)	PS HBM (kV)	ND HBM (kV)	NS HBM (kV)	Pin-to-Pin HBM (kV)	Pin-to-Pin TLP V_{t1} (V)	Pin-to-Pin TLP V_{hoid} (V)	Pin-to-Pin TLP I_{CP} (A)
Proposed Design	40	5	0.32	121.5	3 3 3.25	3 3 3	3 3 3	3 3 3	2.75 2.75 2.75	1.3	1.1	1.1
		10		120.6	2.5 2.5 2.75	2.75 2.75 2.75	2.5 2.5 2.75	2.5 2.5 2.5	2.5 2.5 2.5	1.3	1.2	1.0
		20		113.6	2.25 2.25 2.5	2.25 2.5 2.5	2.25 2.25 2.25	2.25 2.25 2.25	2 2.25 2.25	1.6	1.4	1.0
Dual Diodes	40	N/A	N/A	122.9	2 2 2.25	2 2 2.25	2 2 2	2 2 2	1.75 1.75 2	2.0	2.4	0.8
Stacked Diodes	40	N/A	N/A	83.4	2.5 2.25 2.5	2 2 2.5	2 2 2.5	2 2 2	1.75 2 2	2.8	4.5	0.9

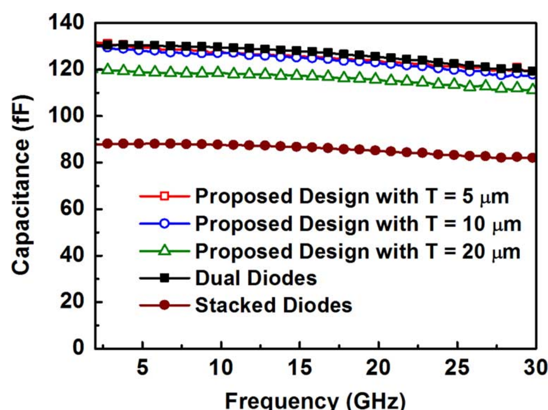

Fig. 6. Measured parasitic capacitances of test circuits.

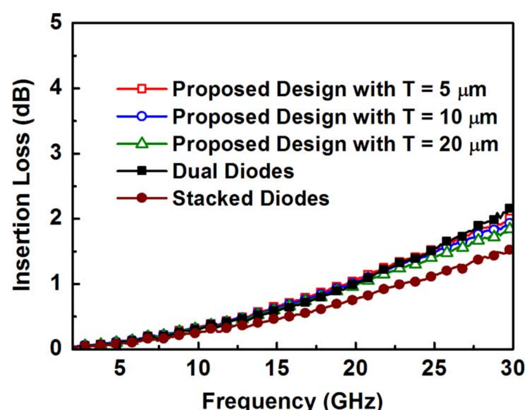

Fig. 7. Measured insertion losses of test circuits.

Fig. 6 shows the extracted parasitic capacitances seen at $\mathrm{RF_{IN1}}$ or $\mathrm{RF_{IN2}}$ of the test circuits from 1 to 30 GHz. With the narrower T, which is identical to the narrowed w_2 and the widened w_1, the parasitic capacitances are slightly increased. The parasitic capacitance of the proposed design is lower than 200 fF, and the proposed ESD protection design is expected to have much better ESD robustness.

The extracted insertion losses seen at $\mathrm{RF_{IN1}}$ or $\mathrm{RF_{IN2}}$ of the test circuits from 1 to 30 GHz are shown in Fig. 7. At 24 GHz, the insertion loss of the proposed design with $W = 40$ μm and $T = 5$ μm/10 μm/20 μm is 1.43 dB/1.38 dB/1.31 dB, and those of the dual-diode and stacked-diode ESD protection are 1.41 and 1.05 dB, respectively.

B. Leakage Current

The standby leakage currents from V_{DD} to V_{SS} of the test circuits, including the power-rail ESD clamp circuit, under 1.2-V bias are measured. At 25 °C, the leakage current of the proposed design with $W = 40$ μm and $T = 5$ μm/10 μm/20 μm is 4.39 μA/4.32 μA/4.31 μA, while those of the dual-diode and stacked-diode ESD protection are 4.31 and 4.34 μA, respectively. As the temperature increased to 100 °C, the leakage current of the proposed design with $W = 40$ μm and $T = 5$ μm/10 μm/20 μm is 15.34 μA/15.32 μA/15.23 μA, while those of the dual-diode and stacked-diode ESD protection are 15.15 and 15.58 μA, respectively. The proposed ESD protection design has almost the same leakage current as the dual-diode and stacked-diode ESD protection.

C. ESD Robustness

The HBM ESD robustness of the test circuits have been evaluated by the ESD tester. The HBM ESD pulses are stressed to each test circuit under PD, PS, ND, NS, and pin-to-pin ESD stress conditions. The failure criterion is defined as the *I–V* curve seen between test pads shifting over 30% from its original curve after ESD stressed at every ESD test level. All ESD robustness of the test circuits are measured three times (three samples). All these measured ESD robustness are listed in Table I. According to the measurement results, the proposed design with $W = 40$ μm and $T = 5$ μm/10 μm/20 μm can pass the

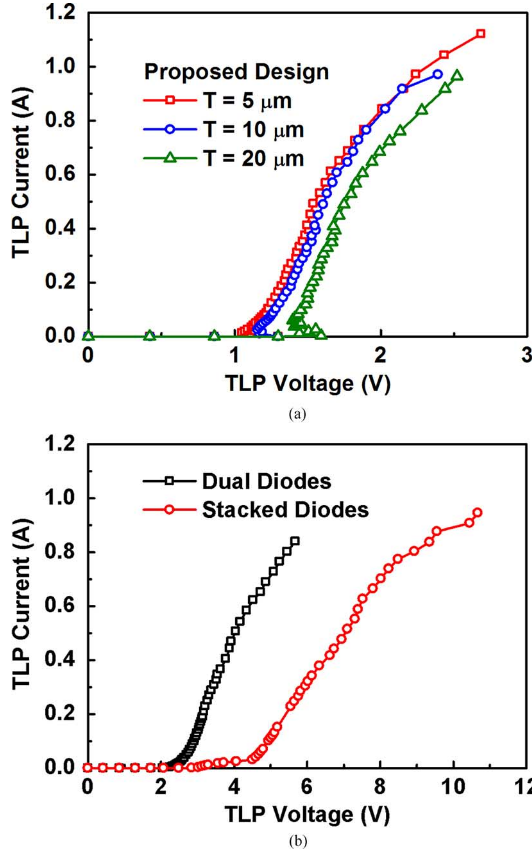

Fig. 8. TLP *I–V* curves of: (a) proposed design and (b) conventional designs under pin-to-pin stress.

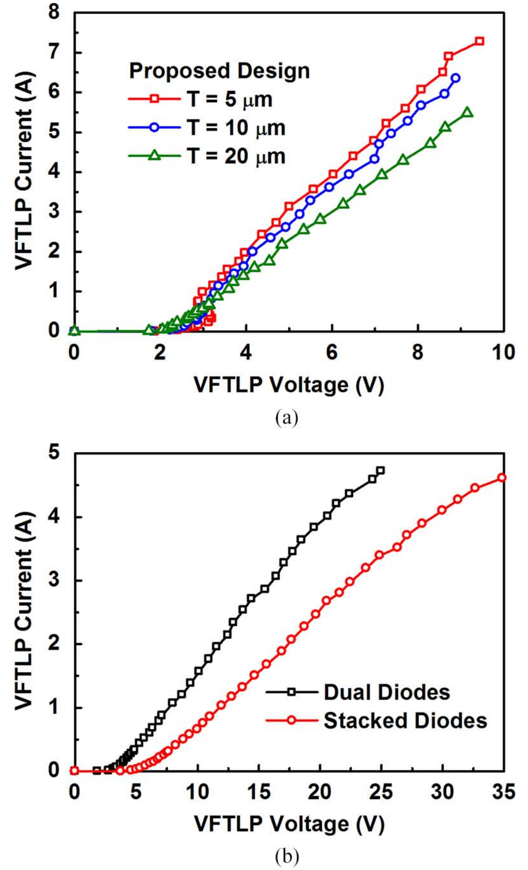

Fig. 9. VFTLP *I–V* curves of: (a) proposed design and (b) conventional designs under pin-to-pin stress.

2.75-kV/2.5-kV/2-kV HBM ESD test, which is obtained from the lowest level of the test results. The dual- or stacked-diode ESD protection with the same $W = 40$ μm can only pass the 1.75-kV HBM ESD test. Even though the test results varied among the samples, the HBM ESD robustness of the proposed design are still higher than those of the dual- and stacked-diode ESD protection.

D. Transmission-Line-Pulsing (TLP) I–V Characteristics

To investigate the turn-on behavior and the *I–V* curve in the high-current region of the ESD protection circuit, the TLP system with 10-ns rise time and 100-ns pulsewidth is used [21]. The TLP-measured *I–V* characteristics of the ESD protection circuit under pin-to-pin stress are shown in Fig. 8. The trigger voltages $(V_{\rm t1})$ of the proposed designs are 1.3–1.6 V, while those of the dual diodes and stacked diodes are 2.0 and 2.8 V, respectively. The holding voltage $(V_{\rm hold})$ of the proposed designs are 1.1–1.4 V, while those of the dual diodes and stacked diodes are 2.4 and 4.5 V, respectively. Besides, the current compression point $(I_{\rm CP})$, which is defined as the current level, deviates from the linearly extrapolated low-current curve by 20% [22] of the test circuits that are also measured. The $I_{\rm CP}$ of the proposed designs are 1.0–1.1 A, while those of the dual diodes and stacked diodes are 0.8 and 0.9 A, respectively. All TLP-measured *I–V* characteristics are listed in Table I. The proposed ESD protection design with lower $V_{\rm t1}$, lower $V_{\rm hold}$, and higher $I_{\rm CP}$ is more suitable for ESD protection. The proposed ESD protection design especially has the lower clamping voltage, and it can provide effective ESD protection on the gigahertz differential LNA.

E. Very Fast Transmisson-Line-Pulsing (VFTLP) I–V Characteristics

Another VFTLP system with 0.2-ns rise time and 1-ns pulsewidth is used to evaluate the ESD protection circuit in faster ESD-transient events. The VFTLP system can be used to capture the transient behavior of the ESD protection circuit in the time domain of the charged-device-model (CDM) ESD event [23]. The VFTLP-measured *I–V* characteristics of the ESD protection circuit under pin-to-pin stress are shown in Fig. 9. The proposed ESD protection design is fast enough to be turned on under such a fast-transient pulse.

IV. Application of Proposed ESD Protection Design to 24-GHz Differential LNA

A. Differential LNA

The differential LNA is designed to operate at 24 GHz with a V_{DD} supply of 1.2 V. The circuit schematic of the reference LNA without ESD protection is shown in Fig. 10. The architecture of common-source inductive degeneration is applied to match the source impedance (50 Ω) at resonance. Using the cascode configuration can achieve good isolation between the input and output. Moreover, the cascode configuration reduces

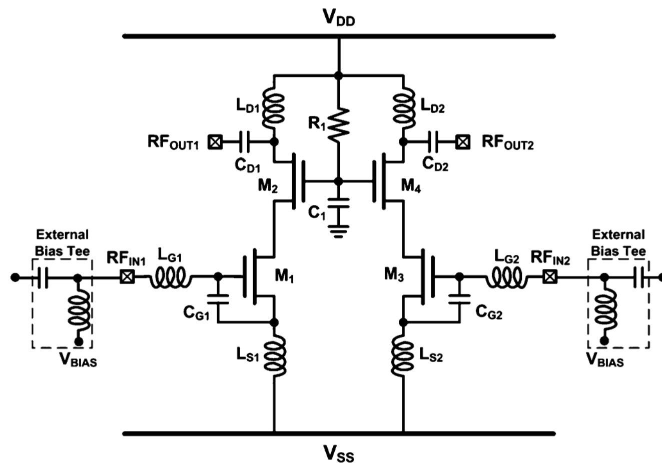

Fig. 10. Differential LNA without ESD protection.

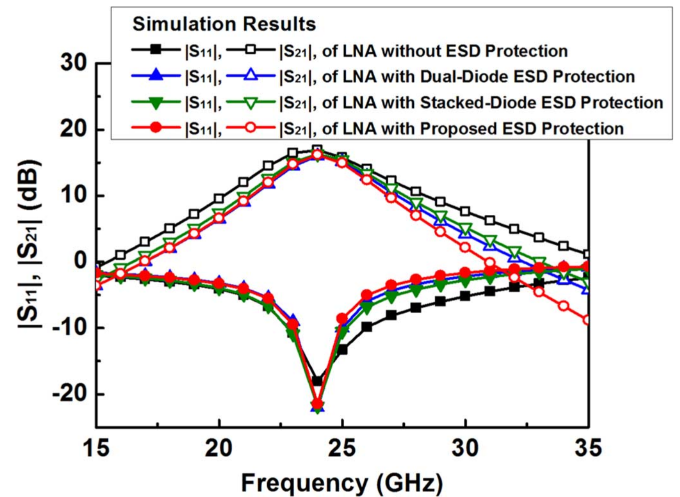

Fig. 11. Simulated $|S_{11}|$ and $|S_{21}|$ of the LNA with and without ESD protection.

the Miller effect and provides good stability. The dimensions of the input nMOS transistors were designed according to the optimization of the noise figure (NF) [24]. The power consumption was also considered simultaneously. With the deep N-well structure, the P-well (bulk) region of each nMOS transistor can be fully isolated from the common P-substrate so the source and bulk terminals are connected together to eliminate the body effect. All of the inductors are the on-chip spiral inductors implemented by the top metal layer. The active and passive devices are fully integrated in the silicon chip in the 65-nm CMOS process.

The RF characteristics of the differential LNA with and without ESD protection are simulated by using the microwave circuit simulator ADS. The LNA have been retuned after adding the ESD protection circuits. Since the device model of the proposed ESD protection design is not available in the given CMOS process, a 200-fF capacitor at each input pad of the differential LNA is used to simulate the proposed ESD protection design. Fig. 11 shows the post-layout simulation results of the differential LNA with and without ESD protection. These LNAs exhibit good input matching ($|S_{11}| < -15$ dB) around 24 GHz. The LNA without ESD protection has 16.9-dB $|S_{21}|$ gain at 24 GHz. After adding the ESD protection circuits, the $|S_{21}|$ gain of the LNA with dual-diode, stacked-diode, and proposed ESD protection designs are 16.0, 16.3, and 16.2 dB, respectively. The P1dB of the LNA without ESD protection, the LNA with dual diodes, the LNA with stacked diodes, and the LNA with proposed design are -14, -13, -13, and -13 dBm, respectively, and the third-order intermodulation intercept point (IIP3) are -4, -3, -3, and -3 dBm, respectively.

The LNA with and without ESD protection circuits have been fabricated in the same 65-nm CMOS process. The proposed ESD protection design with $W = 40$ μm and $T = 10$ μm is used to protect the $\mathrm{RF_{IN1}}$ and $\mathrm{RF_{IN2}}$ pads of the differential LNA. This ESD protection circuit has been verified to pass the 2.5-kV HBM ESD test. Fig. 12 shows a chip photograph of the ESD-protected LNA. For comparison purposes, the ESD protection designs with dual diodes and stacked diodes are also used to protect the $\mathrm{RF_{IN1}}$ and $\mathrm{RF_{IN2}}$ pads of the other test LNA. The area of each LNA is 750 μm $\times$ 800 μm, including all pads.

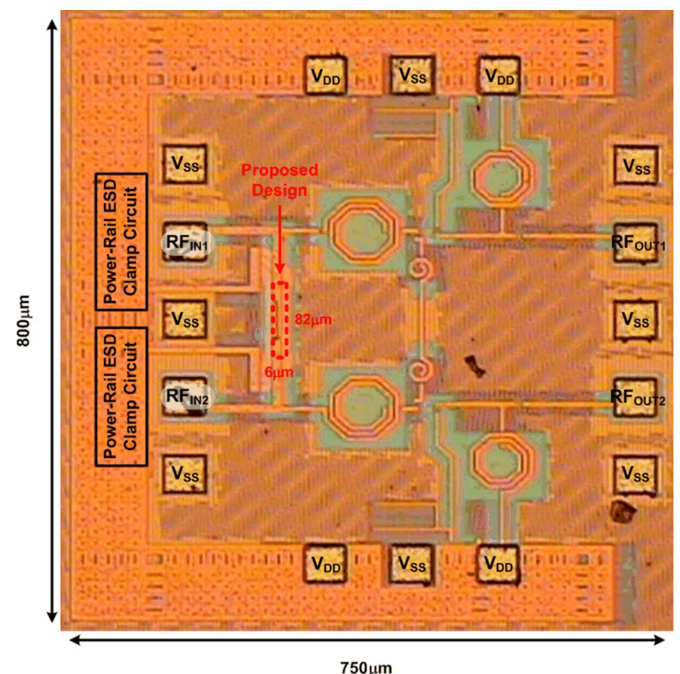

Fig. 12. Chip photograph of differential LNA with proposed ESD protection design.

Fig. 13 shows enlarged photographs of the ESD protection circuits used in the ESD-protected LNA. The metal routing of each ESD protection circuit is also shown in Fig. 13. The ESD devices are connected by using a top metal with 10-μm width and a bottom metal with >30-μm width.

B. Experimental Results

The RF characteristics are measured on wafer through G–S–G–S–G microwave probes. Each LNA operates with the 1.2-V V_{DD} supply and draws a total current of 18 mA. The used bias voltage driven through the external bias tee is 0.65 V. The RF performances of all LNA are measured before and after ESD stress. The measured $|S_{21}|$ parameters and NFs of all the LNAs are shown in Figs. 14–21. The peak gain frequency

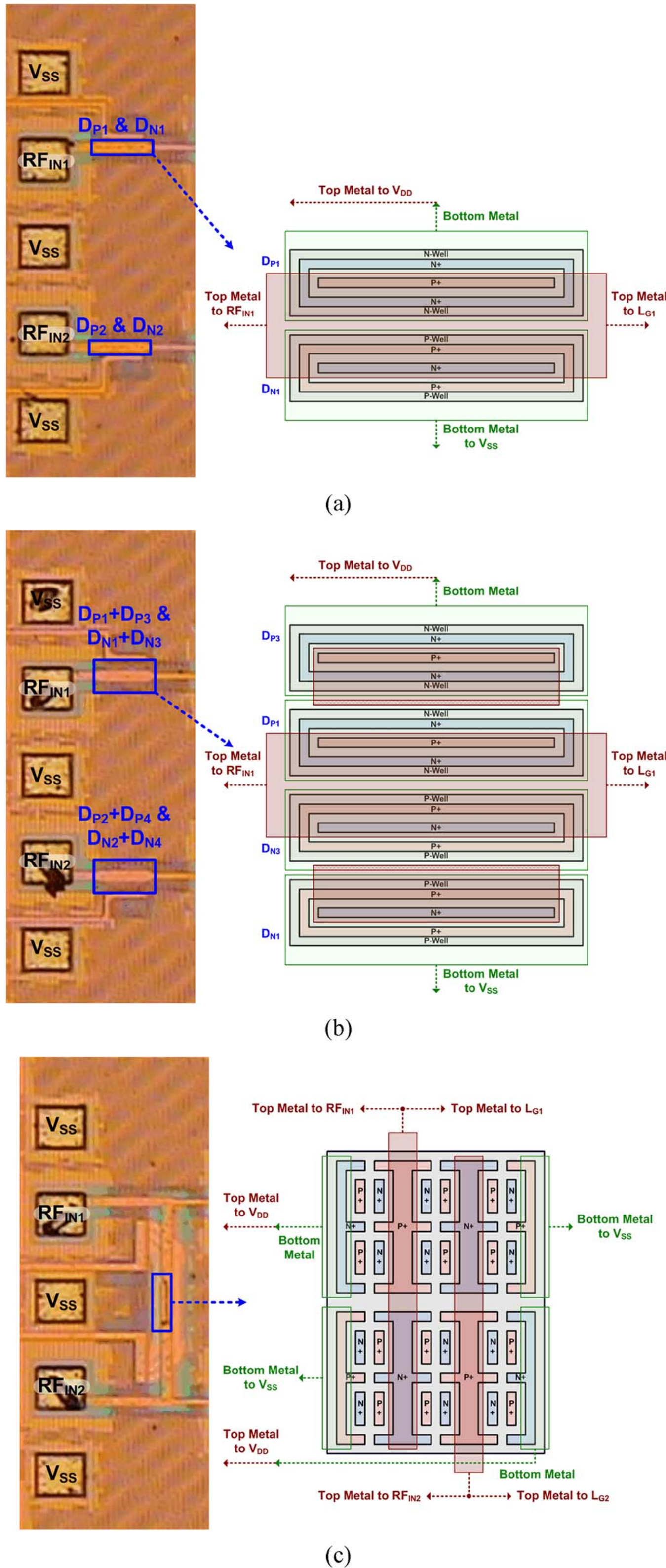

Fig. 13. Chip photograph and metal routing of: (a) dual-diode ESD protection, (b) stacked-diode ESD protection, and (c) proposed ESD protection.

of the LNA is shifted to about 21 GHz. The shift of the peak gain frequency may be due to the inaccurate device model as frequency higher than 20 GHz since the device model is only promised below 20 GHz in the given CMOS process. Before

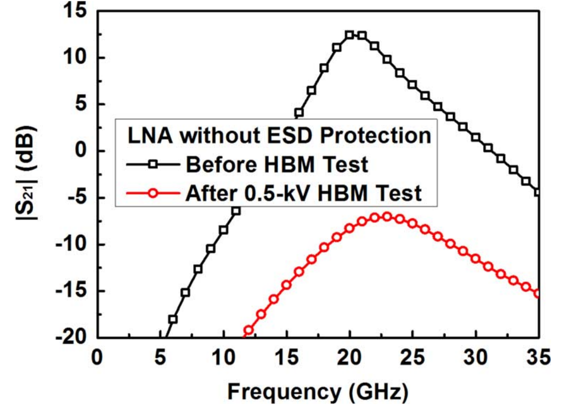

Fig. 14. Measured $|S_{21}|$ of the LNA without ESD protection.

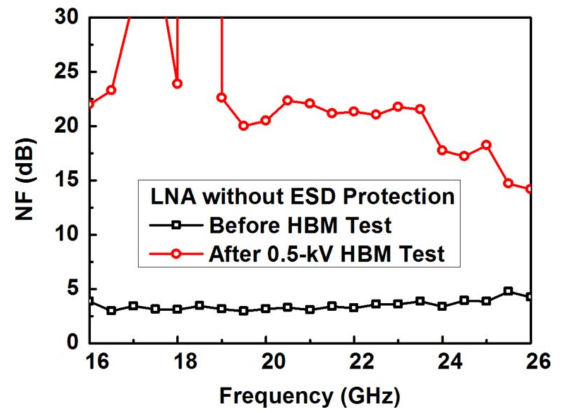

Fig. 15. Measured NF of the LNA without ESD protection.

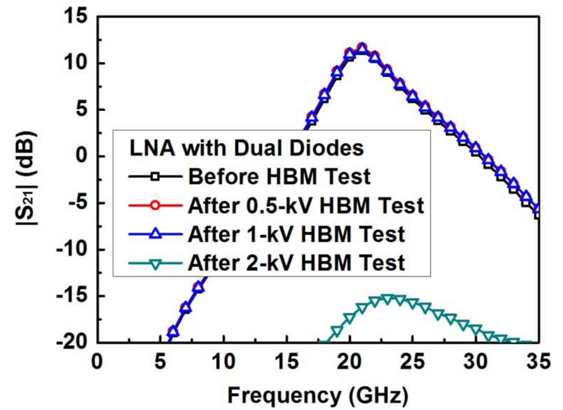

Fig. 16. Measured $|S_{21}|$ of the LNA with dual-diode ESD protection.

ESD stress, the $|S_{21}|$ at 21 GHz of the LNA without ESD protection, the LNA with dual diodes, the LNA with stacked diodes, and the LNA with proposed design are 12.3, 11.3, 11.1, and 11.5 dB, respectively, the $|S_{11}|$ at 21 GHz are all lower than -15 dB, and the NF at 21 GHz are 3.1, 3.8, 4.0, and 4.3 dB, respectively.

To verify the ESD protection ability, the RF performances of all the LNA after ESD tests are re-measured. All PD, PS, ND, NS, and pin-to-pin modes of HBM ESD stresses are performed to the LNA. The RF performances of the LNA without ESD protection are severely degraded after 0.5-kV HBM ESD tests,

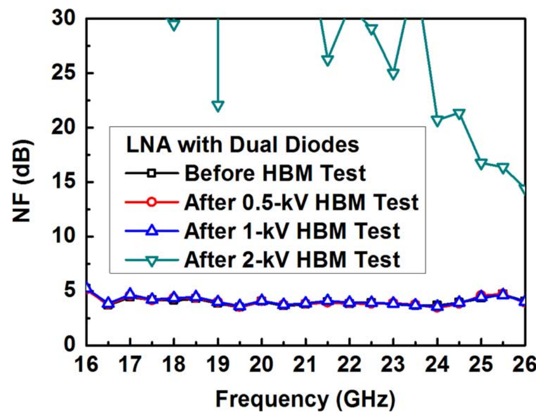

Fig. 17. Measured NF of the LNA with dual-diode ESD protection.

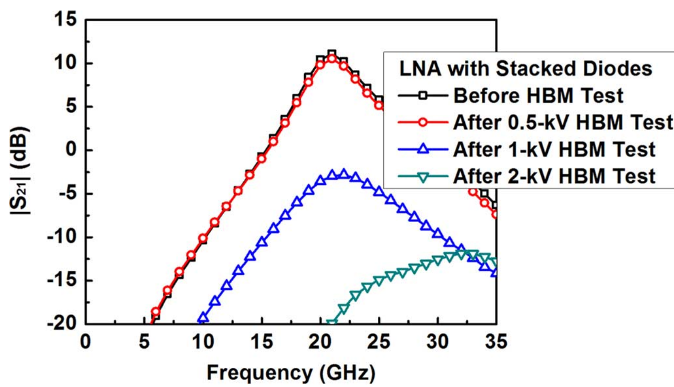

Fig. 18. Measured $|S_{21}|$ of the LNA with stacked-diode ESD protection.

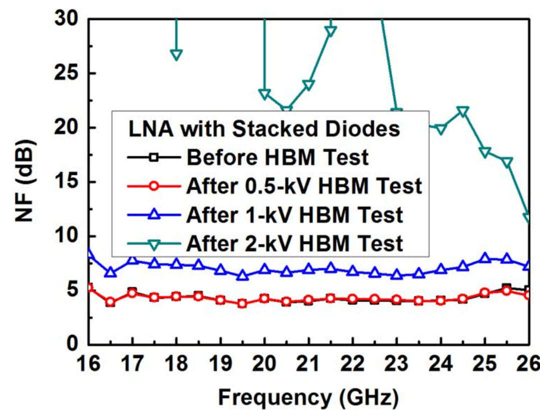

Fig. 19. Measured NF of the LNA with stacked-diode ESD protection.

as shown in Figs. 14 and 15. The RF performances of the LNA with dual- and stacked-diode ESD protections are degraded after 2- and 1-kV HBM ESD tests, respectively, as shown in Figs. 16–19. In contrast, the RF performances of the LNA with the proposed ESD protection design are still excellent matching after 2-kV HBM ESD stress, as shown in Figs. 20 and 21.

The current consumptions of all the LNA after ESD tests are re-measured. Fig. 22 shows the measured current consumptions of all the LNA before and after HBM ESD tests in which 0 kV indicates that the LNA was before the HBM ESD tests.

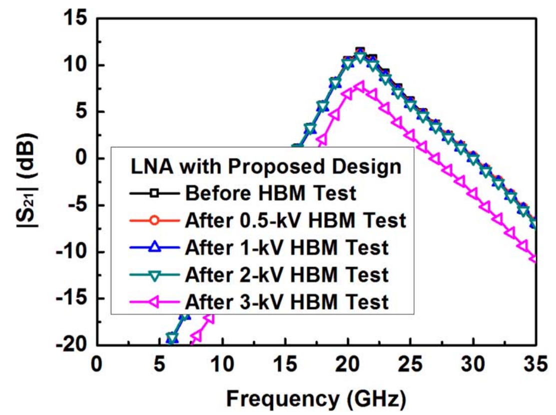

Fig. 20. Measured $|S_{21}|$ of the LNA with proposed ESD protection.

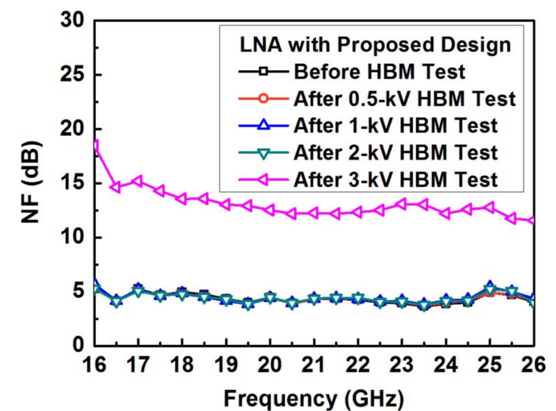

Fig. 21. Measured NF of the LNA with proposed ESD protection.

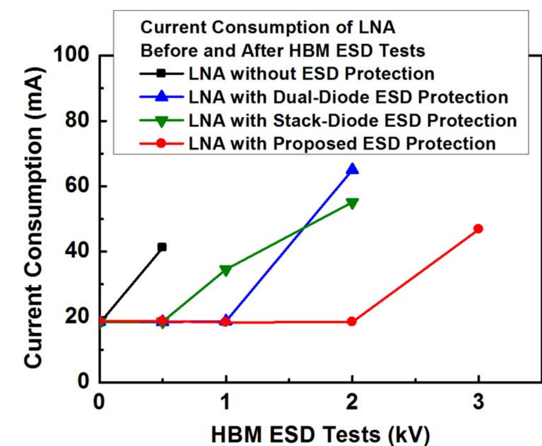

Fig. 22. Measured current consumptions of the LNA before and after HBM ESD tests.

C. Failure Analysis

After ESD tests, the LNA with and without ESD protection circuits are analyzed. The scanning electron microscope (SEM) was used to find the failure locations.

The SEM photographs of the LNA without ESD protection after 0.5-kV HBM ESD tests are shown in Fig. 23. The failure

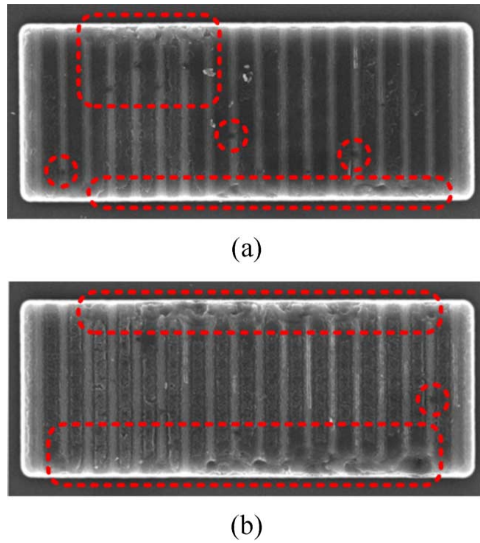

Fig. 23. SEM photograph of: (a) M_1 and (b) M_3 in the LNA without ESD protection after 0.5-kV HBM ESD tests.

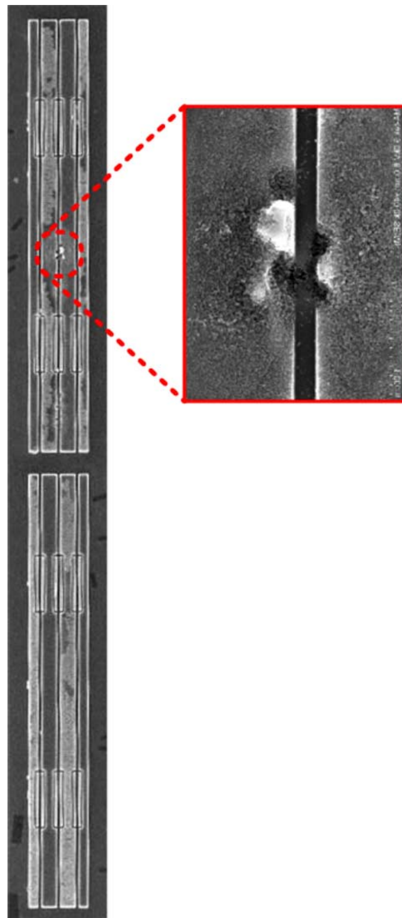

Fig. 24. SEM photograph of proposed ESD protection design after 3-kV HBM ESD tests.

points are located at the gates of M_1 and M_3. The SEM photographs of the LNA with dual- and stacked-diode ESD protections after 2-kV HBM ESD tests are also taken. The failure points are still located at the gates of M_1 or M_3. The failure mechanism indicates that the conventional ESD protection design cannot effectively clamp the overshooting voltage to protect the gate oxide from damage. The SEM photographs of the LNA with proposed ESD protection design after 3-kV HBM ESD tests is shown in Fig. 24. The failure point is located at the embedded SCR_1.

V. Conclusion

The proposed ESD protection diodes with an embedded SCR has been developed for the gigahertz differential LNA. Without adding an extra device, the proposed design combines P + /N-well diodes and P-well/N+ diodes to form the embedded P+/N-well/P-well/N+ SCR paths by using layout skill, and this design also includes the trigger circuit of the SCR to enhance the turn-on speed. The proposed ESD protection design has been verified in a 65-nm CMOS process with low parasitic capacitance, low clamping voltage, and high ESD robustness. The proposed ESD protection design with $W = 40\ \mu$m, $T = 10\ \mu$m, 120.6-fF parasitic capacitance, and 2.5-kV HBM ESD robustness has been applied to a differential LNA. Measurement results verify the RF performances and confirm the ESD protection ability of the proposed ESD protection design.

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