Effects of Gate Dielectric and Process Treatments on the Electrical Characteristics of IGZO TFTs With Film Profile Engineering

Bo-Shiuan Shie, Horng-Chih Lin, *Senior Member, IEEE*, Rong-Jye Lyu, and Tiao-Yuan Huang, *Fellow, IEEE*

***Abstract*— In this paper, high-performance InGaZnO (IGZO) thin-film transistors were fabricated with film-profile-engineering scheme. The impacts of gate dielectric, O_2/Ar ratio during the sputtering of the IGZO, and annealing ambient on the device performance were investigated. It is found that the turn-ON voltage of the device is closely related to the gate dielectric material. For the devices with Al_2O_3 as the gate dielectric, decent performance in terms of high ON/OFF current ratio (>10^8), extremely steep subthreshold swing (62 mV/decade), and good mobility (19.8 $cm^2/V{\cdot}s$) is obtained. The influences of O_2/Ar flow ratio are distinct for the devices with Al_2O_3 gate oxide. Significant improvement in the stability of the devices to the environment is achieved with the anneal done in a low-pressure N_2 ambient.**

***Index Terms*— Film profile engineering (FPE), InGaZnO (IGZO), metal oxide, thin-film transistors (TFTs).**

I. Introduction

METAL–OXIDE–SEMICONDUCTORS are appealing to the manufacturing of large-area electronics because of their fascinating characteristics. In the active-matrix liquid-crystal displays (AMLCDs) application, oxide semiconductors could substitute for amorphous silicon as the channel material of switching thin-film transistors (TFTs) because of the higher carrier mobility [1]. Furthermore, the oxide-based TFTs with superior electrical characteristics are suitable for high-end AMLCD products that demand higher resolution and faster frame rate [2]. Some oxide semiconductors, such as InGaZnO (IGZO), are amorphous, which benefits from the good uniform electrical performance. This feature is advantageous to large-area display applications [3] and makes the oxide semiconductor appealing for replacing low-temperature poly-silicon (poly-Si) as the channel material of driving TFTs in the active-matrix organic light-emitting diode display application [4]. Last but not least, oxide semiconductors can be prepared at low process temperatures, suitable for manufacturing of high-performance flexible display [5]. Apart from display applications, for the past few years, oxide semiconductors have also been explored in various fields, such as back-end-of-line (BEOL) transistors [6], [7] integrated in the Cu-interconnects process. The feasibility is enabled because of the low fabrication temperatures and wide bandgap (>3 eV) of the oxide semiconductors [8]. The latter allows the BEOL transistors to be operated at a high voltage (∼100 V). Considering the high carrier mobility, metal-oxide TFTs have also been proposed to act as select transistors in 3-D flash memories [9]. These examples evidence the potential of oxide-based TFTs for applications to many emerging fields.

Recently, we developed a film-profile-engineering (FPE) scheme [10], [11] for fabrication of high-performance metal-oxide TFTs. Principles of the FPE methods are to deposit the major thin films, e.g., gate dielectric, channel, and source/drain (S/D) metal contacts, in a device with desirable profiles. Feasibility of the FPE concept has been demonstrated by the fabricated ZnO TFTs in our previous work with the aid of a suspended bridge built directly on the wafer surface to shadow the deposition species of selected tools with appropriate process conditions. Nevertheless, the ZnO channel studied in the previous work is polycrystalline in nature, which would give rise to the concern about performance uniformity. In this paper, we adopt an amorphous IGZO (a-IGZO) as channel material in the FPE device fabrication and investigate the influences of gate dielectric and various process parameters on the device performance.

II. Experimental Details

To clearly understand the effects of process conditions on the device characteristics, the fabrication method we adopted is a simple one-mask process rather than the complicated four-mask one reported in [11]. The process flow for fabricating IGZO TFTs is shown in Fig. 1. The starting substrates were n^+ heavily doped Si wafers, which also served as the bottom gate. First, 400-nm-thick oxide and 100-nm-thick poly-Si layers were deposited in sequence through low-pressure chemical vapor deposition (Step I). The two layers served as sacrificial and hard mask (HM), respectively. Next, the S/D regions [Fig. 2(a)] were defined by photolithography with an I-line

Manuscript received March 28, 2014; revised July 13, 2014 and September 17, 2014; accepted September 17, 2014. Date of publication October 8, 2014; date of current version December 9, 2014. This work was supported in part by the Ministry of Science and Technology (MOST), National Science Council of Taiwan, under Contract NSC-102-2221-E-009-097-MY3, in part by the NCTU-UCB I-RiCE Program under Contract MOST-103-2911-I-009-302, and in part by the Ministry of Education, Taiwan, within the ATU Program.

B.-S. Shie, R.-J. Lyu, and T.-Y. Huang are with the Department of Electronics Engineering, Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan (e-mail: boshiuan7374@gmail.com; dragonsnake319@yahoo.com.tw; tyhuang@mail.nctu.edu.tw).

H.-C. Lin is with the Department of Electronics Engineering, Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan, and also with National Nano Device Laboratories, Hsinchu 300, Taiwan (e-mail: hclin@faculty.nctu.edu.tw).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPS.2014.2359992

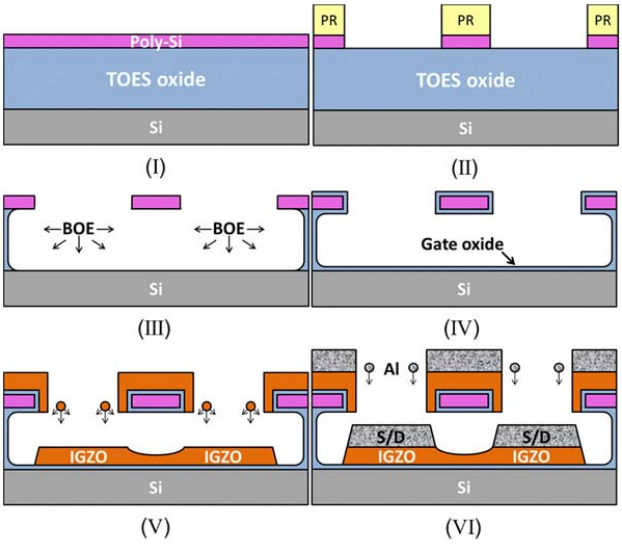


Fig. 1. Process sequence of the FPE IGZO TFT.

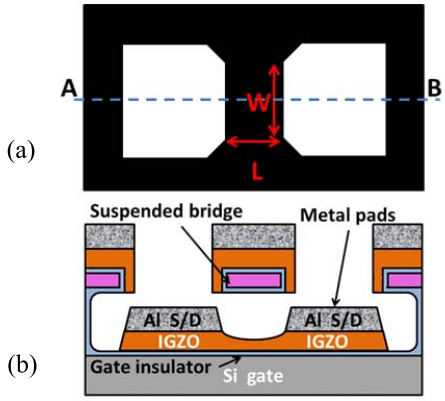


Fig. 2. (a) Top-view layout and (b) cross-sectional view of the FPE device [along the line AB in (a)]. Channel L and W are defined by the patterned poly-Si HM.

stepper and then the poly-Si HM was anisotropically etched with a reactive high-density plasma etcher (Step II). After stripping OFF the photoresist, sacrificial oxide was selectively etched with an HF containing solution (Step III). The suspended poly-Si bridge was formed over the Si substrate as the underlying oxide is cleared off. It represents the pivotal structure for realization of the FPE scheme utilized in the following deposition of gate dielectric, channel, and metal contact layers. In this paper, two kinds of gate dielectric were studied (Step IV). One is SiO_2 with nominal thickness of 60 nm deposited by plasma-enhanced chemical vapor deposition (PECVD) under a pressure of 500 mTorr at 300 °C. The other is 15-nm-thick Al_2O_3 deposited by atomic layer deposition (ALD) at 250 °C. Next, an a-IGZO channel layer with the nominal thickness of 60 nm was deposited by radio-frequency sputtering at an input power of 100 W under a working pressure of 5 mTorr at room temperature (Step V). The gas mixture ratio of O_2/Ar was varied from 0% to 2% to investigate the impact of O_2 flow on the electrical properties of the fabricated devices. Finally, a 100-nm-thick Al was deposited by thermal evaporation as the S/D metal contact pads

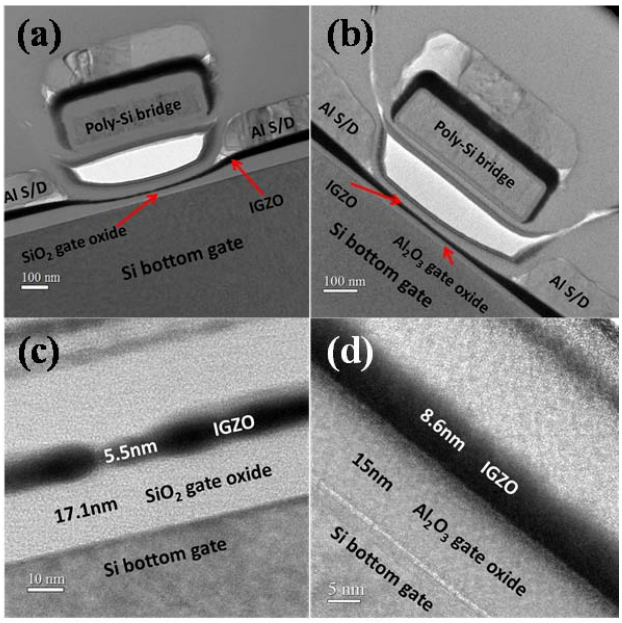


Fig. 3. Cross-sectional TEM images of the fabricated IGZO TFTs with (a) PE-SiO_2 and (b) ALD-Al_2O_3 gate oxide. (c) and (d) Enlarged views taken at the channel center in (a) and (b), respectively.

at room temperature (Step VI). Note that the Al metal layer was neatly formed only on S/D regions and self-aligned to the poly-Si bridge due to the long mean free path (MFP) (>1 m) under a low operation pressure ($\sim 10^5$ Torr). All devices were fabricated without any passivation layer in order to study the effects of annealing ambient. The annealing was done at 300 °C in vacuum or N_2 (0.2 torr) for 30 min. The top and cross-sectional images of the fabricated devices are shown in Fig. 2(a) and (b), respectively. The channel length (L) and width (W) were defined by the patterned poly-Si HM and W/L were 1/0.4 μm. The electrical characterization was carried out by HP 4156C parameter analyzer at room temperature. The device cross section was characterized by transmission electron microscopy (TEM).

III. Results and Discussion

The cross-sectional TEM images of fabricated devices with PE-SiO_2 and ALD-Al_2O_3 gate insulator were shown in Fig. 3(a) and (b), respectively. As can be seen in the figures, in addition to the discrete Al S/D contacts and highly concave IGZO channel, the profile of SiO_2 is concave while that of ALD-Al_2O_3 is conformal. The enlarged views of the devices taken at the channel center for the two devices are shown in Fig. 3(c) and (d), respectively. The measured SiO_2 thickness is $\sim$17 nm at the channel center, much thinner than the nominal value (60 nm). The difference in profile originates from the natures of the deposition methods (PECVD and ALD). During the deposition of PE-SiO_2, the species of SiO_2 were shadowed by the suspended poly-Si bridge because the MFP is not short enough ($\sim 10^{-6}$ m) at the working pressure of 500 mTorr, leading to the concave profile. In the ALD-Al_2O_3 case, the deposition is dependent on self-limiting surface reactions [12] so that the conformity of film profile is good. Another interesting observation is that, despite the same

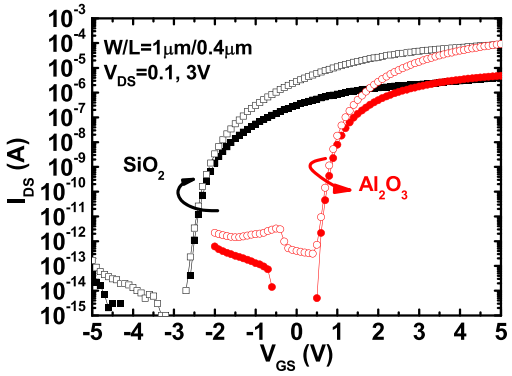


Fig. 4. Transfer curves of the IGZO TFTs with SiO_2 and Al_2O_3 gate oxide measured at $V_{DS} = 0.1$ and 3 V.

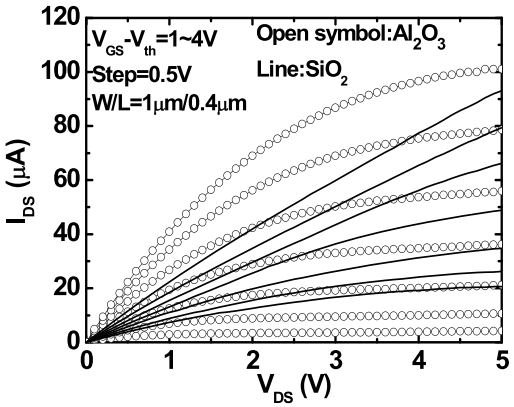


Fig. 5. Output characteristics of the IGZO TFTs with SiO_2 and Al_2O_3 gate oxide, measured at $V_{GS} - V_{th} = 1 \sim 4$V.

deposition condition, the central IGZO channel is ~5.5 nm for the device with SiO_2 gate oxide, much thinner than that for the device with Al_2O_3 gate oxide (8.6 nm). Details about the root causes for the difference are unknown at this stage, but we speculate that the adsorption and migration mobility of the deposition species are significantly affected by the surface properties of the gate dielectric.

Transfer characteristics of the devices with SiO_2 and Al_2O_3 gate oxide are shown in Fig. 4. Channel length (L)/width (W) is 0.4/1 μm. The O_2/Ar flow ratio was 2% during IGZO sputtering and all fabricated devices were annealed at 300 °C in vacuum for 30 min. As can be seen in the figures, the gate dielectric plays an important role in affecting the turn-ON behavior. Evidently, the device is normally ON [threshold voltage (V_{th}) = −1.3 V] with SiO_2 gate oxide, and becomes normally OFF ($V_{th} = 1.14$ V) as Al_2O_3 is employed instead. V_{th} is defined as V_{GS} at $I_{DS} = (W/L) \times 10^{-8}$ A. This indicates the existence of negative fixed charges at the IGZO/Al_2O_3 interface. Overall, the characteristics are decent. Steep *SS* of 81 and 62 mV/decade and high ON/OFF current ratio of 8.9×10^9 and 2.9×10^8 are achieved for device with SiO_2 and Al_2O_3 gate insulator, respectively. The drain-induced barrier lowering is negligible. The outstanding subthreshold performance is mainly ascribed to the formation of the ultra-thin channel [13]. Note that, for TFTs, *SS* can be approximated with the following form [14]:

$$SS = \ln 10 \times \left(\frac{kT}{q}\right) \times \left[1 + \frac{q(N_{it} + N_t)}{C_{ox}}\right] \quad (1)$$

where C_{ox} is gate-oxide capacitance per unit area, k is Botzmann constant, T is absolute temperature, q is elementary charge, N_{it} is interface state density, and N_t is effective trap density contained in the channel. Thinning down of the channel tends to reduce the amount of N_t and thus *SS* is improved accordingly [13], [14]. As compared with the device with a uniform channel thickness, the concave channel profile would help to spread out the current paths conducting from the channel to the metal pads and accordingly reduce the parasitic resistance. Moreover, the thin gate dielectric is also helpful in improving *SS* as C_{ox} is increased. This explains why the device with Al_2O_3 in Fig. 4 shows steeper *SS*.

In the OFF-state region, the leakage current of the device with SiO_2 dielectric is lower than that of the device with Al_2O_3 dielectric, especially at $V_{DS} = 3$ V due to the thicker thickness. Nonetheless, it should be noted that the measurable leakage currents of the devices are in large part caused by the significant overlap areas between bottom gate and S/D metal pads. As the refined structure with a discrete bottom gate is implemented [11], the gate-to-S/D overlap area and accordingly the leakage current can be dramatically reduced. In addition, high field-effect mobility (μ_{FE}) values of 17.5 and 19.8 $cm^2/V \cdot s$ are extracted from devices with SiO_2 and Al_2O_3 gate oxide, respectively. The output characteristics of the fabricated devices are shown in Fig. 5. The device with Al_2O_3 gate insulator shows better performance due to the thinner equivalent oxide thickness and thicker channel [Fig. 3(d)]. Superior electrical characteristics are the evidence of the advantages of the FPE approach. The IGZO/SiO_2 TFT does not show saturation behavior in Fig. 5, which is likely due to the rather high S/D series resistance.

The effects of O_2/Ar flow ratio on the electrical properties of the fabricated devices are also addressed. Fig. 6(a) and (b) shows the transfer characteristics of the devices measured at $V_{DS} = 3$ V with SiO_2 and Al_2O_3 gate oxide, respectively. As can be seen in Fig. 6(a), as the O_2 flow rate increases, V_{th} is slightly increased while the ON current is degraded. The observed trends are ascribed to the reduction in oxygen vacancies in the IGZO channel, which could lead to a decrease in the carrier concentration [15]. To confirm this postulation, we perform Hall measurements on blanket IGZO films deposited with various O_2/Ar flow ratios. The results shown in Fig. 7 demonstrate the above inference that the increase in O_2 flow indeed reduces the carrier concentration in the deposited film.

In Fig. 6(b), an anomalously high current (>10^{-8} A) is induced in the OFF-state in the samples with O_2/Ar ratio of 0.8% and 0%. Note that, the OFF-state leakage is identified to be flowing from the source to drain and shows weak dependence on the gate bias, implying that the flow path of the leakage for the two samples is through the back surface of the channel, as shown in Fig. 8. The different outcomes in this regard between Fig. 6(a) and (b) are in large part due to the thicker channel of the Al_2O_3 split, as shown in Fig. 3(d). As the oxygen flow is reduced during the sputtering, the concentration of oxygen vacancies and thus the concentration of carriers in the channel increases. The conductivity of the

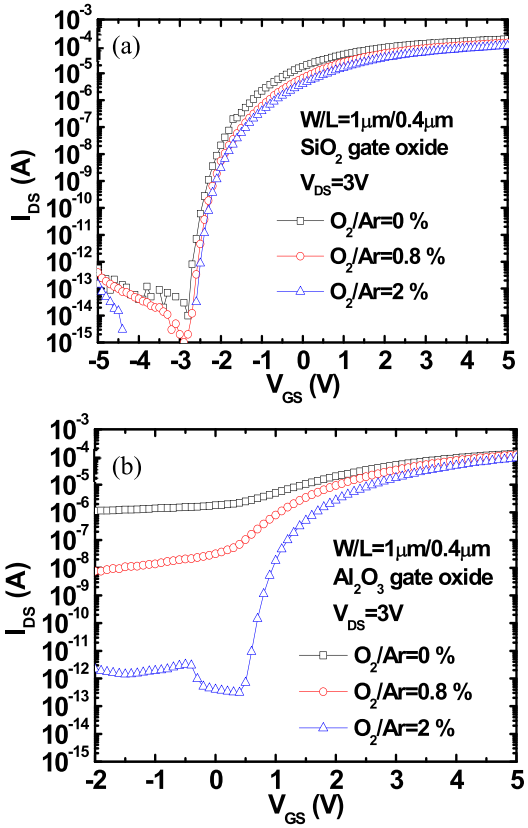


Fig. 6. Transfer curves of the IGZO TFTs with (a) SiO_2 and (b) Al_2O_3 gate oxide measured at $V_{DS} = 3$ V with different O_2/Ar gas mixture ratio during IGZO sputtering.

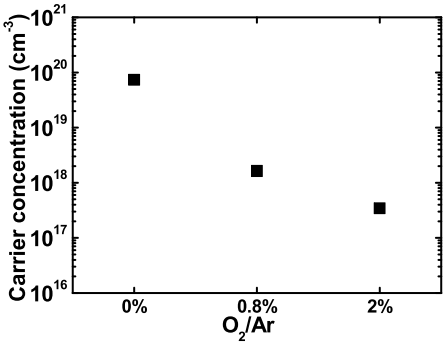


Fig. 7. Carrier concentration obtained by Hall measurements as a function of O_2/Ar ratio.

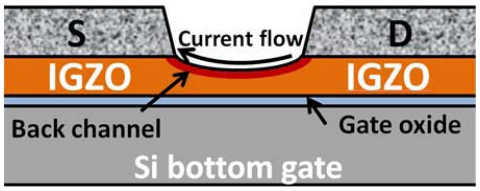


Fig. 8. Leakage path between source and drain is formed at the back surface of the channel as the carrier concentration of the channel is high.

channel increases accordingly. For the Al_2O_3 split, owing to the rather thick channel, the portion of the channel away from the back surface side would not be easily modulated by the bottom gate bias. As a result, the high OFF-state leakage is resulted.

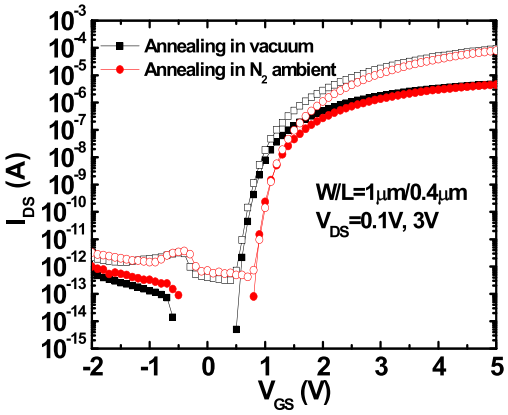


Fig. 9. Transfer curves of the IGZO TFTs with Al_2O_3 gate oxide annealed in vacuum and N_2 ambient measured at $V_{DS} = 0.1$ and 3 V.

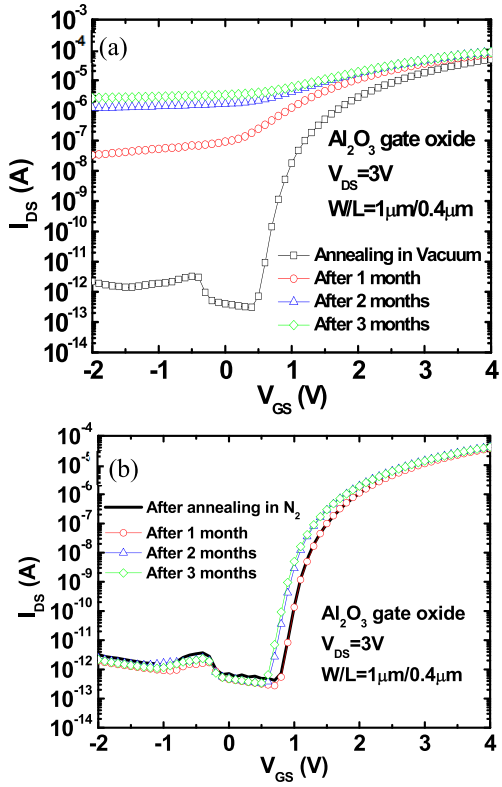


Fig. 10. Transfer curves of the IGZO TFT with Al_2O_3 gate oxide measured at $V_{DS} = 3$ V as a function of storage time after annealing in (a) vacuum and (b) N_2 ambient.

Next, we study the effects of annealing ambient. The test samples are with IGZO channel deposited with O_2/Ar flow ratio of 2% and Al_2O_3 gate insulator. Fig. 9 shows the transfer characteristics of the two splits of devices. As can be seen, the characteristics of the N_2-annealed device are essentially the same as that of vacuum-annealed one except a positive shift in V_{th}. Nevertheless, we found that the stability of the device exposing to the atmosphere could be drastically improved by the low-pressure N_2 annealing. The transfer curves for the two splits of devices measured at $V_{DS} = 3$ V after different

storage days are shown in Fig. 10(a) and (b), respectively. It is clearly observed that the stability is enhanced as the annealing was done in N_2 ambient. For the device annealed in vacuum, punchthrough current is induced just after one month of storage. The cause is attributed to the donor effect reported in [16] owing to the absorption of H_2O. Particularly, when the back surface of the IGZO channel is absorbed by water molecules, extraelectrons could be induced and form a conductive back-channel layer. The situation is similar to that shown in Fig. 6(b) for devices with low O_2 flow. When annealed in N_2, the back surface of the IGZO would be passivated by nitrogen and become immune to water absorption due to the substitution of nitrogen for inactive oxygen [17]. As a result, the shift in device characteristics remains small even after three months of storage, as shown in Fig. 10(b).

IV. Conclusion

The effects of gate-oxide material and process conditions on the characteristics of FPE IGZO TFTs were investigated. Devices with SiO_2 gate oxide are normally ON and become normally OFF as Al_2O_3 gate insulator is used instead. Steep *SS* of 81 and 62 mV/decade, high ON/OFF current ratio of 8.9×10^9 and 2.9×10^8, and superior field-effect mobility of 17.5 and 19.8 $cm^2/(V{\cdot}s)$ are obtained for devices with SiO_2 and Al_2O_3 gate insulator, respectively. The O_2 flow during the sputtering deposition of IGZO is found to have a major impact on the device characteristics, especially for the devices with Al_2O_3 gate oxide. Enhancement in environmental stability is also shown as the fabricated devices were annealed in a low-pressure N_2 ambient.

References

[1] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," *Nature*, vol. 432, no. 7016, pp. 488–492, Nov. 2004.

[2] T. Hirao *et al.*, "Bottom-gate zinc oxide thin-film transistors (ZnO TFTs) for AM-LCDs," *IEEE Trans. Electron Devices*, vol. 55, no. 11, pp. 3136–3142, Nov. 2008.

[3] E. Scheer *et al.*, "Manufacturing of large area high mobility AM-TFT backplanes using IGZO rotary sputtering targets," in *Proc. IEEE Photon. Conf.*, Oct. 2011, pp. 626–627.

[4] J. Y. Kwon *et al.*, "Bottom-gate gallium indium zinc oxide thin-film transistor array for high-resolution AMOLED display," *IEEE Electron Devices Lett.*, vol. 29, no. 12, pp. 1309–1311, Dec. 2008.

[5] J.-S. Park *et al.*, "Flexible full color organic light-emitting diode display on polyimide plastic substrate driven by amorphous indium gallium zinc oxide thin-film transistors," *Appl. Phys. Lett.*, vol. 95, no. 1, pp. 013503-1–013503-3, Jul. 2009.

[6] K. Kaneko, N. Inoue, S. Saito, N. Furutake, and Y. Hayashi, "A novel BEOL transistor (BETr) with InGaZnO embedded in Cu-interconnects for on-chip high voltage I/Os in standard CMOS LSIs," in *Proc. Symp. VLSI Technol.*, Jun. 2011, pp. 120–121.

[7] K. Kaneko *et al.*, "Operation of functional circuit elements using BEOL-transistor with InGaZnO channel for on-chip high/low voltage bridging I/Os and high-current switches," in *Proc. Symp. VLSI Technol.*, Jun. 2012, pp. 123–124.

[8] J. Jeon, G. J. Lee, J. Kim, J. H. Kim, and B. Choi, "High operating voltage application of transparent a-InGaZnO thin-film transistors," *Semicond. Sci. Technol.*, vol. 28, no. 2, p. 025015, 2013.

[9] I. Song *et al.*, "Short channel characteristics of gallium–indium–zinc–oxide thin film transistors for three-dimensional stacking memory," *IEEE Electron Devices Lett.*, vol. 29, no. 6, pp. 549–551, Jun. 2008.

[10] H. C. Lin, R. Y. Lyu, and T. Y. Huang, "Fabrication of high-performance ZnO TFT with sub-micron channel length," *IEEE Electron Devices Lett.*, vol. 34, no. 6, pp. 1160–1162, Sep. 2013.

[11] R. Y. Lyu, H.-C. Lin, M. H. Wu, B. S. Shie, H. T. Hung, and T. Y. Huang, "Film profile engineering (FPE): A new concept for manufacturing of short-channel metal oxide TFTs," in *Tech. Dig. IEDM*, 2013, pp. 288–291.

[12] S. M. George, "Atomic layer deposition: An overview," *Chem. Rev.*, vol. 110, no. 1, pp. 111–131, Jan. 2010.

[13] P. Barquinha, A. Pimentel, A. Marques, L. Pereira, R. Martins, and E. Fortunato, "Influence of the semiconductor thickness on the electrical properties of transparent TFTs based on indium zinc oxide," *J. Non-Cryst. Solids*, vol. 352, nos. 9–20, pp. 1749–1752, Jun. 2006.

[14] H.-H. Hsu, H.-C. Lin, L. Chan, and T.-Y. Huang, "Threshold-voltage fluctuation of double-gated poly-Si nanowire field-effect transistor," *IEEE Electron Devices Lett.*, vol. 30, no. 3, pp. 243–245, Mar. 2009.

[15] X. Xiao *et al.*, "Effect of O_2 flow rate during channel layer deposition on negative gate bias stress-induced V_{th} shift of a-IGZO TFTs," *IEEE Trans. Electron Devices*, vol. 60, no. 12, pp. 4159–4165, Dec. 2013.

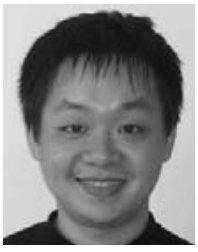
[16] J. S. Park, J. K. Jeong, H. J. Chung, Y. G. Mo, and H. D. Kim, "Electronic transport properties of amorphous indium-gallium-zinc oxide semiconductor upon exposure to water," *Appl. Phys. Lett.*, vol. 92, no. 7, Feb. 2008, Art. ID 072104.

[17] P.-T. Liu, Y.-T. Chou, L.-F. Teng, F.-H. Li, and H.-P. Shieh, "Nitrogenated amorphous InGaZnO thin film transistor," *Appl. Phys. Lett.*, vol. 98, no. 5, Jan. 2011, Art. ID 052102.

Bo-Shiuan Shie received the M.S. degree from National Tsing Hua University, Hsinchu, Taiwan, in 2009. He is currently pursuing the Ph.D. degree with National Chiao Tung University, Hsinchu.

Horng-Chih Lin (S'90–M'94–SM'01) received the Ph.D. degree in electronics engineering from National Chiao Tung University (NCTU), Hsinchu, Taiwan, in 1994.

He joined NCTU, in 2004, where he is currently a Professor.



Rong-Jye Lyu received the B.S. degree in material science and engineering from National Chung Hsing University, Taichung, Taiwan, in 2009, and the M.S. degree in engineering and system science from National Tsing Hua University, Hsinchu, Taiwan, in 2011. He is currently pursuing the Ph.D. degree with National Chiao Tung University, Hsinchu.

Tiao-Yuan Huang (S'78–M'78–SM'88–F'95) received the Ph.D. degree from the University of New Mexico, Albuquerque, NM, USA, in 1981.

He has been a Professor with the Department of Electronics Engineering, National Chiao Tung University, Hsinchu, Taiwan, since 1995.