A 340 GHz Triple-Push Oscillator With Differential Output in 40 nm CMOS

Chun-Hsing Li, *Member, IEEE*, Chun-Lin Ko, *Member, IEEE*, Chien-Nan Kuo, *Member, IEEE*, Ming-Ching Kuo, *Member, IEEE*, and Da-Chiang Chang, *Member, IEEE*

***Abstract*—A low-power triple-push oscillator with differential output is proposed in this letter. By extracting signals from the same current loop, the oscillator can naturally provide differential output without any additional active circuit or passive balun required. Therefore, the output power can be increased and the chip area and power consumption can be reduced. Realized in 40 nm CMOS technology, the proposed oscillator can oscillate at 340.6 GHz while providing equivalent isotropically radiated power (EIRP) as −21.8 dBm. The power consumption is only 34.1 mW from a 0.9 V supply. The oscillator core only occupies area of 0.028 mm^2.**

***Index Terms*—CMOS, differential, oscillator, THz, triple-push.**

I. Introduction

THz applications such as high-speed communications, medical imaging, and security defense, have attracted great attention in recent years. Among circuit blocks of these systems, a signal source with sufficient output power is the key to make these applications feasible. Differential signal source is particularly desired in terms of system aspect. However, signal source design at THz frequency is very challenging because of the speed limit of active devices, especially if using CMOS technology. For instance, the maximum oscillation frequency $f_{\max}$ of 40 nm CMOS adopted in this letter is only around 270 GHz. Obviously, it is not possible to have a fundamental oscillator working at THz frequency, that is, beyond 300 GHz. Therefore, either more advanced technologies with higher $f_{\max}$ is chosen, which increases the realization cost, or proper circuit topology should be developed to tackle the low $f_{\max}$ issue.

N-push oscillator topology is widely employed to have oscillation beyond $f_{\max}$ [1], [2]. Unfortunately, this topology cannot provide differential output. Additional balun or more complicated circuit topology is needed [3]. Power consumption and chip area are inevitably increased. Moreover, if passive balun is employed, induced passive loss degrades the available signal power.

In this letter, a triple-push oscillator with differential output is proposed by extracting output signals from the same current loop without requiring any additional balun or other circuits. Hence, the chip area can be small and the power consumption can be reduced.

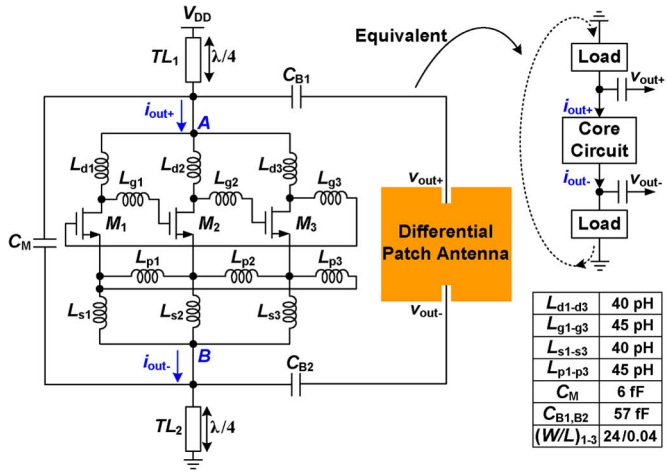

Fig. 1. Proposed triple-push oscillator with differential output.

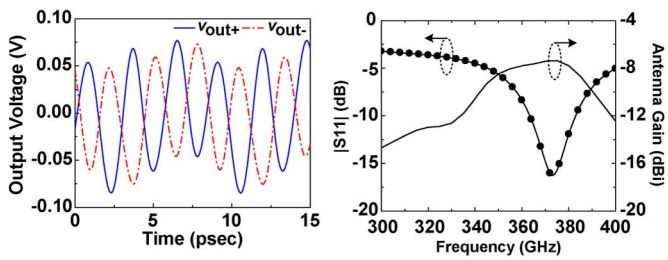

Fig. 2. (a) Post-layout simulation result of differential output waveform. (b) Simulated input return loss and antenna gain of the differential patch antenna.

II. Differential Triple-Push Oscillator Design

Fig. 1 shows the proposed triple-push oscillator that can provide differential output. C_{M} and $C_{\mathrm{B1,B2}}$ are used for output impedance matching and dc blocking, respectively. $TL_{1,2}$ used as RF chokes are realized by microstrip lines with electrical length of $\lambda/4$ at the targeted frequency of 360 GHz. The oscillator is essentially a ring oscillator topology. As the oscillation condition is fulfilled, it oscillates and sustains stable signals

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C.-H. Li is with the Department of Electrical Engineering, National Central University, Jhongli 320, Taiwan (e-mail: chli@ee.ncu.edu.tw).

C.-L. Ko and D.-C. Chang are with the National Chip Implementation Center (CIC), the National Applied Research Laboratories, Hsinchu 300, Taiwan.

C.-N. Kuo is with the Department of Electronic Engineering and the Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan (e-mail: cnkuo@mail.nctu.edu.tw).

M.-C. Kuo is with the Information and Communications Research Laboratories (ICL), Industrial Technology Research Institute (ITRI), Hsinchu 310, Taiwan.

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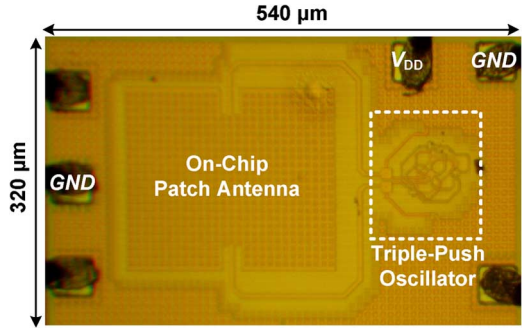

Fig. 3. Chip micrograph of the proposed triple-push oscillator.

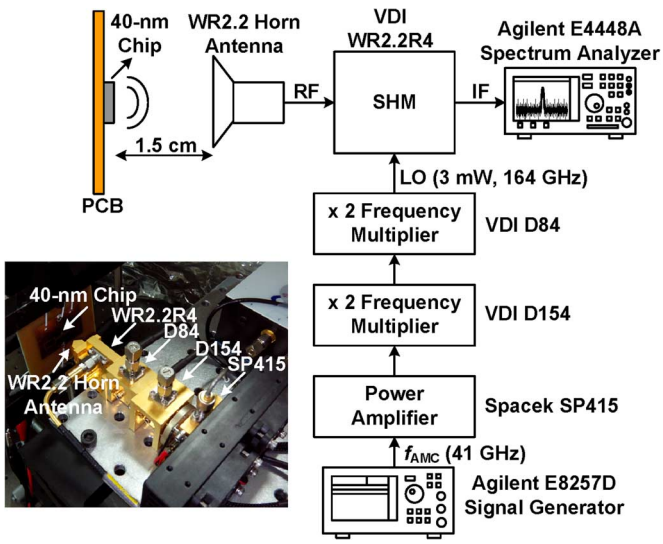

Fig. 4. Experimental setup for measuring oscillation frequency and EIRP.

with equal amplitude but 120° phase difference at drain nodes of M_{1-3}. By combining these signals through $L_{\mathrm{d1-d3}}$ at node A, the 3rd harmonics of these signals are added in phase while 1st and 2nd harmonics will be rejected. Hence, the oscillator can oscillate at f_{osc}, i.e., $3f_{\mathrm{o}}$, which is easily designed to be beyond $f_{\max}$. Note that $L_{\mathrm{g1-g3}}$ is used to adjust the phase and amplitude of the fundamental signal at the drain and the gate to fulfill the optimal condition of transistors for power generation [2]. The same mechanism also applies at the source nodes of transistors. By combining these signals through $L_{\mathrm{s1-s3}}$ at node B, another triple-push signal is obtained. Interestingly, the signals extracted from the source and drain nodes exactly have same amplitude but out of phase. The reason can be easily understood by an equivalent circuit shown in Fig. 1. Essentially, differential operation is guaranteed since differential output currents $i_{\mathrm{out+}}$ and $i_{\mathrm{out-}}$ are extracted from the same current loop. After converting to voltage domain by the Load, $v_{\mathrm{out+}}$ and $v_{\mathrm{out-}}$ shows perfect balanced form.

The oscillator is designed by observing activity condition G_{MM} of a transistor [2]. If $G_{\mathrm{MM}} > 0$, the oscillator can sustain stable oscillation. Transistor width is chosen as 1 μm for maximizing $f_{\max}$. With V_{GS} of 0.9 V, the transistor can provide $f_{\max}$ of around 250 GHz. Although bigger transistor size can give higher G_{MM}, inductors become not easy to be implemented since their inductance value will be too small for the frequency of interest. To have reasonable inductor size and maximize G_{MM}, the finger number of transistors is designed as 24. If these inductors are ideal, the oscillator can provide a

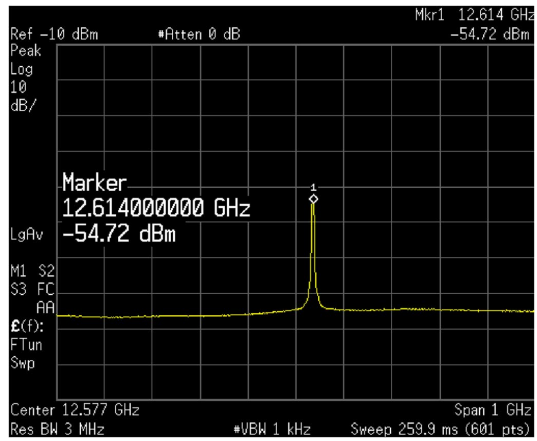

Fig. 5. Measured output IF spectrum.

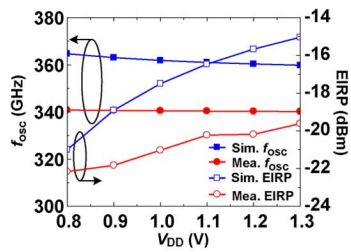

Fig. 6. Measured EIRP and oscillation frequency versus supply voltage.

perfect differential output. However, in practice, a real inductor has parasitic capacitances that shunt the desired output currents, $i_{\mathrm{out+}}$ and $i_{\mathrm{out-}}$, resulting in imbalanced outputs. To tackle this issue, $L_{\mathrm{p1-p3}}$ is added to tune out parasitic capacitance at source nodes to avoid signal leakages from this parasitic path, which can improve output signal balance. They also make the layout more symmetric. Finally, the inductance value of $L_{\mathrm{d1-d3}}$ and $L_{\mathrm{s1-s3}}$, and $L_{\mathrm{g1-g3}}$ and $L_{\mathrm{p1-p3}}$ are designed as 45 pH and 40 pH, respectively, for oscillation at 360 GHz.

Transmission lines are used to realize the inductors. C_{M} is directly realized by a parallel plate using metal layers of M8 and M9 at the summing point located at the center of the layout. The layout arrangement is carefully planned to minimize coupling between the inductors. The whole chip, except the area around transistors, is simulated using ANSYS HFSS while interconnects between transistors to transmission lines are simulated by ANSYS Designer. The post-layout simulation indicates that the fundamental oscillation frequency f_o is around 121 GHz. The simulated output voltage waveform is shown in Fig. 2(a). The amplitude and phase imbalance are only 0.7 dB and 2.4°, respectively. The output power can be as high as -11.1 dBm (100 Ω load) at 363 GHz while only dissipating 31.5 mW from a 0.9 V supply. To assess the oscillator performance, the output differential signal is measured through antenna radiation of an on-chip differential patch with differential input impedance of 100 Ω. The simulated frequency response of the differential patch antenna is shown in Fig. 2(b). The on-chip antenna can provide differential antenna gain of -7.8 dBi at 360 GHz.

III. Experimental Result

The proposed oscillator is realized in 40 nm CMOS technology. The chip micrograph is shown in Fig. 3. The chip size is 540 μm × 320 μm, including dc pads. The oscillator core only occupies 0.028 mm^2. The chip is measured by an

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH PRIOR WORKS

Reference	Technology	Topology	V_{DD} (V)	P_{DC} (mW)	f_{osc} (GHz)	Measurement	P_{out} (dBm)	EIRP (dBm)	Differential Output	Area (mm^2)
[2]	65-nm CMOS	Triple-Push	1.2	61	482	Probe	-7.9	NA	No	0.022
[2]	0.13-μm CMOS	Triple-Push	1.2	71	256	Probe	-17	NA	No	0.052
[3]	65-nm CMOS	Triple-Push	1.8	275	288	Probe	-1.5	NA	Yes	0.285
[4]	45-nm CMOS	Quadruple-Push	1.4	64.4	553	Antenna	-36.5[e]	NA	No	0.286
[5]	45-nm CMOS	Push-Push	1.5	16.5	410	Antenna	-47[e]	NA	No	0.25
[6]	90-nm CMOS	3rd Harmonic	2.0	128	217	Antenna	-8.8	1.8	No	0.531
[7]	45-nm SOI	2nd Harmonic	NA	46.4	316.5	Probe	-21	NA	No	0.338
[7]	45-nm SOI	2nd Harmonic	NA	57.5	216.2	Probe	-14.4	NA	No	0.522
[8]	0.13-μm SiGe BiCMOS	Quadrupler	NA	364	380	Antenna	NA	-13	No	4.18[d]
[9]	65-nm CMOS	2nd Harmonic	1.0	92	265	Antenna	NA	-6.6	No	1.56
[10]	InP HBT	Fundamental	2.3	29.9	311.6	Probe	-9[c]	NA	No	0.12
[11]	InP HEMT	Fundamental	1.3	11.7	346	Probe	-16.0	NA	No	0.16
[12]	InP Gunn Diode	3rd Harmonic	NA	1670	412.2	Waveguide	-5.5	NA	No	NA
This Work	**40-nm CMOS**	Triple-Push	**0.9**	**34.1**	**340.6**	**Antenna**	**-11.1[a]**	**-21.8**	**Yes**	**0.17 (0.028[b])**
This Work	**40-nm CMOS**	Triple-Push	**1.3**	**78.3**	**340.1**	**Antenna**	**-9.1[a]**	**-19.6**	**Yes**	**0.17 (0.028[b])**

(a) Estimated by using simulated antenna gain of −10.5 dBi. (b) Active area. (c) Simulation result. (d) Whole transceiver area. (e) Measured using bolometer.

on-board setup. DC bias is given by wire-bonding to a PCB. The setup for measuring the oscillator frequency and output EIRP is illustrated in Fig. 4. The THz signal from the proposed triple-push oscillator transmits through air, received by a VDI WR2.2 diagonal horn antenna, and then down-converted by a VDI WR2.2R4 subharmonic mixer (SHM) to an IF signal. The IF spectrum can be measured by a spectrum analyzer. The required LO power of 3 mW for the SHM is generated by a chain of frequency multipliers and a signal generator generating a 41 GHz signal of −6.8 dBm. The chip is positioned around 1.5 cm from the horn antenna. The oscillator consumes only 34.1 mW from a 0.9 V supply, around 2.6 mW higher than the simulated result.

The measured output IF spectrum is shown in Fig. 5 as the supply voltage is 0.9 V. The measured IF frequency f_{IF} is 12.61 GHz. As the LO frequency increases by 1 GHz, the IF frequency decreases by 2 GHz. Hence, the oscillation frequency can be calculated by 328 GHz + f_{IF}, i.e., 340.6 GHz, around 22.4 GHz lower than the simulated result. The measured IF power is −52.62 dBm after calibrating IF cable loss of 2.1 dB at 12 GHz. The EIRP of the proposed oscillator can be calibrated to be −21.8 dBm by using Friis transmission equation and noting that the conversion loss of the SHM is around 9.2 dB and the horn antenna gain is around 25 dBi at 340 GHz according to the datasheets provided by Virginia Diodes, Inc. The output power from the proposed oscillator can be estimated to be −11.3 dBm if the simulated patch antenna gain of −10.5 dBi at 340 GHz is used. The oscillation frequency and EIRP at different supply voltage are also measured and illustrated in Fig. 6. The measured result shows a similar trend with that of the simulated one. The EIRP can be increased up to −19.6 dBm as the supply voltage is 1.3 V. Table I summarizes the performance of the proposed triple-push oscillator and makes comparison with prior works [4]–[12]. Obviously, the proposed signal source can give differential output while consuming low dc power, providing high output power, and occupying small chip area.

IV. CONCLUSION

A low-power triple-push oscillator with differential output is proposed and successfully verified by experimental results. By extracting and combining signals from source and drain nodes of transistors, the proposed oscillator can provide differential output without any other circuit required. Implemented in 40 nm CMOS, the measured result shows that the oscillator can oscillate at 340.6 GHz while providing EIRP of −21.8 dBm. The power consumption is only 34.1 mW from a 0.9 V supply.

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