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EFFECTS OF THE REAR INTERFACE STATES AND FIXED CHARGES ON THE ELECTRICAL CHARACTERISTICS OF THIN FILM TRANSISTORS WITH THIN AMORPHOUS SILICON LAYERS

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Abstract—The electrical characteristics of the thin film transistors (TFT's) with hydrogenated amorphous silicon (a-Si:H) films thinner than 0.1 μm have been carefully studied to show that the interface states and fixed charges at the rear interface will play the comparable effects to those at the front interface on the field effect conductance. It is clearly demonstrated that as the thickness of the active layer is smaller than the theoretically expected width of the space charge region, the potential at the rear interface will be affected by the gate voltage. This is very different from the conventional case with a thicker active layer. Since the TFT's at present have smaller typical thicknesses of the semiconductor films than the expected width of the space charge region, the effects of the interface states and the fixed charges at both the rear and front interfaces, as well as the bulk states of the thin a-Si:H films, must be taken into account concurrently.

1. INTRODUCTION

Hydrogenated amorphous silicon (a-Si:H) thin-film transistors (TFT's) have been widely studied because of their practical applications in liquid crystal displays[1]. The field effect conductance measurement is a main technique to analyze the electrical characteristics of the TFT's. In many earlier reports[2–9] concerning the analysis of the field effect conductance of the TFT's, the potential at the semiconductor surface apart from the gate insulator/a-Si:H interface, i.e. the rear interface, was assumed to be zero as a boundary condition for the Poisson's equation. Based on this assumption, it was derived that the electrical potential distribution, namely, the band bending profiles, in the a-Si:H shifts rigidly along the distance from the gate insulator/a-Si:H interface (the front interface) with the varying gate voltage. Then, the effect of the defect states on the conductance at a given gate voltage can be attributed to the states at the front interface with respect to the gate voltage. Thereby, the energy dependent density of states (DOS) of the a-Si:H films can be extracted from the experimentally measured field effect conductance. However, if the expected width of the space charge region corresponding to the gate voltage is larger than the thickness of the semiconductor film of the TFT, in other words, if the band bending extends right through the semiconductor, the assumption of the zero-potential rear interface and the rigidly shifting potential distribution along the distance becomes invalid.

A method was proposed in Ref. [10] to calculate the electrical potential distributions and the field effect conductances in the active layer for different gate voltages to study the effects of the bulk and interface states in the a-Si:H films of the TFT's. In that report, the contribution of the charge from the rear interface was considered. Nevertheless, the a-Si:H film thickness was still thick and the description of the band bending profiles and the field effect conductance for the a-Si:H, much thinner than the theoretical width of the space charge region, has not been reported yet.

In this paper, the effects of interface states and fixed charges on the electrical characterization of the TFT's with thin a-Si:H films are investigated. The density of states in the a-Si:H film is assumed to be spatially uniform and the same for the films with different thicknesses. The results show that the band bending profiles and the effects of the interface states and fixed charges are greatly dependent on the thickness of the semiconductor, as the active layer of the TFT's is thinner than the required width of the space charge region.

2. MODEL CALCULATION

For the one-dimensional gate electrode/insulator/a-Si:H structure, the Poisson's equation in the

a-Si:H active layer can be written as:

$$\frac{d\phi(x)}{dx} = -\xi(x), \tag{1}$$

$$\frac{d\xi(x)}{dx} = \frac{1}{\epsilon_{Si}}\left\{-q\left[\int_{Ev}^{Ec} N(E)(f(E-q\phi)-f(E))\,dE + n_b(e^{-q\phi/kT}-1) - p_b(e^{q\phi/kT}-1)\right]\right\}, \tag{2}$$

where ϕ and ξ are the electrical potential and field in the semiconductor, respectively, x is the distance from the gate insulator/*a*-Si:H interface, q is the electron charge magnitude, ϵ_{Si} is the permittivity of the *a*-Si:H, Ec and Ev are the conduction and valence band edges, correspondingly, $N(E)$ is the energy-dependent DOS and assumed to be spatially uniform, f is the Fermi–Dirac occupation function, n_b and p_b are the densities of the mobile electrons and holes, accordingly, k is the Boltzmann's constant, and T is the absolute temperature. The boundary condition at the rear interface ($x = t$) is:

$$\zeta(t) = \frac{1}{\epsilon_{Si}}\left\{Q_b - \int_{Ev}^{Ec} v_b(E) \times [f(E-q\phi(t))-f(E)]\,dE\right\}, \tag{3}$$

where t is the thickness of the *a*-Si:H layer, Q_b and v_b are the fixed surface charge densities and the surface densities of states at the rear interface, respectively, and $\phi(t)$ is the electrical potential at the rear interface.

To determine the band bending profile in the active layer, the *a*-Si:H film is divided into many super thin slabs with the thickness of Δx. In each super thin film, the electrical potential ϕ can be taken as a constant and the conductivity σ of the film is thus given by

$$\sigma = q\mu_e\left\{\int_{Ec}^{\infty} N_C f(E)\,dE\right\}e^{-q\phi/kT} + q\mu_h\left\{\int_{-\infty}^{Ev} N_V[1-f(E)]\,dE\right\}e^{q\phi/kT} \cong q\mu_e N_C e^{-(Ec-Ef+q\phi)/kT}kT + q\mu_h N_V e^{(Ef-Ev+q\phi)/kT}kT, \tag{4}$$

where μ_e and μ_h are the electron and hole mobilities, respectively, N_C and N_V are the density of states at Ec and Ev, accordingly, and Ef is the Fermi energy.

Once the DOS distribution $N(E)$, the interface states (v_f and v_b), and fixed charges (Q_f, and Q_b) are given, the static field effect conductance-gate voltage characteristics of the TFT's can be attained by the following procedure. Assuming a potential ϕ' for the super thin slab at the semiconductor surface apart from the gate insulator/*a*-Si:H interface, the sheet conductance of this film is $\sigma\Delta x$ and the potential in the super thin slab next to this one is $\phi' - \xi\Delta x$, where the electrical field ξ is given by eqn (3). By repeating the computation and applying eqn (2), the potentials of the rest of the super thin films, i.e. the band bending profile along the active layer, can be determined. Corresponding to this potential profile, the gate voltage V_G can be written as:

$$V_G = -\frac{\epsilon_{Si}}{C_{ins}}\xi(0) + \phi_S, \tag{5}$$

where C_{ins} is the gate insulator capacitance per unit area and $\xi(0)$ and ϕ_S are the electrical field and potential at the front interface. The front interface electrical field can be given by:

$$\xi(0) = \frac{1}{\epsilon_{Si}}\left\{Q + Q_f - \int_{Ev}^{Ec} v_f(E) \times [F(E-q\phi(0))-f(E)]\,dE\right\}, \tag{6}$$

where Q is the total induced charge density in the *a*-Si:H layer, Q_f and v_f are the fixed surface charge densities and the surface densities of states at the front interface, accordingly, and $\phi(0)$ is the electrical potential at the front interface.

Moreover, the conductance of the whole active layer is obtained by summing up the conductance of each super thin film. Therefore, the gate voltage and the associating field effect conductance of the semiconductor can be obtained via giving the potentials ϕ'. Then, the field effect mobility and the threshold voltage are obtained according to the slope and the intercept, respectively, of the curve of gate voltage against field effect conductance for various potentials ϕ'.

The energy gap for the *a*-Si:H in the simulation study is assumed to be 1.8 eV and the Fermi energy is chosen to be 1.2 eV above the valence band according to Ref. [11]. The density of states at the band edges is set to be $10^{21}\,cm^{-3}\,eV^{-1}$. In addition, the widths of the linear distribution of the tail states near the band edges is defined as 0.07 eV. The band mobility of the electrons for the calculation of eqn (4) is given to be $10\,cm^2\,V^{-1}\,s^{-1}$ [12], while the hole mobility is zero since the n^+ source/drain regions will block the conduction of the holes.

To verify the validity of the simulation, the *a*-Si:H TFT's with inverted-staggered structure, the gate insulator capacitance per unit area C_{ins} of 16 nF cm^{-2} and the 250 nm thick active layer, fabricated by successive plasma-enhanced chemical vapor deposition and necessary etching of the silicon nitride, *a*-Si:H, and n^+*a*-Si:H on the chromium gate electrode were also tested to compare with the simulation results. The calculated curve of the field effect conductance vs the gate voltage fit the experimental results perfectly, as shown in Fig. 1. Furthermore, the activation energy of the field effect conductance was also measured with respect to the gate voltage. It gives the good agreement to the calculated separation of the Fermi level from the conduction band edge at the gate insulator/*a*-Si:H interface[11,13].

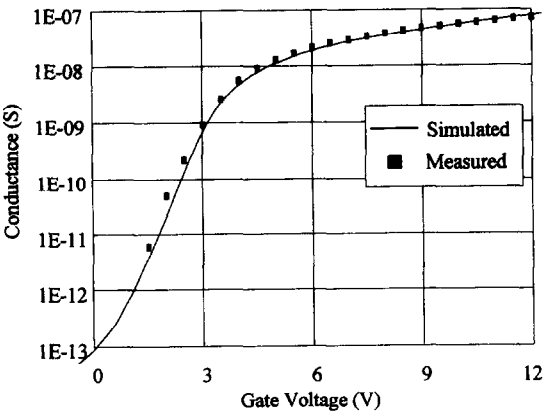

Fig. 1. The measured and the simulated field effect conductance of the TFT as functions of the gate voltage.

3. RESULTS AND DISCUSSION

3.1. *Effects of the* a-*Si:H thickness*

The simulated band bending profiles of the TFT's with various thicknesses of the semiconductor layers, which have the bulk state density of $10^{17}\,cm^{-3}\,eV^{-1}$ biased at the same front interface potential of $Ec–Ef = 0.15$ eV, are shown in Fig. 2. It can be seen that the potential distributions in the active layers with the thicknesses of 1 and 0.5 μm are indistinguishable and approaching to the flat band condition near the rear interfaces. However, a very different potential distribution is observed for the active layers thinner than 0.2 μm. A more detailed illustration in the insert of Fig. 2 shows that the potential profiles for the TFT's with the a-Si:H films thinner than 0.2 μm split near the rear interfaces and the potentials are no longer close to the Fermi level at the flat band condition where $Ec–Ef = 0.6$ eV. With the same gate bias, the departure of the rear interface potential from its flat band position increases as the semiconductor film thickness shrinks down.

This phenomenon is due to the thinner films only having limited volumes to confine the induced charges under a positive gate bias. In a metal/insulator/semiconductor structure, the space charge region is formed as the gate voltage is applied. Provided that the semiconductor film thickness is infinite, the theoretical width of the space charge region corresponding to the surface potential is influenced by the bulk states of the semiconductor and the states at the front interface. For the intrinsic a-Si:H film without interface states, the space charges consist of the free carriers and the charges trapped by the states in the energy gap. If the thickness of the semiconductor is larger than the width of the space charge layer, the potential distributes as it does in the infinitely thick a-Si:H film and the region near the rear interface will not be affected by the gate voltage. The theoretical width of the space charge region calculated with the $N(E)$ of the semiconductor in this study is about 0.5 μm. For the 0.1 μm-thick active layer, however, the Fermi level in the whole film is forced to move toward the conduction band. It shows that the induced charges in the thin semiconductor films under the applied positive gate voltage would push the potential at the rear interface downward to distribute these charges in such a thin layer. Hence, for the thinner a-Si:H film, the Fermi level will be closer to the conduction band to confine the constant amount of the charges induced by the positive gate voltage in a small volume. This is an important feature for the *thin-film* transistors.

In the following context, "thin" film and "thick" film are used to state that the thicknesses of the films are smaller and larger than the theoretical width

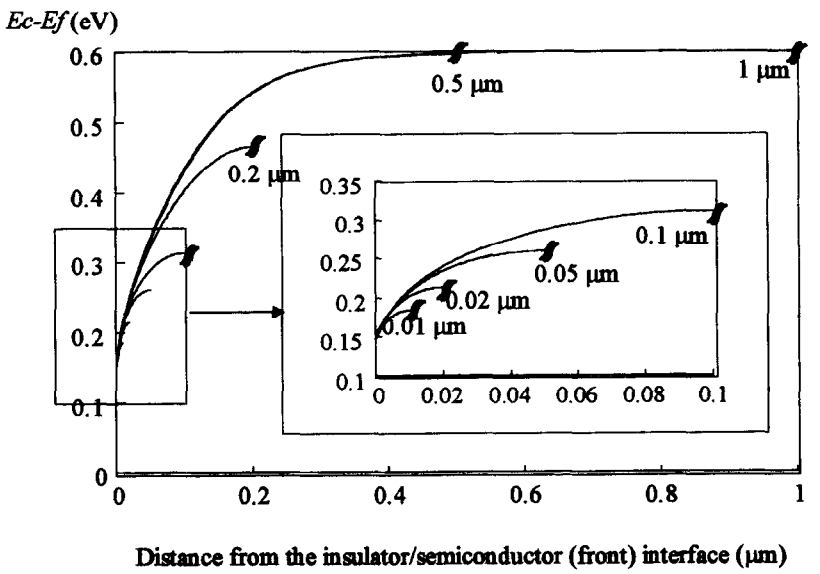

Fig. 2. Band bending potential profiles for several thicknesses of the semiconductor in the TFT's biased at the same front interface potential.

of the space charge region, respectively. It should be noted that the thickness effect of the *a*-Si:H film is dependent on the bulk state density. The smaller deep state density results in the wider space charge region. Therefore, the so-called "thin" and "thick" active layers would depend on the bulk state density in the semiconductor film.

Furthermore, the potential profile in the thick silicon films shifts rigidly along the distance from the insulator/semiconductor interface as the gate voltage increases, as shown in Fig. 3(a). Therefore, the variation of the conductance of the active layer can be all attributed to the change of the potential profile near the front interface. This is the basis of the commonly used technique to extract the density of states of the semiconductor from the field-effect-conductance measurement of the thin film transistors. In Refs [2–9], this analysis method was applied to the TFT's with thick semiconductor films and thus, the increment of the field effect conductance can be exclusively correlated to the states near the front interface at the particular energy, and the DOS can be extracted. However, the results in this study reveal that the assumption of the zero-potential rear interface is improper for the thin semiconductor films and the rigidly shifting behavior of the band bending is not observed in Fig. 3(b), which has the *a*-Si:H film as 0.1 μm in thickness. Accordingly, the relationships of the surface potential ϕ_S at the front interface to the gate voltage V_G and for the semiconductors with different thicknesses are calculated and illustrated in Fig. 4. For the thicker semiconductor films, i.e. 1.0

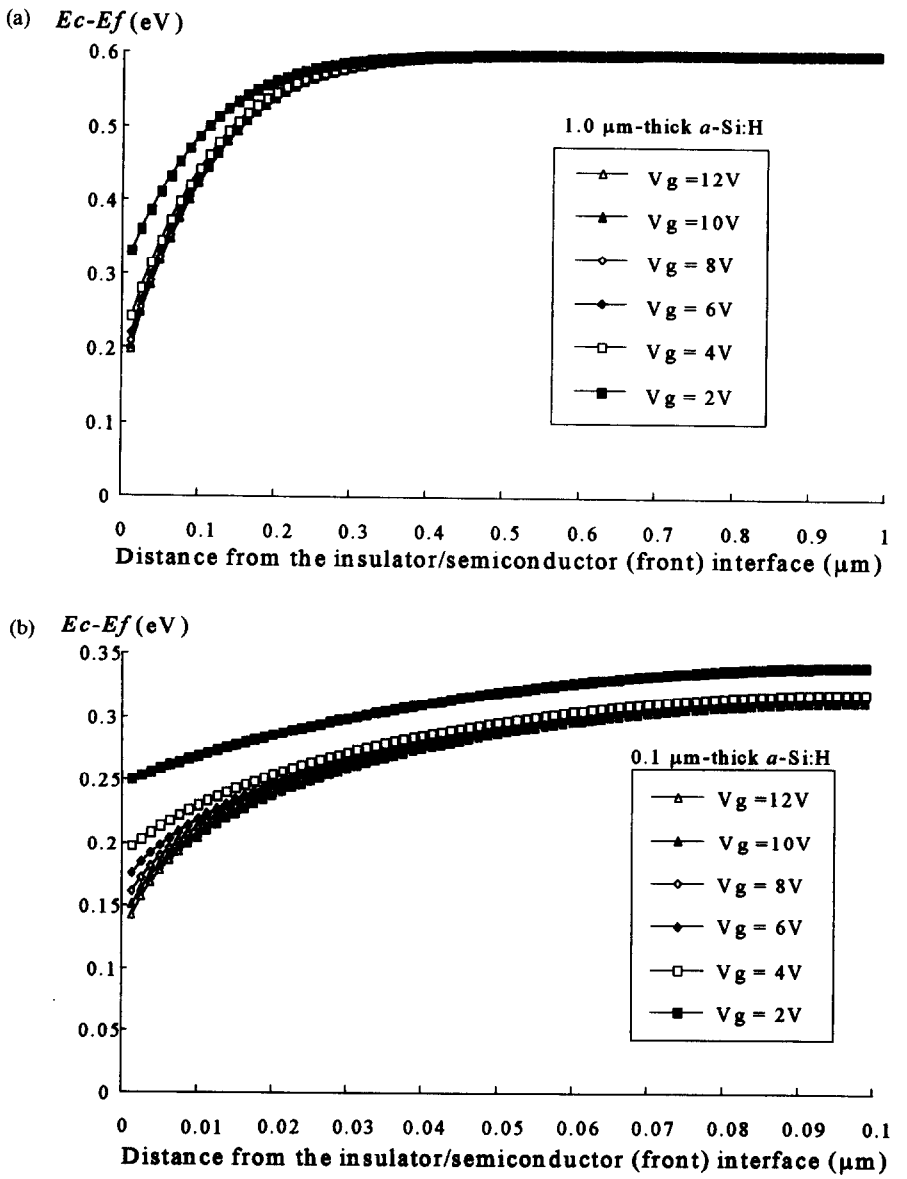

Fig. 3. Potential distributions in the *a*-Si:H films with thicknesses of (a) 1 μm and (b) 0.1 μm under the various gate bias voltage.

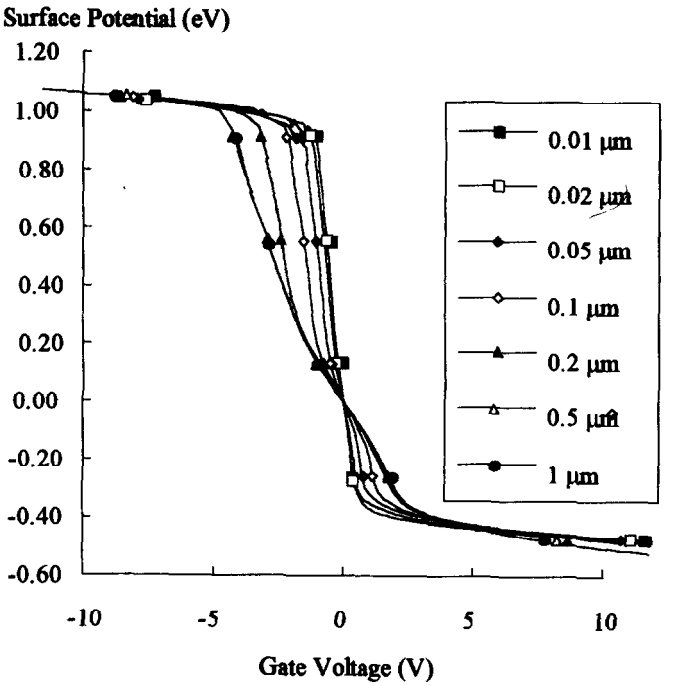

Fig. 4. The dependence of the surface potential at the front interface on the gate voltage for the differently thick semiconductors.

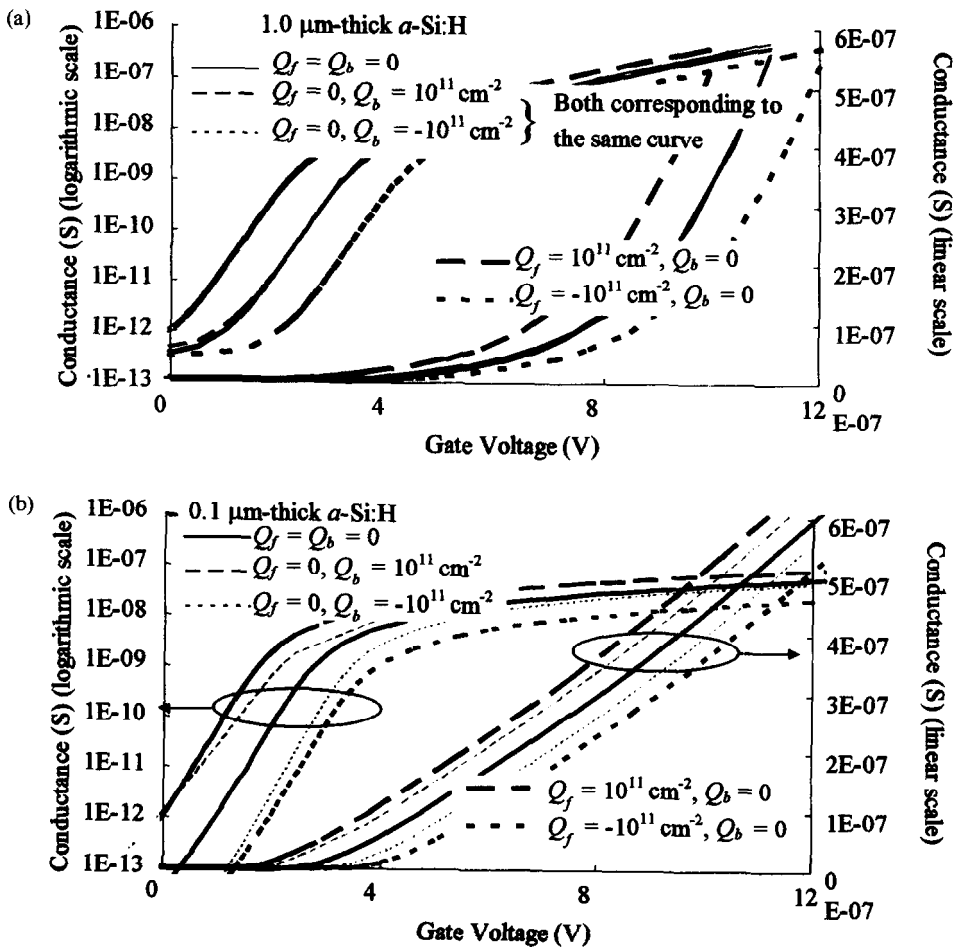

Fig. 5. The field effect conductance as functions of the gate voltage for the (a) 1.0 μm and (b) 0.1 μm a-Si:H TFT's with various rear and front interface fixed charges.

and 0.5 μm, the dependencies of ϕ_S on V_G are identical. On the other hand, the slopes near $V_G = 0$ V are becoming steeper for the thinner films. This is because for the thinner semiconductor films which have the smaller volume, the total deep states are fewer and thus the corresponding gate voltage swing required to fill the deep states is less. Again, the semiconductor thickness effect on the electrical characteristics of the *a*-Si:H TFT's need to be considered as the film is less than the expected width space charge region. By the way, this phenomenon will also happen in the polycrystalline silicon and silicon on insulator (SOI) TFT's if the doping concentration and the density of states of the semiconductor is very low and/or the active layer is very thin.

According to the above discussion, it can be found that the electrical characteristics of the TFT's with thin *a*-Si:H films can be very different from those with thick active layers. For the TFT's with thin semiconductor layers, the variance of the band bending profiles with respect to the gate voltage cannot be described at a single energy in the band gap. Consequently, using the methods presented in Refs [2–9] to analyze the DOS requires careful application. The accurate density of states in the thin active layer can then be obtained by fitting the calculated field-effect conductance with a guessed possible density of states to the experimentally measured data via the procedure proposed in the former section, as the effects of the interfaces are neglected.

3.2. *Interface states and charges*

The effects of the interface fixed charges and interface states on the electrical properties of the TFT's are also considered. Based on the model mentioned in Section 2, the curves of the field effect conductance vs the gate voltage of the TFT's with different front interface fixed charges (Q_f) are calculated. For both thick and thin active layers, the field-effect conductance rigidly shifts along the gate voltage for a constant variation of the front interface fixed charges. Indeed, a common gate capacitance

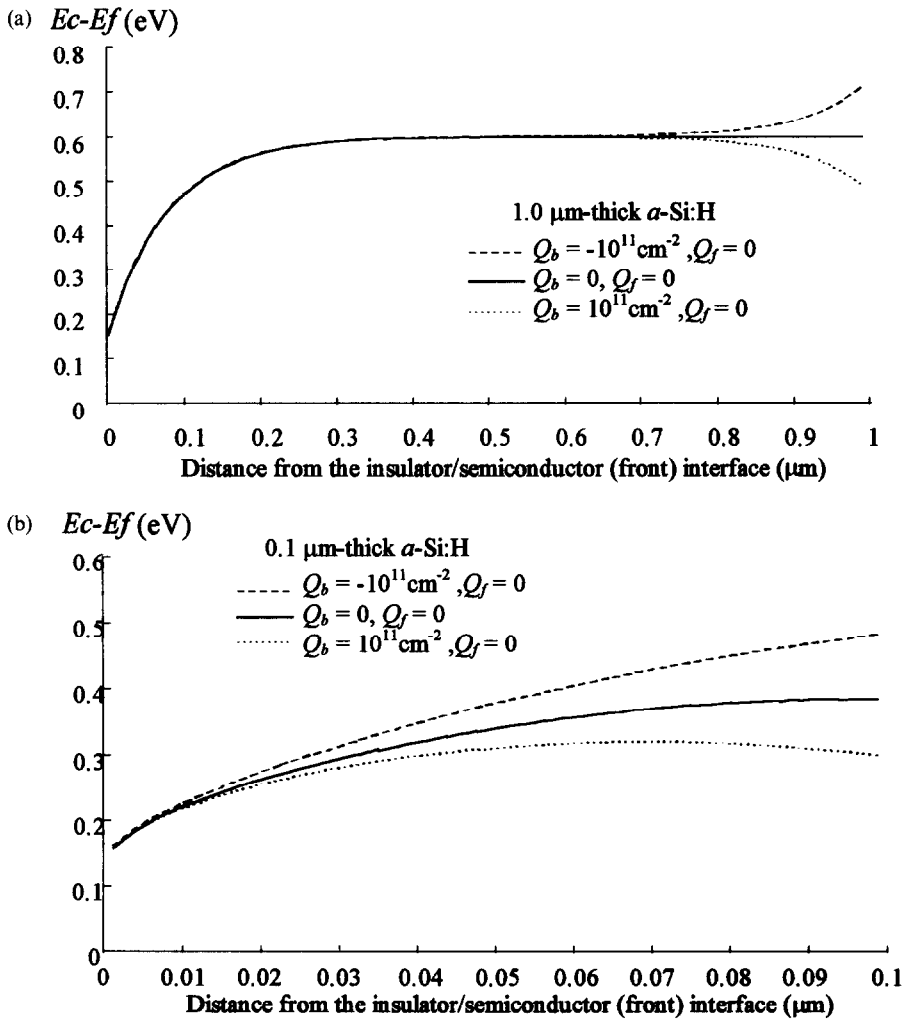

Fig. 6. Potential distributions in the *a*-Si:H films with thickness of (a) 1.0 μm and (b) 0.1 μm biased at the same front interface potential of Ec–$Ef = 0.15$ eV with different fixed charge densities at the rear interface.

value of 16 nF cm^{-2} and the positive and negative charge density of 10^{11} cm^{-2} will lead to the shifts of the threshold voltage with one volt positively and negatively, accordingly, i.e. 1.6×10^{-19} C $\times$ 10^{11} cm^{-2}/16×10^{-9} F cm^{-2} = 1 V. It depicts that the semiconductor films with various thicknesses will have the similar dependence of the file effect conductance shift on the front interface fixed charges. As for the fixed charges at the rear interface (Q_b), different effects on the characteristics of the TFT's were observed for the thick and thin active layers. The effects of Q_b on the field effect conductance of the TFT's with 1.0 and 0.1 μm-thick active layers are illustrated in Fig. 5(a) and (b), respectively. For the thick active layer, the effects of Q_b on the conductance appear only when the TFT's are turned off, as earlier reported[10,14]. Contrarily, for the thin a-Si:H films, Q_b influences the field effect conductance in the subthreshold region and shifts the threshold voltage. To demonstrate how Q_b affects the electrical properties of the TFT's, the potential distributions for the 1.0 and 0.1 μm-thick silicon films with different Q_b values biased at the same gate voltage are plotted in Fig. 6(a) and (b), accordingly. As illustrated in Fig. 6(a) for the thick active layers, the potential distribution under the gate voltage will bend to a distance of about 0.3 μm from the rear interface by the rear interface fixed charge of 10^{11} cm^{-2}. Consequently, the same rear interface charge of 10^{11} cm^{-2} will influence the potential distribution even until the front interface, which has the potential determined by the gate voltage.

Finally, the effects of the states at the front interface and the rear interface are also investigated. For the thick semiconductor, the densities of the front interface states are much less than the total bulk state density and thus their effects cannot be observed. On the contrary, the front interface states for the thin active layer can degrade the electrical properties of the TFT's as reported in a previous paper[9]. For the rear interface states, their effects are slightly apparent for the 0.1 μm-thick a-Si:H film, as shown in Fig. 7, and become more obvious for the TFT's with ultra thin active layers.

The electrical field induced by the gate voltage can penetrate to the rear interface if the a-Si:H layer is thin enough. The states at the rear interface can help pinning the Fermi energy at the rear interface and thus, the potential distributions at different gate bias are not the same as those without rear interface

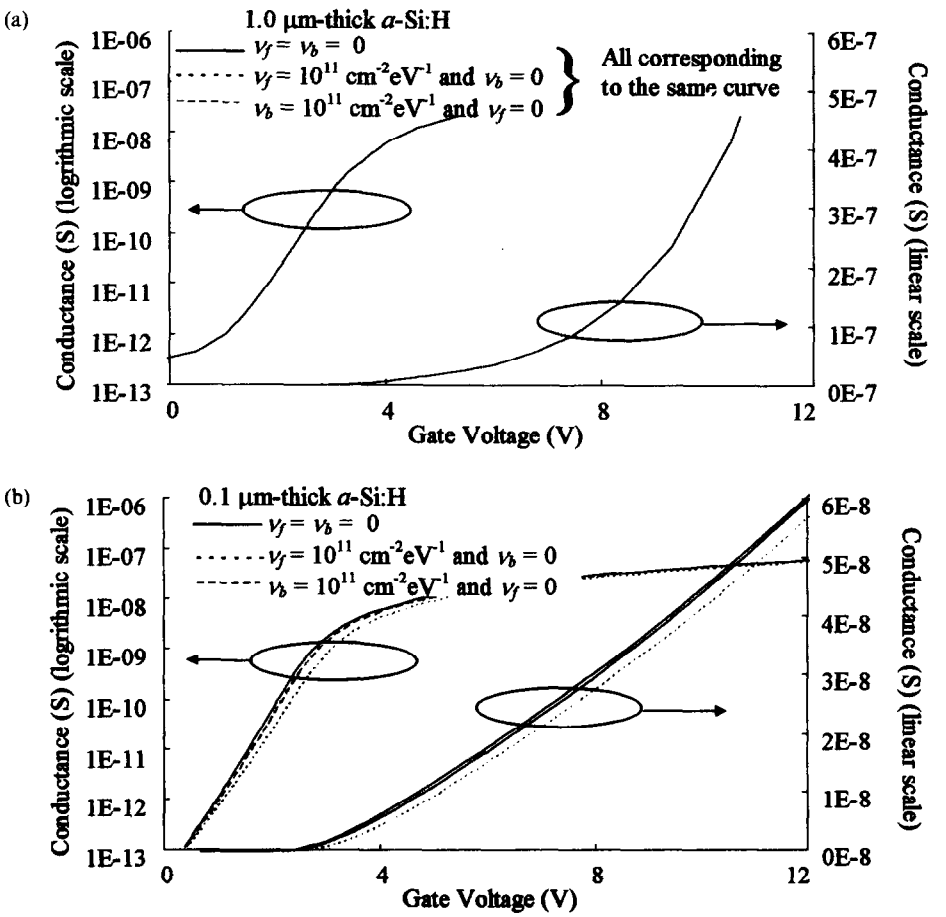

Fig. 7. The dependence of the field effect conductance on the gate voltage of the (a) 1.0 μm and (b) 0.1 μm a-Si:H TFT's with and without the interface states at the front and the rear interfaces.

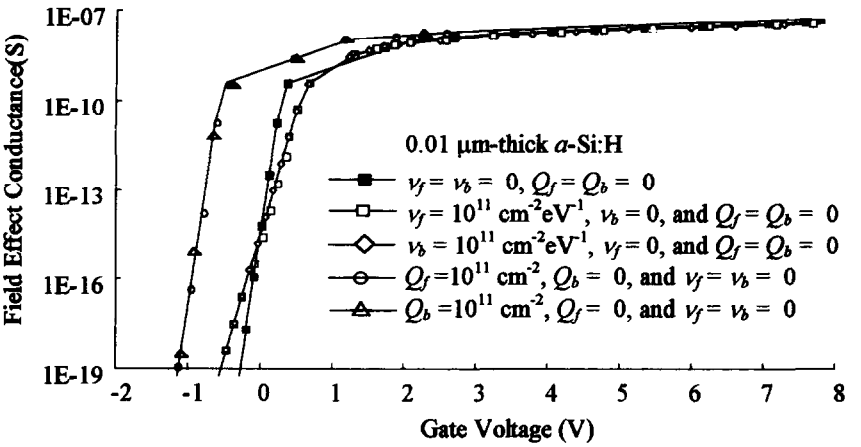

Fig. 8. Effect of the interface states and fixed charges on the field effect conductance for the TFT's with 0.01 μm-thick active layers.

states. Furthermore, the rear interface fixed charge can also generate an electrical field which will couple with that induced by the front gate voltage. The states, as well as the fixed charges at the rear interface, can modulate the band bending profiles if the active layer is thin. For the even thinner a-Si:H layer, their effects become much more important, as will be discussed in the next section.

3.3. *Ultra thin active layers*

For the 0.01 μm-thick a-Si:H films, the curves of the field effect conductance vs the gate voltage of the TFT's without and with the front or the rear interface state density of $10^{11}\,cm^{-2}eV^{-1}$ are calculated and plotted in Fig. 8. The states at the both interfaces considerably degrade the subthreshold behavior of the TFT's. The rear interface states exhibit almost the same effect as the states at the front interface do. It reveals that if the active layer is very thin, the preparation of the rear interface is as important as that for the front interface.

The influences of the fixed charges density at the front and rear interfaces on the field effect conductance of the TFT's with 0.01 μm-thick active layers were also investigated. The fixed charges at the front and the rear interface show nearly the same effect. It depicts that for the TFT's with very thin active layers, the characteristic of the rear interface can affect the performance of the TFT's as much as the front interface does. Since the rear interface for the TFT's is an interface of the a-Si:H and the passivation layer, it must be carefully treated while fabricating the passivation layer.

4. CONCLUSIONS

The band bending profiles of the semiconductor films with different thicknesses are calculated. It is found that if the thicknesses of the a-Si:H films are larger than the theoretical width of space charge region, which is about 5 μm, the potential distribution will behave like the infinitely thick films and the rear interface exhibits little effect on the field effect conductance for the thick a-Si:H films. On the other hand, if the active layer thickness is less than this width, the zero-potential rear interface will be improper and the rigidly shifting behavior of the band bending will not be valid. Furthermore, for the 0.1 μm-thick or even thinner active layers, the properties of the rear interfaces can exhibit profound effects on the electrical characteristics of the TFT's like those of the front interface. Therefore, it is necessary to consider the effects of both the film thickness and the rear front interface for the TFT's with thin a-Si:H films.

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REFERENCES

1. I. Magarino, *Appl. Phys. A* **41**, 297 (1986).
2. N. B. Goodman, H. Fritzsche and H. Ozaki, *J. Non-crystalline Solids* **35** and **36**, 599 (1980).
3. M. J. Powell, *Phil. Mag. B* **43**, 93 (1981).
4. R. L. Weisfield and Anderson, *Phil. Mag. B* **44**, 83 (1981).
5. T. Suzuki, Y. Osaka and M. Hirose, *J. Appl. Phys.* **21**, L195 (1982).
6. M. Shur and M. Hack, *J. Appl. Phys.* **55**, 3831 (1984).
7. R. E. I. Schropp, J. Snijder and J. F. Verwey, *J. Appl. Phys.* **60**, 643 (1986).
8. G. Fortunato and P. Migliorato, *Appl. Phys. Lett.* **49**, 1025 (1986).
9. R. Saleh, N. Nickel, W. Fuhs and H. Mell, *Mater. Res. Soc. Symp. Proc.* **219**, 339 (1991).
10. M. J. Powell and J. Pritchard, *J. Appl. Phys.* **54**, 3244 (1983).
11. S. C. Deane, F. J. Clough, W. I. Milne and M. J. Powell, *J. Appl. Phys.* **73**, 2895 (1993).
12. R. A. Smith, *Hydrogenated Amorphous Silicon*, Cambridge University Press, Cambridge (1991).
13. J. G. Shaw and M. Hack, *IEEE IEDM*, San Francisco, CA, 13–16 December, pp. 915 (1992).
14. A. Rolland, J. Richard, J. P. Kleider and D. Mencaraglia, *J. Electrochem. Soc.* **140**, 3679 (1993).