雙贏策略：如何擷取核心概念與掌握趨勢

Albert Chin

Professor, Dept. of Electronics Eng., Natl. Chiao Tung Univ.

Vice Director, Multi-Disciplinary Research Center, NCTU

Vice Executive Officer, Diamond Project, NCTU

Distinguished Lecturer & Technical Committee, IEEE Electron Devices

Asian Arrangement Chair, IEEE Intl. Electron Devices Meeting (IEDM)

web2.cc.nctu.edu.tw/~achin/

Brief Bio

Education

B. S. , National Tsing Hua Univ., 1982.
Ph.D., Electrical Eng.-The University of Michigan, Ann Arbor, April 1989.

Experience

1.Consultant at Solar Cells fab.
2.Visiting Professor, Dept. of Electrical Eng., Nat'l Univ. of Singapore (2003 & 2004 summer, sabbatical leave at 2005); SNDL initial funding team
3.Consultant at IC fabs in Taiwan
4.RF IC Design House Co-founder
5.Semiconductor Process & Device Ctr, Texas Instruments (1996-1997).
6.Electronics Lab., General Electric (1990-1992).
7.AT&T Bell Labs. (1989-1990).

Publication

More than 400 journal/conference papers (>300 in *IEEE*) have been published.
Premier International conferences:
***IEDM (International Electron Devices Meeting)*- 22 papers including 1 Invited paper & 2 times in best student paper award competition (14 finalist).**
***Symp. On VLSI*- 16 papers including 1 Highlight Section paper & Best Student Paper Award (2005).**
***Int'l Microwave Symp.*- 17 papers & 1 in best student paper award competition.**
Citation ranking in World-wide Engineering- #400 (ISI Web of Knowledge).

Challenges

2009年《泰晤士報》世界大學排行10月上旬出爐，台灣前五名爲台灣大學，清華大學、成功大學、陽明大學、台灣科技大學、交通大學。

稍晚公布的上海交大世界大學排名，100名之後沒有詳細排名，經各項分數加總，台灣共7所大學進500大。台大是兩岸三地唯一在200大以內的學校，從08年的164進步到09年的150名。此外台灣其他上榜大學多數都有進步，清華大學297名、交通大學327名、長庚大學408名、中央大學441名、陽明大學449名。值得注意的是，成大因爲論文被引用的次數高，分數大增，排名躍進到262名。

《泰晤士報》強調學校聲望，印象分數很高，同儕審查占四成，企業意見占一成，國際教師數和國際學生數占一成，師生數比和每位教師論文平均被引用次數各占兩成。

上海交大則是將教師質量和科研成果量化，排名指標包括教師質量、科研成果，校友和教師得到諾貝爾獎、費爾茲獎數量、教師論文被科學期刊引用的數量等。 (中時電子報 2010-01-14)

The paper citation, highly cited papers, premier journal & conference papers etc are the important indices for 大學排名 & 五百億計畫.

Outline

√ 1. 掌握趨勢

2. 如何擷取核心概念

How to Get Paper Accepted?

Importance

1. **Good research topic (pioneering work, hot topic, citation, attending conference)**
2. **Good team (discussion, direction, e.g., SNDL, SG)**
3. **Research capability (hard working, smart, innovation, ….)**
4. **Proper writing with logic and precision**

High-κ Dielectric Innovation to Logic and Memory Devices by a Local/International Team Effort

Albert Chin

Professor, Dept. of Electronics Eng., Nat'l Chiao Tung Univ.

Deputy Director, Nano-Electronics Consortium of Taiwan

Previously with: TI-SPDC, GE- Electronic Lab, AT&T Bell Lab

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Acknowledge the collaboration with Prof. M-F. Li, D. L. Kwong, B. J. Cho, W. J. Yoo, C. Zhu at SNDL Nat'l Univ. of Singapore; Prof. H. L. Hwang, KS Chang-Liao, M. H. Hong, R. N. Kwo at Nat'l Tsing Hua Univ.; Prof. Shui-Jinn Wang at Nat'l Cheng Kung Univ.; also the hard working students

How to Create High Quality Paper?

1. “High Quality Paper” is the pioneering work and/or in the area of hot topic.
2. The High Quality Paper is the paper in high visibility conferences (ISSCC, IEDM etc) or the invited paper in high visibility conferences.
3. The paper citation is the index of High Quality Paper.
4. Good research funding is useful to do high impact research, but the *innovation* is more important.
5. Hard working is important, but *idea* is the key.

Journals in Intl. Electrical & Electronics Engineering (IEEE)

Journal Citation Reports®

RETURN TO MARKED LIST

2006 JCR Science Edition

MARKED JOURNAL LIST

Sorted by: Impact Factor

Abbreviated Journal Title	ISSN	2006 Total Cites	Impact Factor	Immediacy Index	2006 Articles	Cited Half-life
PROG QUANT ELECTRON	0079-6727	556	4.500	0.000	3	9.0
IEEE T PATTERN ANAL	0162-8828	14708	4.306	0.489	182	9.2
IEEE T MED IMAGING	0278-0062	7766	3.757	0.532	141	6.7
P IEEE	0018-9219	11363	3.686	0.387	137	>10.0
IEEE J SEL TOP QUANT	1077-260X	4712	2.842	0.191	188	5.3
J CRYPTOL	0933-2790	846	2.833	0.235	17	9.5
J LIGHTWAVE TECHNOL	0733-8724	11582	2.824	0.446	556	7.0
IEEE T AUTOMAT CONTR	0018-9286	15573	2.772	0.156	256	>10.0
IEEE ELECTR DEVICE L	0741-3106	5233	2.716	0.500	278	4.9
IEEE T IMAGE PROCESS	1057-7149	7045	2.715	0.307	322	6.7
J MICROELECTROMECH S	1057-7157	3455	2.659	0.232	185	5.0
IEEE SIGNAL PROC MAG	1053-5888	1466	2.655	1.212	52	5.4
IEEE T NEURAL NETWOR	1045-9227	6167	2.620	0.280	150	7.5
IEEE WIREL COMMUN	1536-1284	574	2.577	0.050	60	3.1
IEEE INTELL SYST	1541-1672	1120	2.413	0.176	68	5.1
IEEE PHOTONIC TECH L	1041-1135	13528	2.353	0.461	868	4.5
AUTOMATICA	0005-1098	7529	2.273	0.211	247	8.0
IEEE J QUANTUM ELECT	0018-9197	10005	2.262	0.480	150	>10.0
IEEE NETWORK	0890-8044	1135	2.211	0.057	35	6.2
IEEE T SOFTWARE ENG	0098-5589	3203	2.132	0.158	57	>10.0
IEEE T KNOWL DATA EN	1041-4347	2125	2.063	0.159	126	5.5
IEEE PERVAS COMPUT	1536-1268	447	2.062	0.093	43	3.5
IEEE T ELECTRON DEV	0018-9383	10251	2.052	0.340	423	7.7
IEEE T MICROW THEORY	0018-9480	10815	2.027	0.265	529	7.8
IEEE J SOLID-ST CIRC	0018-9200	7148	2.002	0.234	290	6.8

Total journals listed in ISI Web of Knowledge: 206

1. **High Impact Factor Journal**
2. **Reasonable papers/year**
3. **Large total cites (hot area)**

Micro-Electro-Mechanical Systems
微機電系統

Top 10% Journals in EE: 20/206~10%

IEEE- Electronics, Photonics, Control, Communication, Nano Tech, Energy…..

Journals in Electrical & Electronics Engineering (26~50)

IEEE T INFORM THEORY	0018-9448	14149	1.938	0.398	452	8.8
IEEE T NANOTECHNOL	1536-125X	713	1.909	0.207	111	3.0
PATTERN RECOGN	0031-3203	6437	1.822	0.404	228	7.7
IEEE J SEL AREA COMM	0733-8716	6813	1.816	0.209	235	6.9
IEEE T FUZZY SYST	1063-6706	2579	1.803	0.085	71	6.9
IEEE ACM T NETWORK	1063-6692	3614	1.789	0.131	107	7.4
IEEE T GEOSCI REMOTE	0196-2892	7698	1.752	1.055	343	6.7
IEEE T CIRC SYST VID	1051-8215	3406	1.743	0.146	144	5.7
IEEE T ULTRASON FERR	0885-3010	4384	1.729	0.245	261	6.9
IEEE COMMUN MAG	0163-6804	3691	1.678	0.224	165	5.2
J VAC SCI TECHNOL B	1071-1023	10633	1.597	0.268	589	6.7
SEMICOND SCI TECH	0268-1242	4127	1.586	0.240	333	4.9
IEEE T SIGNAL PROCES	1053-587X	8390	1.570	0.203	434	7.5
COMPUT VIS IMAGE UND	1077-3142	1594	1.548	0.288	66	6.8
J ELECTRON MATER	0361-5235	3502	1.504	0.211	318	5.6
IEEE T NUCL SCI	0018-9499	8582	1.497	0.200	606	6.8
IEEE T ANTENN PROPAG	0018-926X	9487	1.480	0.245	477	9.9
IEEE T ADV PACKAGING	1521-3323	763	1.443	0.106	94	4.8
IEEE T INTELL TRANSP	1524-9050	327	1.434	0.163	49	4.0
SENSOR ACTUAT A-PHYS	0924-4247	6774	1.434	0.146	481	5.9
IEEE T COMPUT	0018-9340	5518	1.426	0.243	140	>10.0
IEEE MICROW WIREL CO	1531-1309	1428	1.424	0.159	226	3.0
MICROELECTRON ENG	0167-9317	3817	1.398	0.220	510	3.9
IEEE T DEVICE MAT RE	1530-4388	309	1.373	0.068	73	2.4
IEEE MICROW MAG	1527-3342	210	1.357	0.167	30	4.0

Total journals listed in ISI Web of Knowledge: 206

1. **High Impact Factor Journal**
2. **Reasonable papers/year**
3. **Large total cites (hot area)**

Top 20% Journals in EE: 40/206

Top 25% Journals in EE: 50/206

Journals in Applied Physics

Abbreviated Journal Title	ISSN	2006 Total Cites	Impact Factor	Immediacy Index	2006 Articles	Cited Half-life
NAT MATER	1476-1122	9611	19.194	3.691	139	2.7
MAT SCI ENG R	0927-796X	2807	17.731	0.600	10	5.9
ADV FUNCT MATER	1616-301X	5647	6.779	1.233	279	2.8
SMALL	1613-6810	1240	6.024	1.152	210	1.4
MRS BULL	0883-7694	3359	5.671	0.422	83	5.8
APPL PHYS LETT	0003-6951	140050	3.977	0.566	6153	5.3
LASER PART BEAMS	0263-0346	1317	3.958	1.070	71	3.2
ORG ELECTRON	1566-1199	625	3.418	0.325	77	3.4
NANOTECHNOLOGY	0957-4484	6798	3.037	0.534	1042	2.7
CURR OPIN SOLID ST M	1359-0286	1787	2.662	0.250	12	5.0
J SYNCHROTRON RADIAT	0909-0495	1966	2.377	0.477	65	5.4
EUR PHYS J E	1292-8941	2346	2.373	0.530	117	4.0
IEEE PHOTONIC TECH L	1041-1135	13528	2.353	0.461	868	4.5
J APPL PHYS	0021-8979	96261	2.316	0.305	3609	7.9
PLASMA PROCESS POLYM	1612-8850	211	2.298	0.210	81	1.6
IEEE J QUANTUM ELECT	0018-9197	10005	2.262	0.480	150	>10.0
J NANOSCI NANOTECHNO	1533-4880	1755	2.194	0.309	586	2.3
J PHYS D APPL PHYS	0022-3727	12716	2.077	0.319	778	6.3
IEEE T ELECTRON DEV	0018-9383	10251	2.052	0.340	423	7.7
APPL PHYS B-LASERS O	0946-2171	6177	2.023	0.488	400	5.5
PROG PHOTOVOLTAICS	1062-7995	842	2.009	0.271	59	4.5
IEEE T NANOTECHNOL	1536-125X	713	1.909	0.207	111	3.0
APPL PHYS A-MATER	0947-8396	7937	1.739	0.549	375	4.9
THIN SOLID FILMS	0040-6090	25176	1.666	0.275	1935	6.6
PHYS REV LETT	0031-9007	268454	7.072	1.676	3758	6.8

Total journals listed in ISI Web of Knowledge: 84

1. **High Impact Factor Journal**
2. **Reasonable papers/year**
3. **Large total cites (hot area)**

Top 10% Journals in EE: 8/84

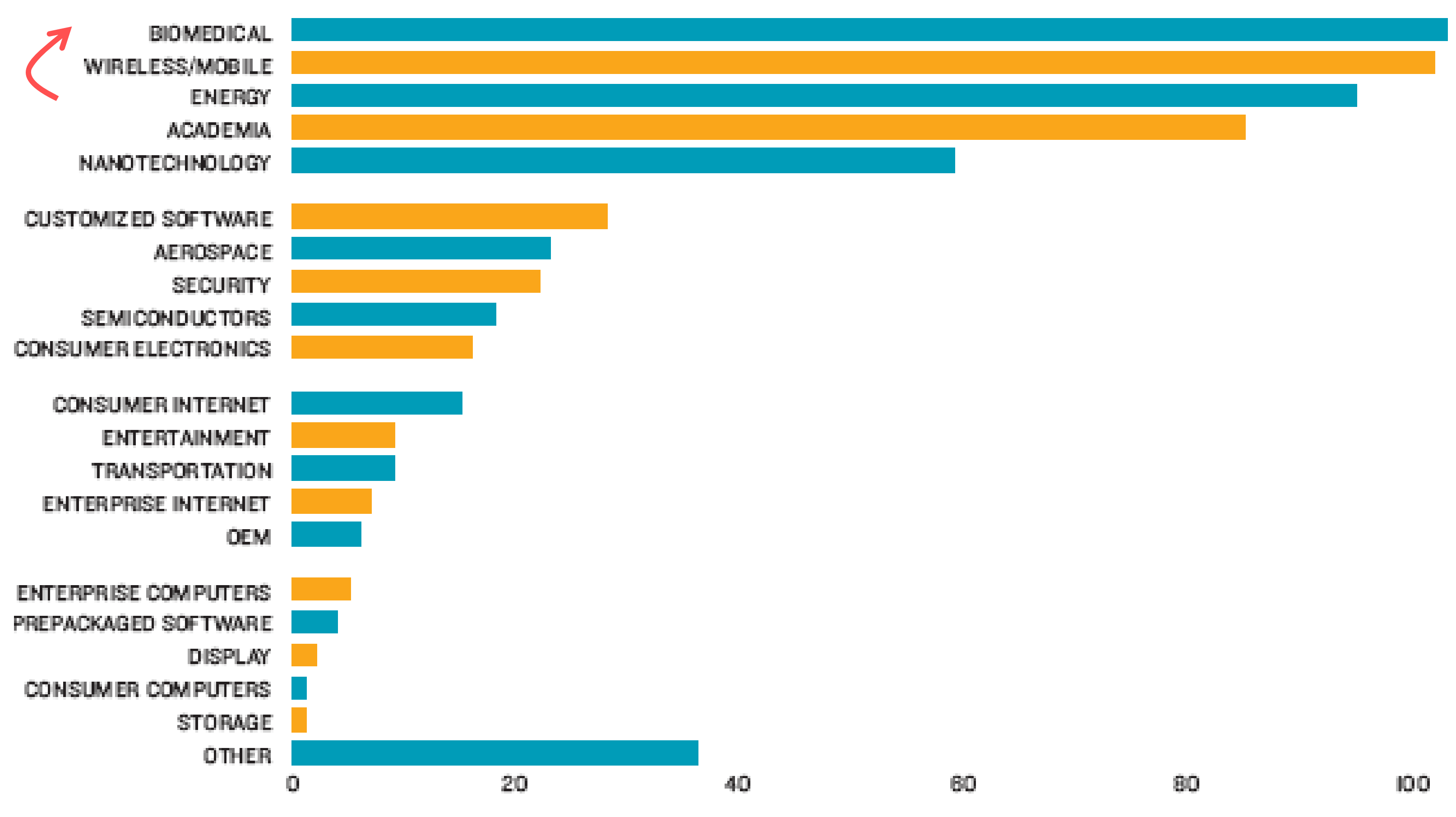
1 reviewer for Appl. Phys. Lett.

Top 20% Journals in EE: 16/84

Nobel Price Winners

Searching Prestigious Company/Media

Searching Prestigious Journals



IEEE Spectrum, Feb. 2007

Attending Premier International Conference

資料來源: 聯合報 | May 11, 2007

記者薛荷玉/台北報導

ISSCC是全世界IC設計領域論文發表的最高指標；在教育部5年500億的「發功加持」下，台大的系統晶片研究中心 (SOC)，今年在ISSCC的論文發表數，不但超過了全球大學，勇奪第一，甚至還超過IBM、Intel等國際知名大廠。

SOC研究團體召集人、台大電機系教授陳良基表示，2002年該團隊在ISSCC的論文發表數還掛零，2003~2005年分別上升到2、3、8篇，去年更一舉達到9篇，勝過麻省理工學院、史丹福及加州大學柏克萊分校，躍居所有大學的第一名；今年論文發表數衝到了11篇，更首度超越IBM、Intel 。

「許多重要的IC設計突破，都在ISSCC發表，如目前任天堂、SONY遊戲機中的CPU，都是IBM做的，就於3年前在ISSCC發表。」陳良基說。

而今年在ISSCC發表的論文，則包括了全世界最快的電路，達75GHz，可運用在無線通訊；陳良基說，目前手機的通訊僅2.4GHz，未來增加到75GHz時，等於頻寬擴充30倍，用手機接收電影、畫面，速度都將快很多。

ISSCC是引領全球、最先進的固態電路及系統晶片國際學術會議，由國際電機電子工程師學會（IEEE）每年2月召開，每年都吸引電子業領先廠商及頂尖IC設計工程師參與；受邀於ISSCC發表的主題演講，將是未來5~10年業界注目的焦點。

Attending Premier International Conference

NTU Tops the World in the 2008 International Solid State Circuits Conference (ISSCC) with Seven Theses Accepted for Presentation

The International Solid State Circuits Conference (ISSCC) is scheduled to take place from February 3rd -7th 2008 in San Francisco, California. Regional conferences are also scheduled to be held from November 26th to December 3rd in Japan, Taiwan, Korea and China.Statistics have shown that NTU ranks the sixth place in global industrial and academic institutions, and starting from 2005, NTU has occupied the first place in academic institutions for six years in succession. This year NTU has seven theses accepted for presentation at ISSCC, a feat that remains unrivalled in the world!

To express his gratitude for Media Tek and TSMC's contributions to NTU, President Si-chen Lee presented Certificates of Appreciation to these two semiconductor companies during the ISSCC 2008 Press Conference and the ISSCC 2008 Banquet and NTU ISSCC Paper Contribution Appreciation which were held in Taipei on November 28th.President Lee emphasized that, although NTU's remarkable performance in ISSCC is largely attributable to the efforts put forth by faculty and students, the support from Taiwan's semiconductor industry also plays a pivotal role. He specifically mentioned Media Tek's sponsorship of N.T. 100 million in the past five years to set up the "NTU/Media Tek Wireless Communication Laboratory" and its offer of scholarships to students whose papers are accepted for presentation. In addition, President Lee said that the "International Research Project" was instrumental in the development of the cutting edge 90 nanometer production process. As he pointed out, the research project was a collaboration among TSMC, UC Berkeley, Stanford and NTU.

www.ntu.edu.tw/engv4/spotlight/2007/e071210_1.html

Attending Premier International Conference

International Electron Devices Meeting (IEDM)

So, what's the correlation between the revenue and the productivity at the IEDM? Or is there a correlation? The table below shows a list of 2004 top-10 semiconductor manufacturers based on IC Insights 2004 revenue projection and the number of papers they presented at IEDM 2004.

1. Intel	8
2. Samsung	21.5
3. TI	3
4. Renesas	3
5. Infineon	7.5
6. Toshiba	11
7. STMicro	12
8. TSMC	4.5
9. NEC	5.5
10.Freescale	4.5

The overall top-10 list for the number of papers presented at IEDM 2004 looks like this.

1. Samsung	21.5
2. IBM	16.5
3. STMicro	12
4. Toshiba	11
5. Intel	8
6. Infineon	7.5
6. CEA-LETI	7.5
8. IMEC	7
9. National University of Singapore	6
10.NEC	5.5

www.semitechonline.com/feature_article.html#postmortem

Attending Premier International Conference

國立交通大學獎狀

本校電子工程系荊鳳德教授學研殊優，在全球半導體特優 International Electron Devices Meeting 會議，有四篇論文發表，為國際學術界之光，對提升吾校之國際學術地位，及促進科技研發之蓬勃發展，貢獻良多，殊堪嘉許。謹頒此狀，以茲表揚。

校長

中 華 民 國 九 十 四 年 十 月 六 日

國立交通大學獎狀

本校電子工程系荊鳳德教授學研殊優，在半導體特優 Symp. On VLSI 會議，有四篇論文發表，為國際學術界最優，對提升吾校之國際學術地位，及促進科技研發之蓬勃發展，貢獻良多，殊堪嘉許。謹頒此狀，以茲表揚。

校長

中華民國九十四年三月二十九日

IEDM in Electron Devices is similar to ISSCC in Circuit (NTU called the Oscar in IC)
(listed in IEEE database, also suggested to VP of Thomson Scientific)

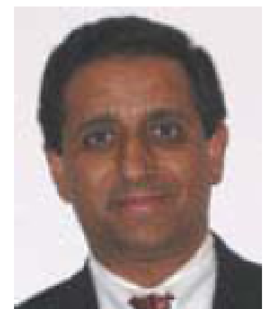
Visibility & Job Connection

International Electron Devices Meeting (IEDM)

Intel Takes 45 nm HKMG Process to IEDM

David Lammers, News Editor -- Semiconductor International, 12/12/2007 5:39:00 AM

Intel Corp. (Santa Clara, Calif.) provided some details of its 45 nm high-k/metal gate (HKMG) process flow at the International Electron Devices Meeting (IEDM) in Washington, D.C., although key elements of the pFET electrode metal remained shrouded.



Kaizad Mistry, Vice President of Logic Integration, Intel

Kaizad Mistry, vice president of logic integration, said Intel used a "high-k first, metal gate last" approach. By keeping the high-temperature annealing steps used to activate the dopants in between the dielectric and metal gate deposition steps, Intel is able to maintain a good workfunction metric for the electrode of its pFET transistor, which he said was 51% faster than the previous generation.

The hafnium-based gate dielectric has a 1 nm equivalent oxide thickness (EOT) for both n- and p-type transistors, with a 7 Å interfacial layer, which Mistry referred to as a "transition layer." Although Intel does not provide its inversion thickness, Mistry said in an interview that the difference between the EOT and T_{inv} "is about 4 Å, plus or minus 1." The physical thickness of the HK layer was 18-20 Å, which is thick enough to provide what Mistry said was a 25× improvement in NMOS leakage current, compared with SiO_2, and a three orders of magnitude (1000×) improvement in PMOS leakage.

The contribution of metal-gate/high-k technology:
according to Intel co-founder Gordon Moore, "The implementation of high-k and metal materials marks the biggest change in transistor technology since the introduction of polysilicon gate MOS transistors in the late 1960s."

Possible for Nobel Laureates!

Visibility & Job Connection

2006畢業	高瑄苓博士	snoopy@mickey.ee.nctu.edu.tw	長庚大學電機工程學系助理教授
2006畢業	賴單宏博士	Vololai.ee90g@nctu.edu.tw	SanDisk/Toshiba公司
2005畢業	廖全昌博士	ccleo@ms47.url.com.tw	國外晶圓代工廠 Manager副處長
2005畢業	于殿聖博士		台積電主任工程師
2004畢業	楊明維博士	yummy.ee88g@nctu.edu.tw	台積電製程整合部門
2003畢業	林全益博士	u8811810@cc.nctu.edu.tw	台積電Memory部門 Technical Manager
2003畢業	黃志翔博士	mic@cc.nctu.edu.tw	台積電先進元件部門Technical Manager
2003畢業	詹婷婷博士	nana.ee88g@nctu.edu.tw	聯發科無線通訊部門副理
2002畢業	C. L. Sun博士		中研院/National Research Council Canada
2002畢業	陳坤白博士		聯發科副理
2001畢業	林偉霖博士		銘傳大學助理教授
2000畢業	巫勇賢博士		清大工科副教授
2010畢業	張明峯博士	jackiejang.eo95g@nctu.edu.tw	台灣積體電路公司
2010畢業	蘇涵超博士	q1894109@mail.ncku.edu.tw	台灣積體電路公司記憶體部門
2010畢業	張惠 博士	tpwang@alummi.nctu.edu.tw	中科院微電子所
2009畢業	林士章博士	d9563815@oz.nthu.edu.tw	服役中
2009畢業	黃瑞謙博士	commi.ee93g@nctu.edu.tw	服役中
2008畢業	鄭詩饌博士	feldcheng@hotmail.com	博士後研究
2008畢業	楊學人博士	bagaalo@yahoo.com.tw	台灣積體電路公司
2008畢業	鄭存甫博士	schumacher.mse88@nctu.edu.tw	台灣積體電路公司主任工程師
2007畢業	金明鋒博士	mcking.ee92g@nctu.edu.tw	Qualcomm(高通)全球市值第一的 IC Design House/Senior Manager/USA
2007畢業	吳建宏博士	q1892122@ccmail.ncku.edu.tw	中華大學助理教授
2007畢業	江國維博士	gorden.ee91g@nctu.edu.tw	台灣積體電路公司記憶體部門
2006畢業	洪彬舫博士	binfun.ee92g@nctu.edu.tw	台積電RF產品部門主任工程師
2006畢業	陳家忠博士	wallance.ee91g@nctu.edu.tw	台積電RF部門

http://web2.cc.nctu.edu.tw/~achin/member.htm

Outline

1. 掌握趨勢

2. 如何擷取核心概念

√ -Go Back to Fundamentals

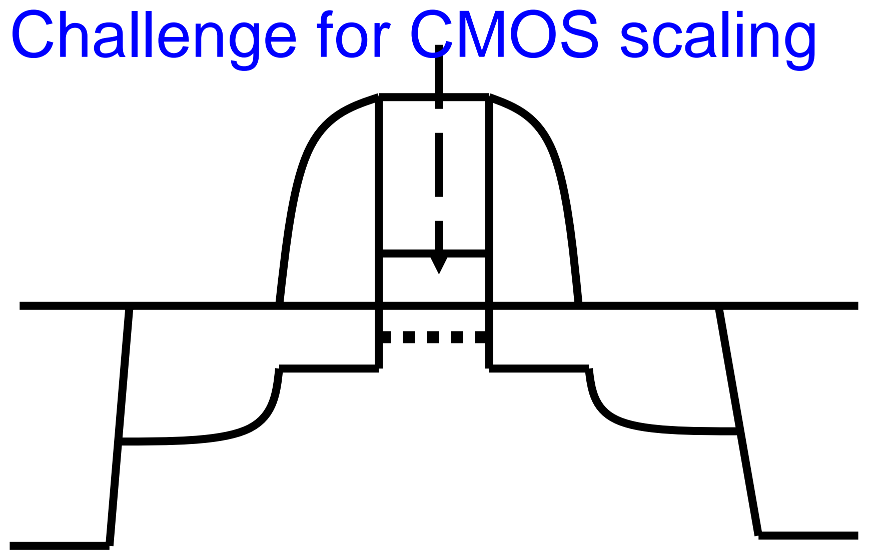
-Understanding the Problem

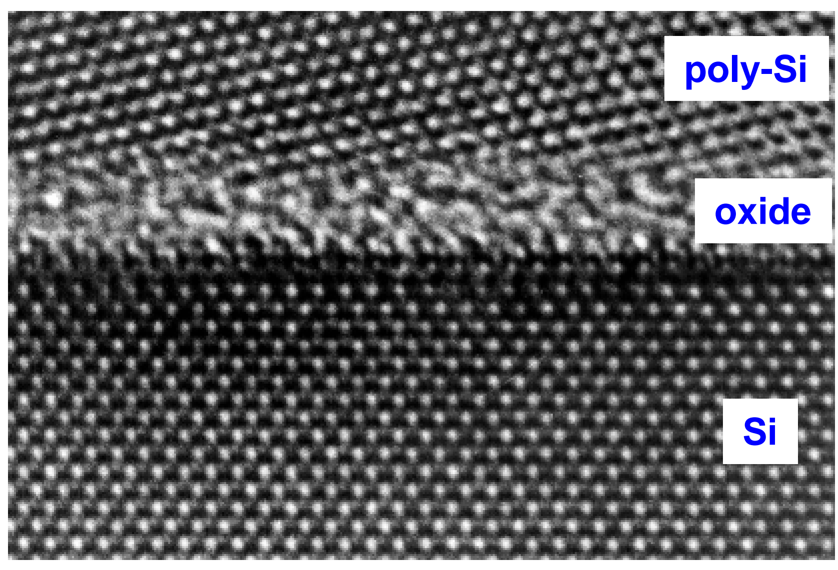
-Multi-Disciplinary Capability

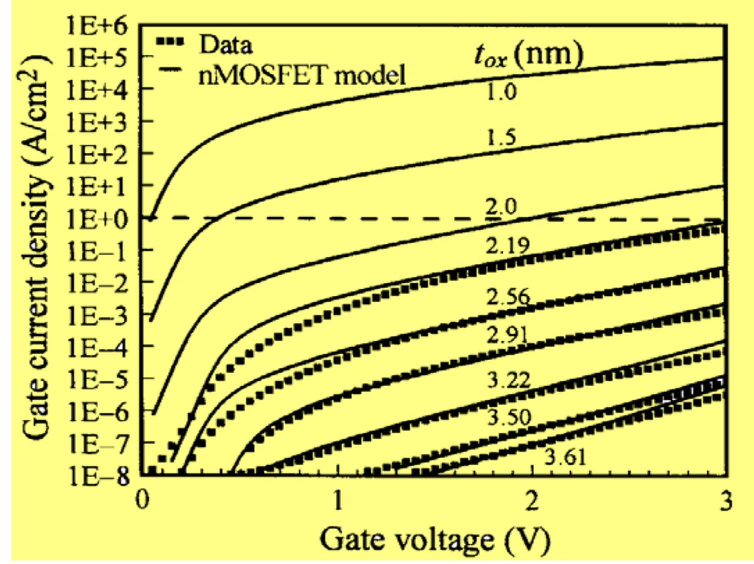
(Examples: nano-technology & RF)

Go Back to Fundamentals

Challenge for CMOS scaling





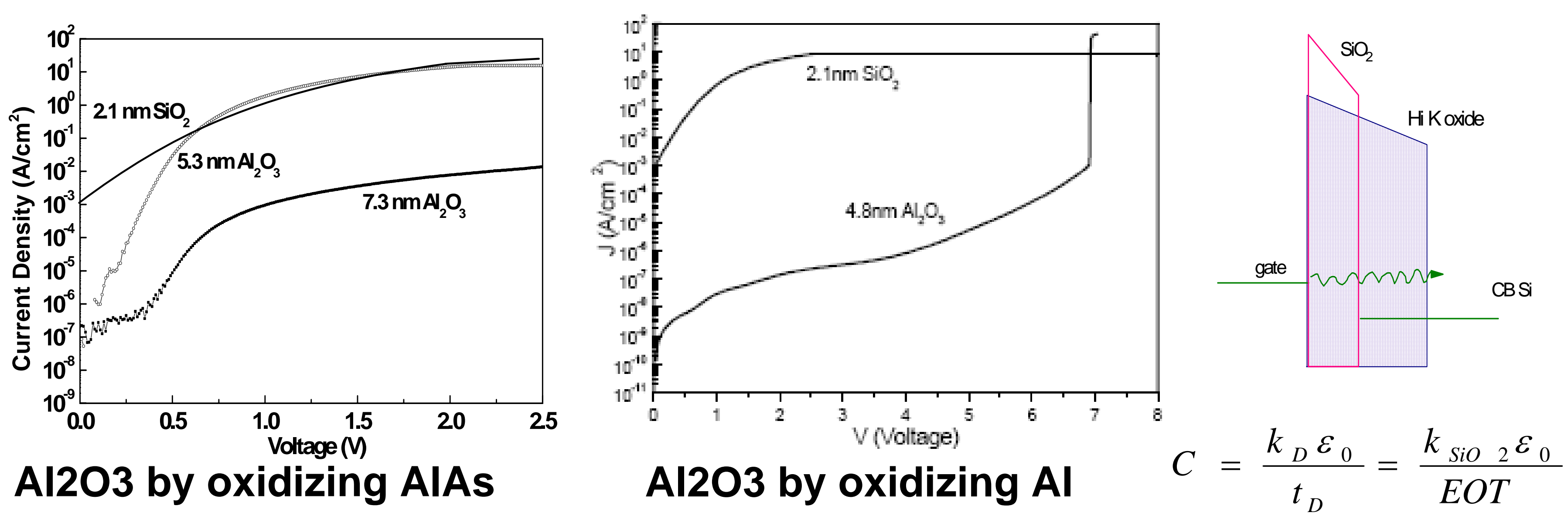


$$I_{D,sat} = C_{ox} W v_s (V_{GS} - V_{off} - E_c L_{G,eff})$$

$$C_{ox} = \frac{\varepsilon_d}{t_d} = \frac{k\varepsilon_0}{t_d}$$

A. Chin et al: IEEE EDL 1997.

From Ideal to Realization



Al2O3 by oxidizing AlAs

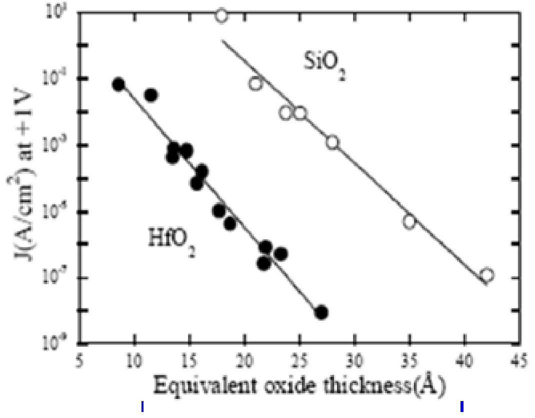
Al2O3 by oxidizing Al

$$C = \frac{k_D \varepsilon_0}{t_D} = \frac{k_{SiO_2} \varepsilon_0}{EOT}$$

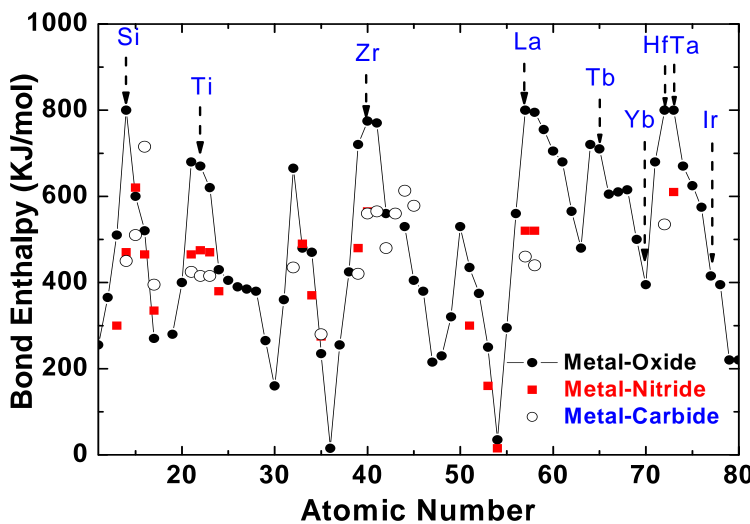
C. C. Liao, A. Chin, and C. Tsai, "Electrical Characterization of Al_2O_3 on Si from MBE-grown AlAs and Al ," 10th Int'l MBE Conf., August 1998.

A Chin, C. C. Liao, C. H. Lu, W. J. Chen1, and C. Tsai, "Device and Reliability of High-k Al_2O_3 Gate Dielectric with Good Mobility and Low D_{it}," *Symp. On VLSI* 1999.

Competition & Speed



"Ultrathin Hafnium Oxide with low leakage and excellent reliability for alternative gate dielectric application", ***IEDM*** **1999, UT-Austin (J. C. Lee's group).**



A Chin, Y. H. Wu, S. B. Chen, et al, "High Quality La_2O_3 and Al_2O_3 Gate Dielectrics with Equivalent Oxide Thickness 5-10Å", *Symp. On VLSI* 2000, (Highlight paper).

Citied by IBM (IEDM 2000)

80 nm poly-silicon gated n-FETs with ultra-thin Al_2O_3 gate dielectric for ULSI applications

D.A. Buchanan[1], E.P. Gusev[1], E. Cartier[1], H. Okorn-Schmidt[1], K. Rim[1], M.A. Gribelyuk[2], A. Mocuta[2], A. Ajmera[2], M. Copel[1], S. Guha[1], N. Bojarczuk[1], A. Callegari[1], C. D'Emic[1], P. Kozlowski[1], K. Chan[1], R. J. Fleming[2], P.C. Jamison[2], J. Brown[2], R. Arndt[2]

[1]IBM - Research, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights NY, U.S.A.

Acknowledgements

The authors would like to acknowledge S.L. Cohen for her assistance in enabling this work, M. Jussila, S. Haukka and M. Tuominen at ASM Microchemistry for supplying the Al_2O_3 films and the ASTC (IBM-Microelectronics) for the fabrication of the FETs.

References

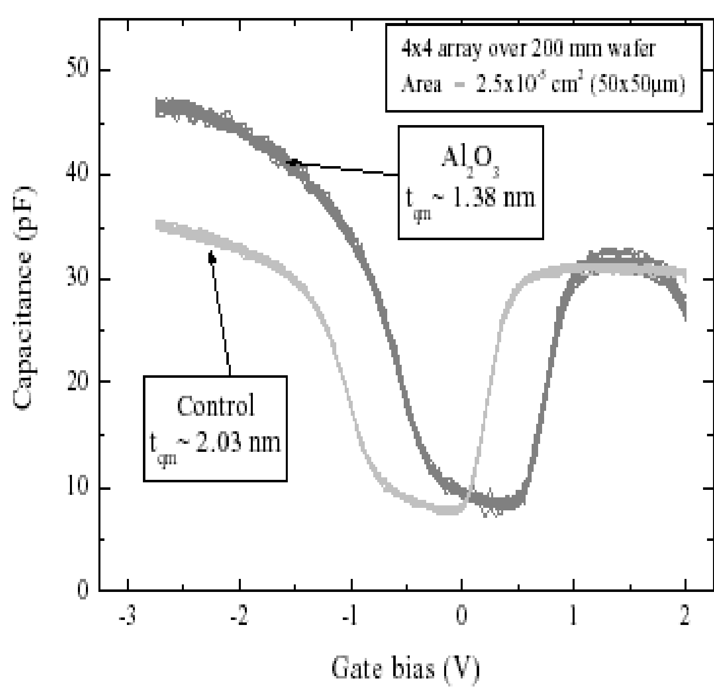
[1] A. Chin, C. C. Liao, C. H. Eu, W. J. Chen, and C.Tsai, "Device and Reliability of High-K Al_2O_3 Gate Dielectric with Good Mobility and Low D_{it}," *VLSI Symposium Technical Digest*, pp. 135-136, 1999.

[2] A. Chin, Y. H. Wu, S. B. Chen, C. C. Liao, and W. J. Chen, "High Quality La_2O_3 and Al_2O_3 Gate Dielectrics with Equivalent Thickness 5-10 A," *VLSI Symposium Technical Digest*, pp. 16-17, 2000.

[3] C. S. Hwang and H. J. Kim, "Deposition and characterization of ZrO_2 thin films on silicon substrate by MOCVD.," *J. Materials Res.*, vol. 8, pp. 1361, 1993.

[4] L. Kang, B. H. Lee, Wen-JieQi, YongjooJeon, ReneeNieh, SundarGopalan, KatsunoriOnishi, and JackC.Lee, "Electrical Characteristics of Highly Reliable Ultrathin Hafnium Oxide Gate Dielectric," *Electron Dev. Lett.* vol. 21, pp. 181-183, 2000.

Figure 1: High-resolution transmission electron micrograph (HRTEM) of a poly Si/Al_2O_3/silicon device.



Confirmed by Other Group (IEDM 2002)

Advanced Gate Dielectric Materials for Sub-100 nm CMOS

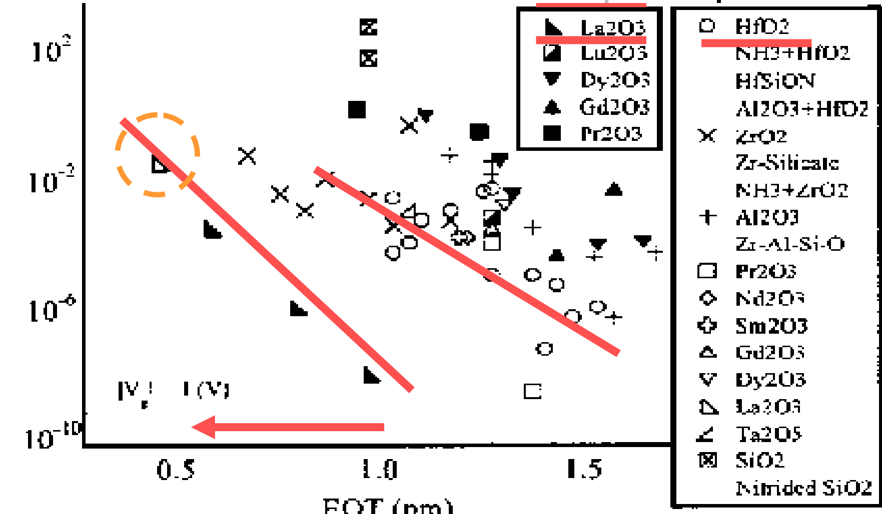
H. Iwai, S. Ohmi*, S. Akama, C. Ohshima, A. Kikuchi, I. Kashiwagi, J. Taguchi, H. Yamamoto, J. Tonotani, Y. Kim, I. Ueda, A. Kuriyama, and Y. Yoshihara

Frontier Collaborative Research Center, *Graduate School of Science and Engineering
Tokyo Institute of Technology

tests as shown in Fig. 11. However, fortunately, when the film was covered by the electrode, the moisture absorption was completely suppressed. The problem will be probably solved by in-situ deposition of the gate electrode and dry process. Fig. 12 shows the material dependence of the moisture absorption. It should be noted that the absorption

(1) B. Yu, H. Wang, A. Joshi, Q. Xiang, E. Ibok, and M.- R. Lin, "15 nm Gate Length Planar CMOS Transistor," IEDM Tech. Dig, Washington D.C., pp.937–939, 2001
(2) A. Chin, Y. H. Wu, S. B. Chen, C. C. Liao, and W. J. Chen, "High quality La_2O_3 and Al_2O_3 gate dielectrics with equivalent oxide thickness 5-10 A," Symp. on VLSI Tech, Dig. Tech., Honolulu, HI, pp.16-17, 2000
(3) S. Ohmi, C. Kobayashi, E. Tokumitsu, H. Ishiwara and H. Iwai, "Low Leakage La_2O_3 Gate Insulator Film with EOTs of 0.8-1.2 nm," Ext. Abs. SSDM, Tokyo, Japan, pp. 496-497, 2001

	La_2O_3	HfO_2
Interfacial layer formation	Not Significant	Yes
Micro-crystal formation	No @ 900 °C	Yes (> 700 °C)
Effective electron mobility (cm^2/V s)	300 @ 1 MV/cm	230 @ 1.5 MV/cm
Interface state density ($eV^{-1}cm^{-2}$)	3.0×10^{10}	8.0×10^{10}
Moisture absorption	Yes significant	Yes



Our pioneered La_2O_3 has potential to achieve EOT <1.0 nm for high-κ beyond HfO_2 (according to Hwai's paper @ IEDM 2002).

(previous IEEE ED president, Eber's Award owner)

Highly Cited Papers

Highly cited papers: top *1%* published papers in Engineering worldwide
http://scientific.thomson.com/isi/
Thomson-Reuters, including *ISI Web of knowledge*, *Science Citation Index* (*SCI*)

Reported by "The New York Times"

The New York Times

Bits

Business ▪ Innovation ▪ Technology ▪ Society

DECEMBER 15, 2008, 8:08 PM

For Chip Makers, Hybrids May Be a Way Forward

By JOHN MARKOFF

Searching for new ways to make computers that run faster and use less power, the chip industry is once again eyeing some exotic materials that can offer great speed, but have been more costly and difficult to manufacture than silicon.

"There are still very serious problems and many challenges, but it looks promising," said Jesus A. del Alamo, an electrical engineering professor who is working in the area and whose research is being partially funded by Intel.

One of the reasons that industry interest is so high is because of the rapidly growing power consumption of consumer gear.

"This is a green transistor," said Albert Chin, one of the organizers of the conference and a professor at National Chiao Tung University in Taiwan.

The researchers also talked about new research on three-dimensional chip structures as a way around the increasing challenges of making smaller microelectronic devices.

最新消息: 奈米國家型科技計畫 nano-taiwan.sinica.edu.tw/

This is also the reason why I became the IEDM Executive Committee Member.

Outline

1. 掌握趨勢

2. 如何擷取核心概念

-Go Back to Fundamentals

√ -Understanding the Problem

-Multi-Disciplinary Capability

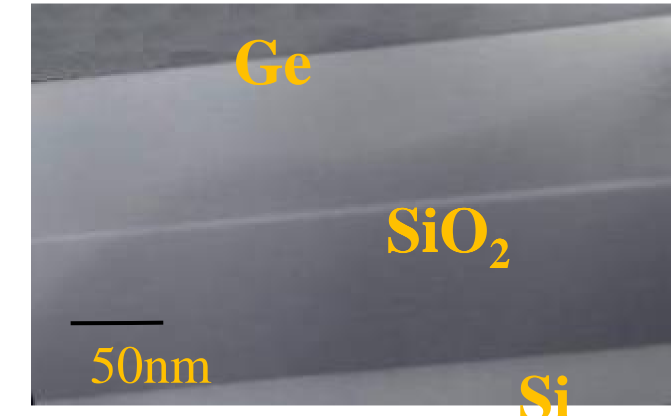
(Examples: nano-technology & RF)

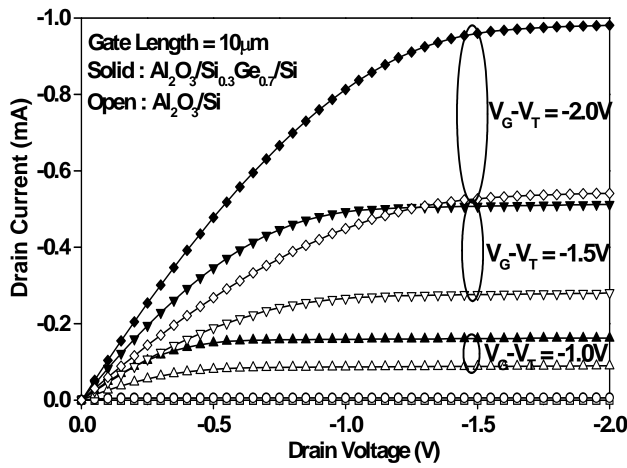
Understanding the Problem- Your Opportunity

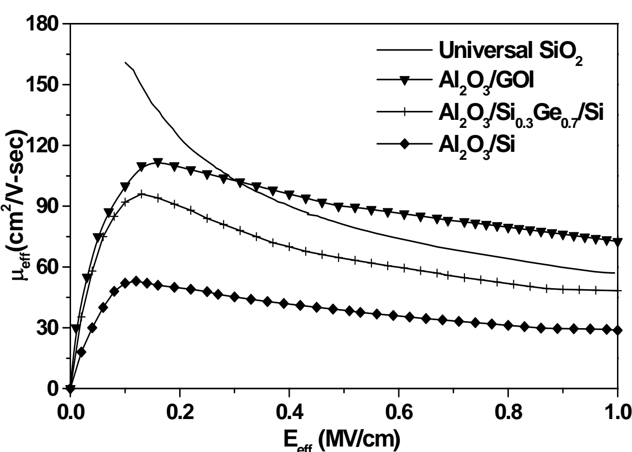
The challenge- always better performance

Scaling Beyond Si CMOS- Invention of GOI

$$I_{ds} = \frac{\mu_{eff} C_{ox} (W/L) \left[(V_g - V_t) V_{ds} - (m/2) V_{ds}^{\ 2} \right]}{1 + \left(\mu_{eff} V_{ds} / v_{sat} L \right)}$$







C. H. Huang, M. Y. Yang, A. Chin, W. J. Chen, C. X. Zhu, B. J. Cho, M.-F. Li, and D. L. Kwong, *Symp. on VLSI Technology,* pp. 119-120, 2003.

Cited by *International Technology Roadmap for Semiconductors (ITRS)*

Table 59a Single-gate Non-classical CMOS Technologies

Device	*Transport-enhanced FETs*	*Ultra-thin Body SOI FETs*		*Source/Drain Engineered FETs*	
	Strained Si, Ge, SiGe; buried oxide; Silicon Substrate	BOX	FD Si film; S; D; Ground Plane; BOX (<20nm); Bulk wafer	silicide; nFET; pFET; Silicon; Schottky barrier isolation	S; D; Non-overlapped region
Concept	Strained Si, Ge, SiGe, SiGeC or other semiconductor; on bulk or SOI	Fully depleted SOI with body thinner than 10 nm	Ultra-thin channel and localized ultra-thin BOX	Schottky source/drain	Non-overlapped S/D extensions on bulk, SOI, or DG devices
Application/Driver	HP CMOS	HP, LOP, and LSTP CMOS	HP, LOP, and LSTP CMOS	HP CMOS	HP, LOP, and LSTP CMOS
Advantages	▪ High mobility	▪ Improved subthreshold slope ▪ No floating body ▪ Potentially lower E_{eff}	▪ SOI-like structure on bulk ▪ Shallow junction by geometry ▪ Junction silicidation as on bulk ▪ Improved S-slope and SCE	▪ Low source/drain resistance	▪ Reduced SCE and DIBL ▪ Reduced parasitic gate capacitance
Particular Strength	▪ High mobility without change in device architecture	▪ Low diode leakage ▪ Low junction capacitance ▪ No significant change in design with respect to bulk	▪ Quasi-DG operation due to ground plane effect enabled by the ultra thin BOX ▪ Bulk compatible	▪ No need for abrupt S/D doping or activation	▪ Very low gate capacitance

Devices 7 … Francisco, … tors Grown … s," Applied … on/SiGe on … Technology … Technique," … l. 1, No. 4, … tics," VLSI … n.

T. Mizuno, "(110)-Surface Strained-SOI CMOS Devices with Higher Carrier Mobility," VLSI Technology Symposium (June 10-12, 2003), Kyoto, Japan.

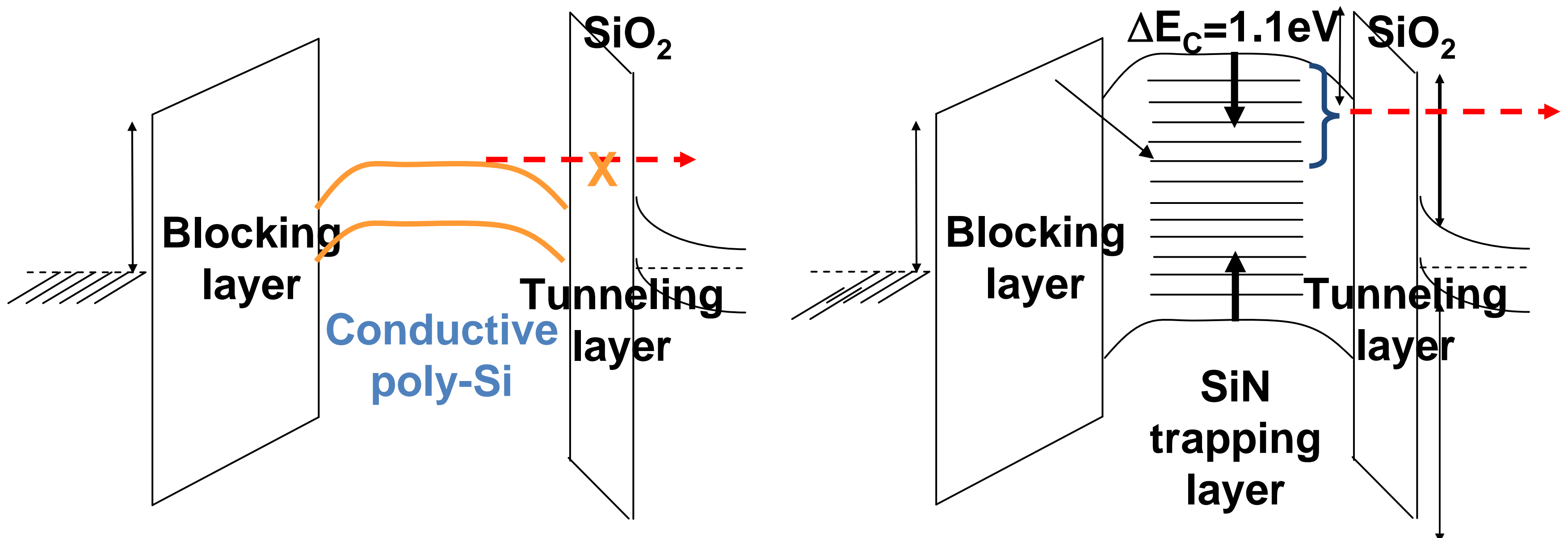
C.H. Huang, "Very Low Defects and High-performance Ge-On-Insulator p-MOSFETs with Al2O3 Gate Dielectrics," VLSI Technology Symposium (June 10-12, 2003), Kyoto, Japan.

Our paper published in *Symp. on VLSI* 2003, has been listed in ITRS roadmap. (first time of any invention from Taiwan's academic society)

Understanding the Problem- Your Opportunity

Challenges for Flash Non-Volatile Memory

Poly-Si floating gate flash **[Metal-gate]-SiO_2-Si_3N_4-SiO_2-Si (MONOS)**

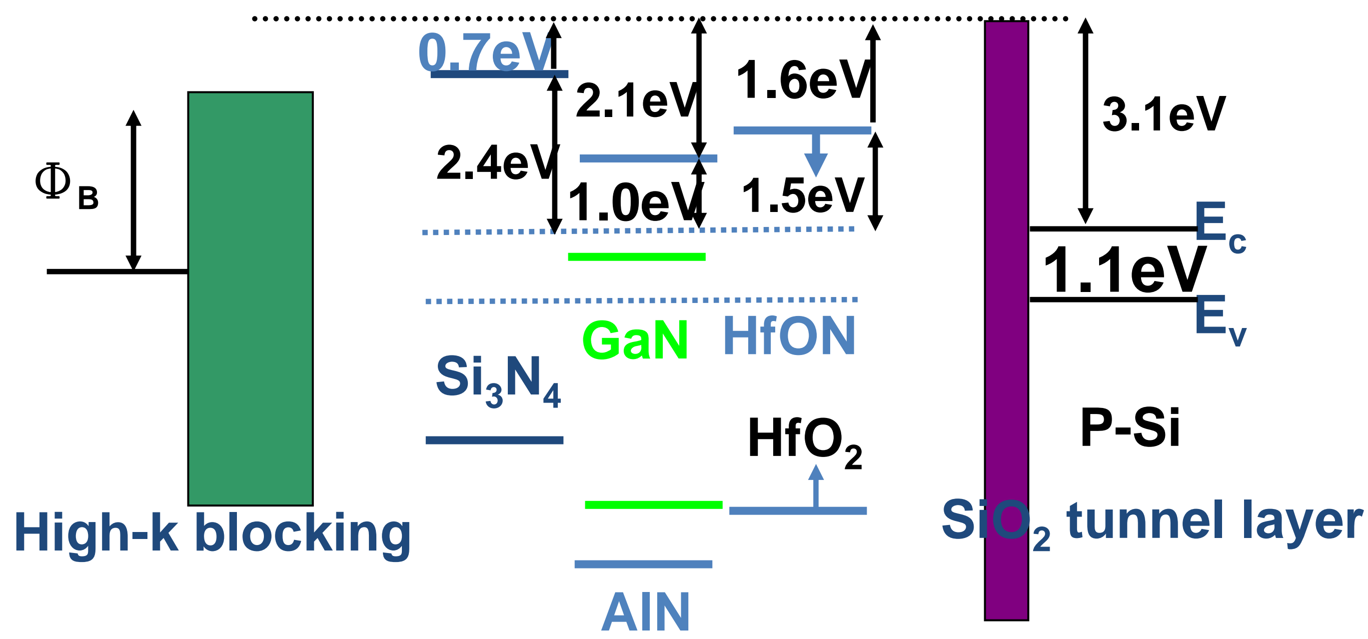


The charge storage flash has the lowest write current than other new type NVM, but still has power consumed by high voltage operation ~20V.

In conventional flash memory, all stored charges can leak out via a single oxide defect by conductive poly-Si, which can be overcome by using discrete 0D nitride traps in MONOS device.

The challenges are the small ΔE_C in Si_3N_4/SiO_2 and spread trap energy to cause charge leakage and erase saturation.

Go Back to Fundamentals



In standard MONOS NVM device, the small ΔE_C of 0.7 eV to SiO_2 will cause the stored charges to leak out by tunneling.

We pioneered the deep E_C high-k AlGaN trapping MONOS.

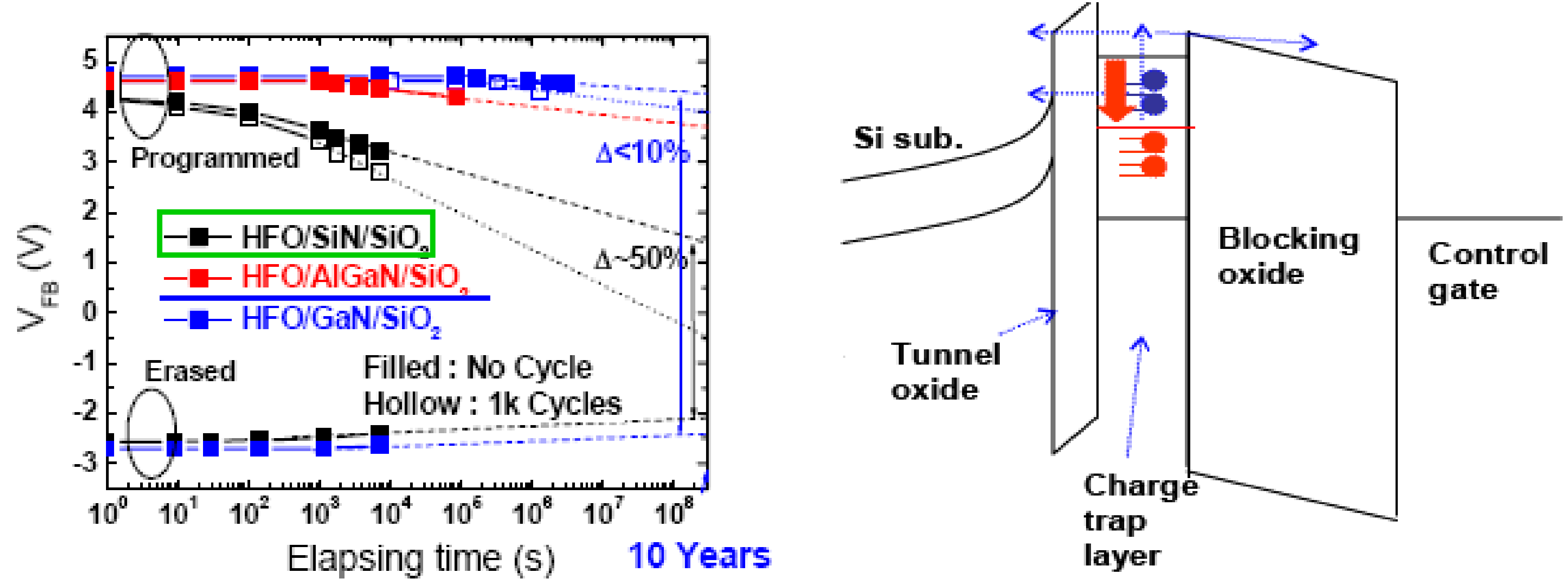
Further lowering write voltage is obtained using higher κ HfON with still large ΔE_C to barrier SiO_2.

K. C. Chiang et al, "Novel SiO_2/AlN/HfAlO/IrO_2 Memory with Fast Erase, Large ΔV_{th} and Good Retention," *Symp. on VLSI.* 2005.

A. Chin et al, "Low Voltage High Speed SiO_2/AlGaN/$AlLaO_3$/TaN Memory with Good Retention," *IEDM* 2005.

C. H. Lai et al, "Very Low Voltage SiO_2/HfON/HfAlO/TaN Memory with Fast Speed and Good Retention," *Symp. on VLSI* 2006.

Confirmed by Samsung



Our better performance Al(Ga)N and HfON MONOS reported in Symp. on VLSI 2005 & IEDM 2005 is also affirmed by Samsung's IEDM 2006 paper: >5X better retention than conventional SiN.

IEDM 2006, from Samsung

Invited Talks/Panelist in Major Devices Conf. in US, EU, ASIA

- Tutorial, *MRS*- Symposium G on Nonvolatile Memories, San Francisco, CA 2010.
- Invited talk, Samsung Electronics, 2009, 2003 (Exec. VP).
- Sub-Committee Chair, Asian Arrangement co-Chair, Chair *IEDM Exec. Committee*, 2008, 2009, 2010.
- Invited talk, 3D workshop (Stanford Univ), 2010.
- Invited talk, 16th Insulating Films on Semiconductors (*INFOS*), Cambridge UK, 2009.
- Invited talk, 7th Int'l Symp. on High κ Gate Stacks (*ISHGS*)- ECS, Vienna, Austria, 2009.
- Reported by "The New York Times" 「紐約時報」
- Invited talk, Int'l Solid-State Devices & Materials Conf. (*SSDM*), Japan, 2008.
- Invited talk, Int'l Symp. Advanced Gate Stack Tech. (*ISAGST*), TX USA, 2008.
- Invited talk, European Materials Research Society (*E-MRS*), 2006.
- Symposium organizer: 3rd Int'l Symp. on High κ Gate Stacks (*ISHGS*)- ECS, 2005. Panelist, New channel MOSFET workshop, SEMATECH, 2005.
- Invited talk, European Solid State Device Research Conf, (*ESSDERC*), 2005.
- Invited talk, Ge technology workshop, IMEC, 2005.
- Rump section panelist, 62nd Device Research Conference (*DRC*), 2004.
- Invited talk, International Electron Devices Meeting (*IEDM*), 2003.

Outline

1. 掌握趨勢

2. 如何擷取核心概念

-Go Back to Fundamentals

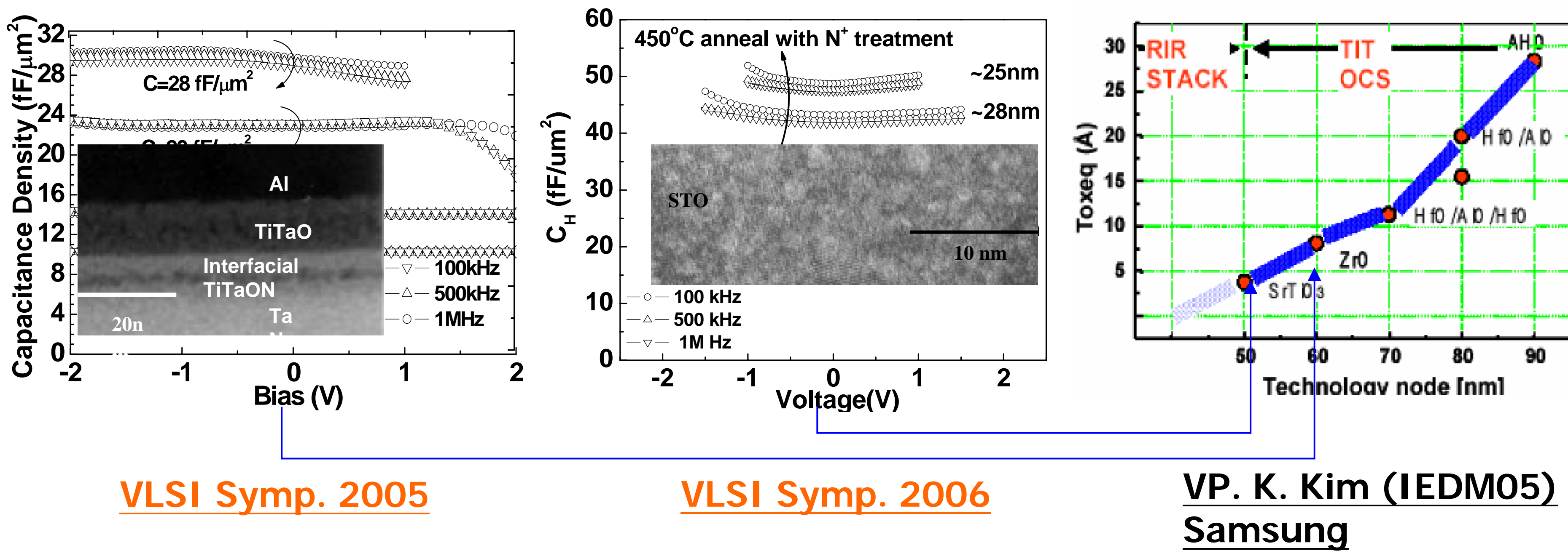
-Understanding the Problem

√ -Multi-Disciplinary Capability

(Examples: nano-technology & RF)

Multi-Disciplinary Capability

Applying the existing technology to other field (high-k CMOS to DRAM):
Our Embedded MIM Device in Samsung's Roadmap



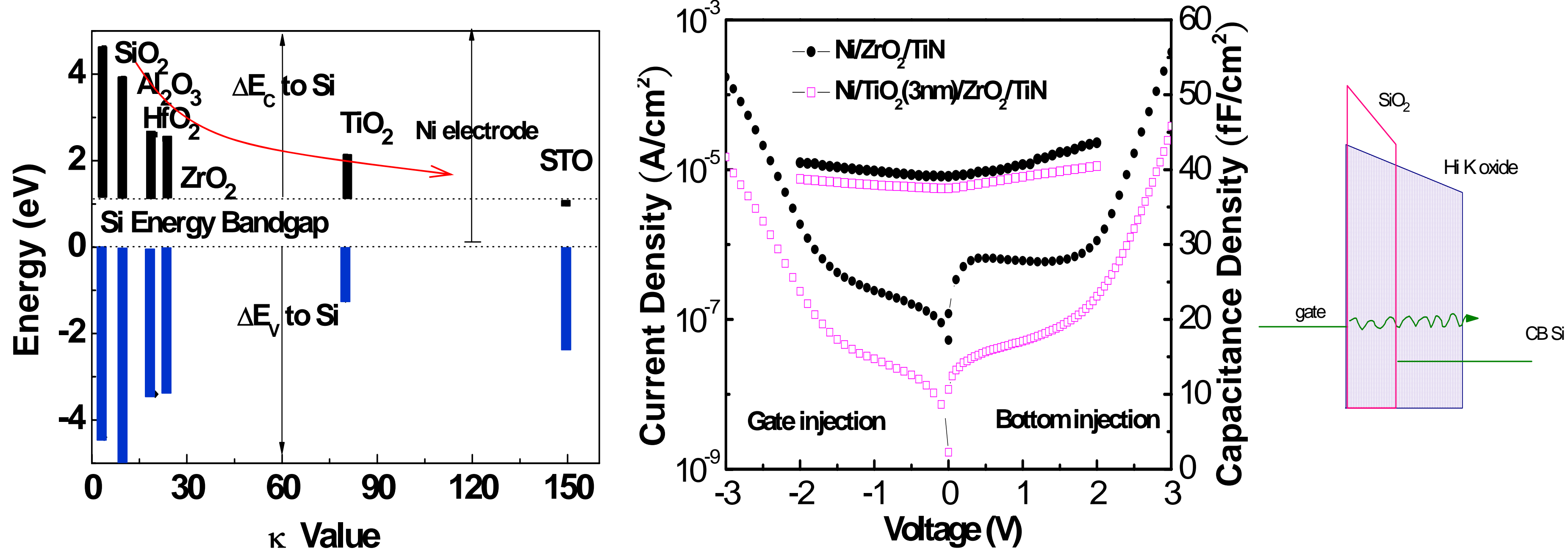
Our developed stacked DRAM & unified capacitor matches well the Samsung's DRAM technology roadmap:

HfO/AlO/HfO *IEDM* 2003: 70 nm node

TiTaO or TiHfO, *VLSI Symp.* 2005: 60 nm node

STO, *VLSI Symp.* 2006: 50 nm node

Understanding the Problem



To continue the scaling trend, higher C density ($\varepsilon_0\kappa/t_D$) using higher κ dielectric, low leakage current and low process temperature (<400°C) are needed according to ITRS, but the fast degraded ΔE_C and leakge current are the challenges.

The higher k ZrTiO has become industry standard for 40 nm node and below DRAM.

Currently, small 0.65 nm CET and low leakage were reached.

Citation

Our developed high-k capacitor cited by *ITRS* roadmap:

http://www.itrs.net/Links/2007ITRS/2007_Chapters/2007_Interconnect.pdf, p. 37, Linked information on Passives

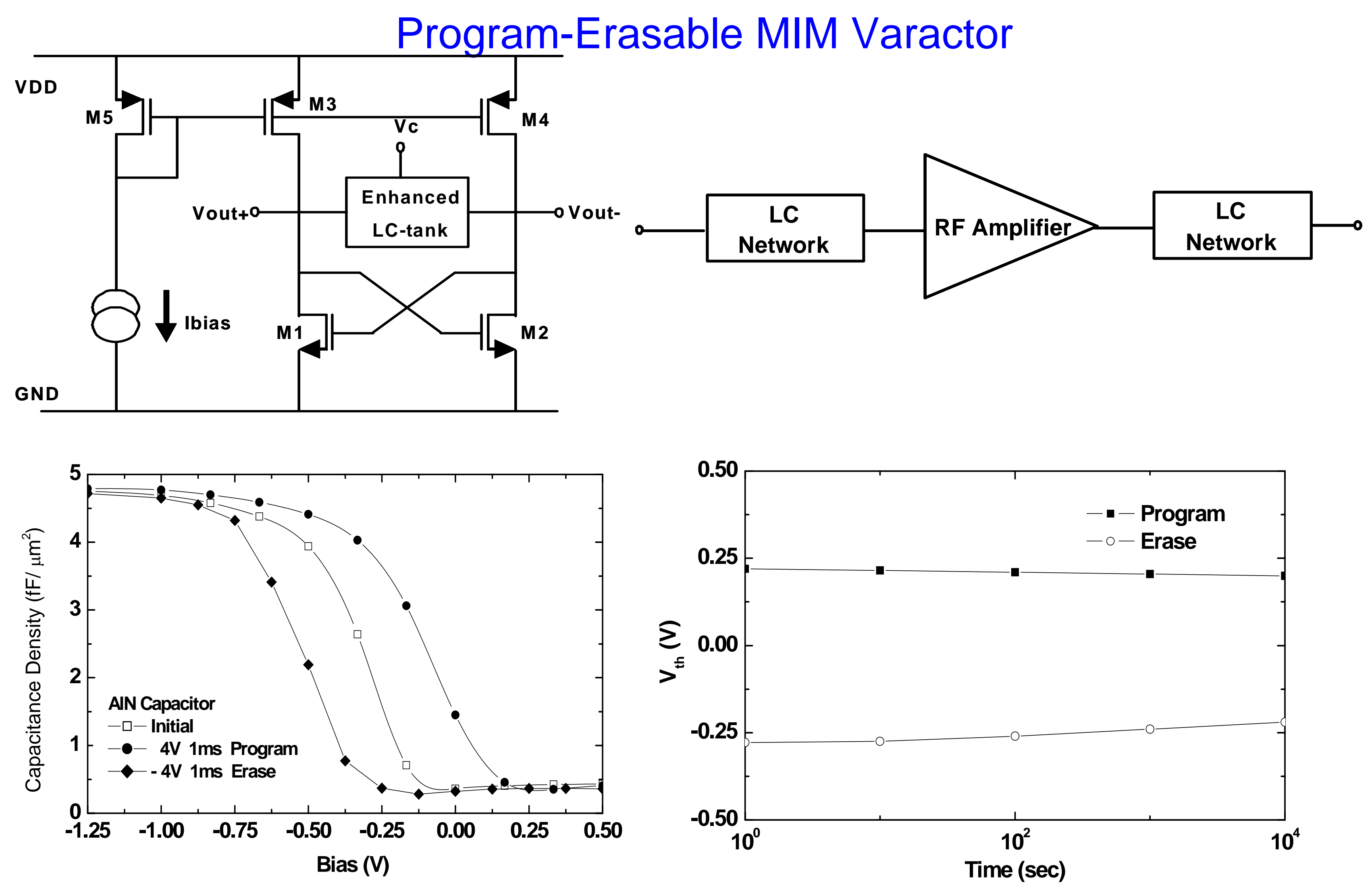
Several papers are published with promising data on the integration of interconnect compatible high k MIM dielectrics (e.g. Al_2O_3, Ta_2O_5, HfO_2, Nb_2O_5, TiTaO, $TiSiO_4$, TaZrO, BST, STO) [3, 20-24, 37, 38, 50-55]. The high k MIM dielectrics are deposited either by PVD followed by an appropriate anneal or by CVD and especially Atomic Layer CVD processes keeping the overall temperature budget typically below 400-450°C.

However, not all approaches with record breaking capacitance densities (> 40 fF/µm^2) may be useful from a leakage current, voltage- & temperature-linearity or dielectric reliability point of view. Recently laminated (multi-layered) films of different high k MIM dielectrics are proposed in order to overcome these problems [37, 39-41, 50]. By proper work-function tuning of the electrode material (i.e. replacing TaN by Ni) a significant reduction of the leakage current was observed for a MIM capacitor with STO high k dielectric [54].

[32] A. Chin, et al.; Digest 2003 IEDM, p. 375
[37] S.J. Kim, et al.; Digest 2005 VLSI Technology Symposium, p. 56
[38] K.C. Chiang, et al.; Digest 2005 VLSI Technology Symposium, p. 62
[39] H. Hu, et al.; Digest 2003 IEDM, p. 379
[50] S-J Kim, et al.; IEEE Electron Dev. Lett., Vol. 26, p. 625, 2005
[53] K.C. Chiang, et al.; Digest 2006 VLSI Technology Symposium, p. 126
[54] K.C. Chiang, et al.; IEEE Electron Dev. Lett., Vol. 28, p. 235, 2007

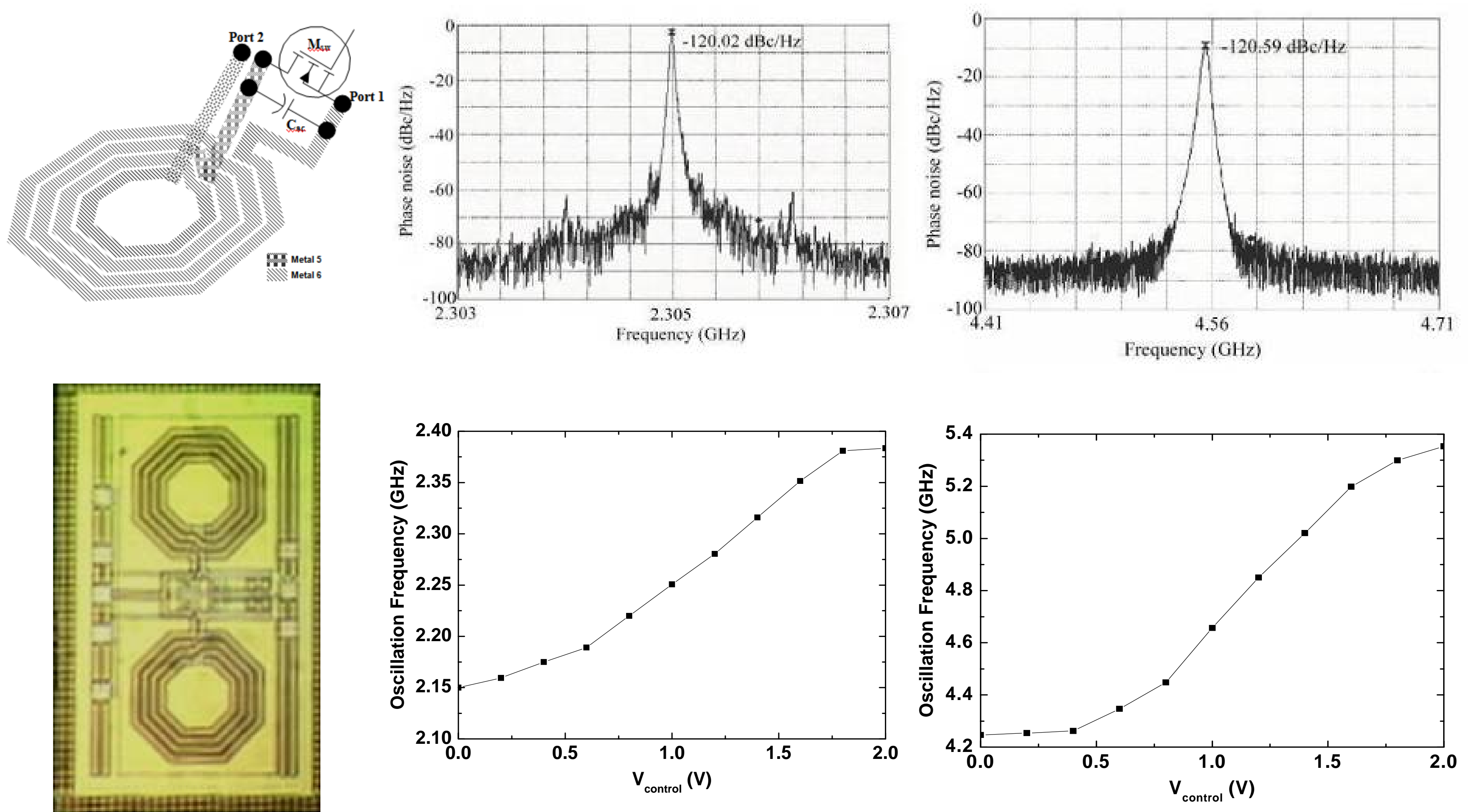
The Ni CVD has been developed for commercial DRAM/CMOS production.

Multi-Disciplinary Capability



***Intl. Microwave Symp.*, C. H. Lai *et al*, 2004 (NCTU).**

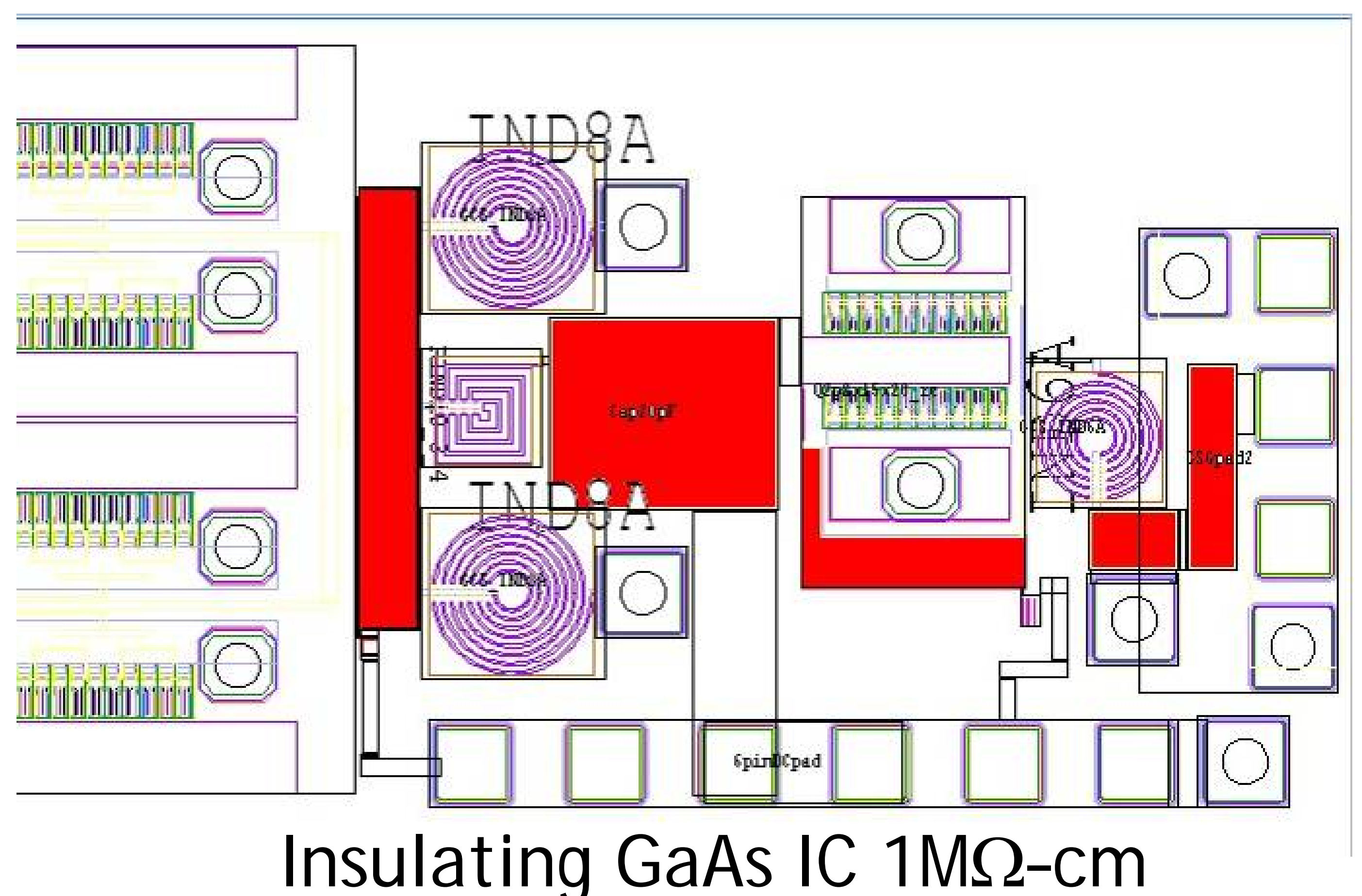
Dual Band VCO Using Passive RF Devices



Y. H. Kao et al, Int'l Microwave Symp. 2007.

Understanding the Problem

- The power consumption of Si RF IC on VLSI-standard substrate (10Ω-cm) is mainly in the low Q passive devices and poor power transistors.



Insulating GaAs IC 1MΩ-cm

Multi-Disciplinary Capability

Create traps in Si

E_C

E_V

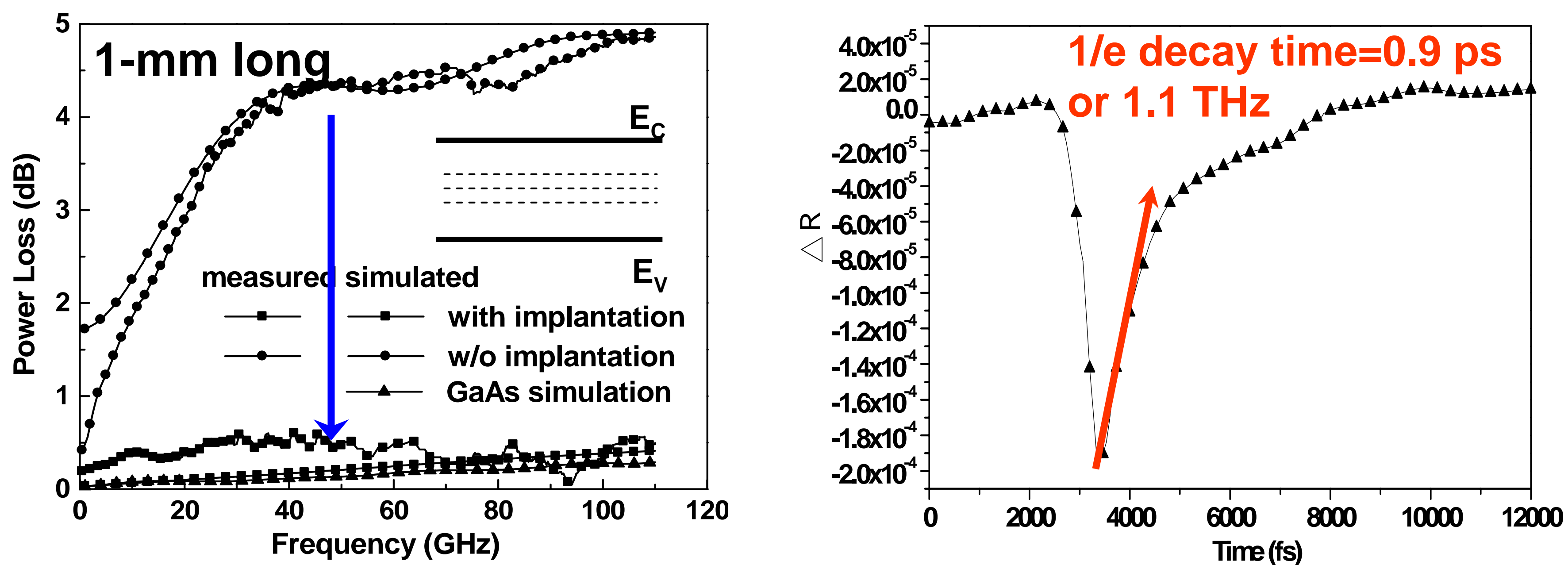
Substrate	SOQ	SOQ	Standard Si 10Ω-cm	Standard Si 10Ω-cm
Implantation type & dose (cm^{-2})	None	As^+ 10^{15}	Proton 10^{15}	Proton 10^{16}
Resistivity, (Ω-cm) As implanted	10	36,000	7,200	1.6×10^6
Resistivity, (Ω-cm) 400°C annealed	10	32,000	6,600	1.2×10^6

SOQ: Si-on-Quartz

Semi-insulating GaAs: ~10^7 Ω-cm

A. Chin et al, *Appl. Phys. Lett.*, vol. 69, no. 5, pp. 653-655, 1996.

Low Loss TML on Local Semi-Insulating Si

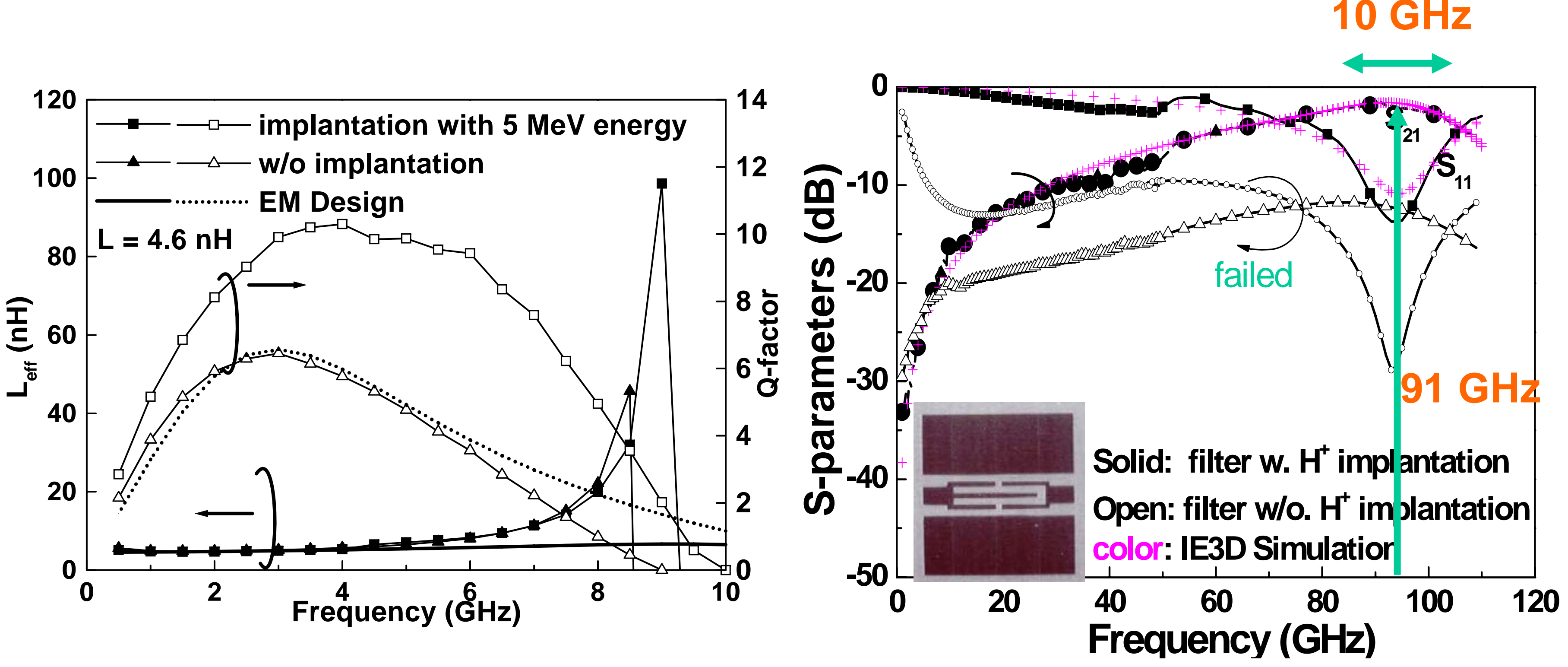


Using proton implantation to increase the resistivity of 10 Ω-cm into semi-insulating (10^6 Ω-cm), much improved RF loss to 110 GHz is obtained and close to GaAs.

The mechanism is due to high-density quantum traps similar to SONOS. The ultimate frequency of this technology is 1.1 THz.

57 **A. Chin, *et al.*; Digest 2003 IEDM, p. 375**

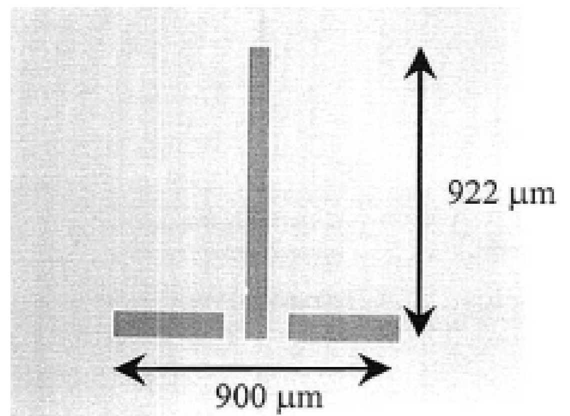
Improvement in Inductor & Filter

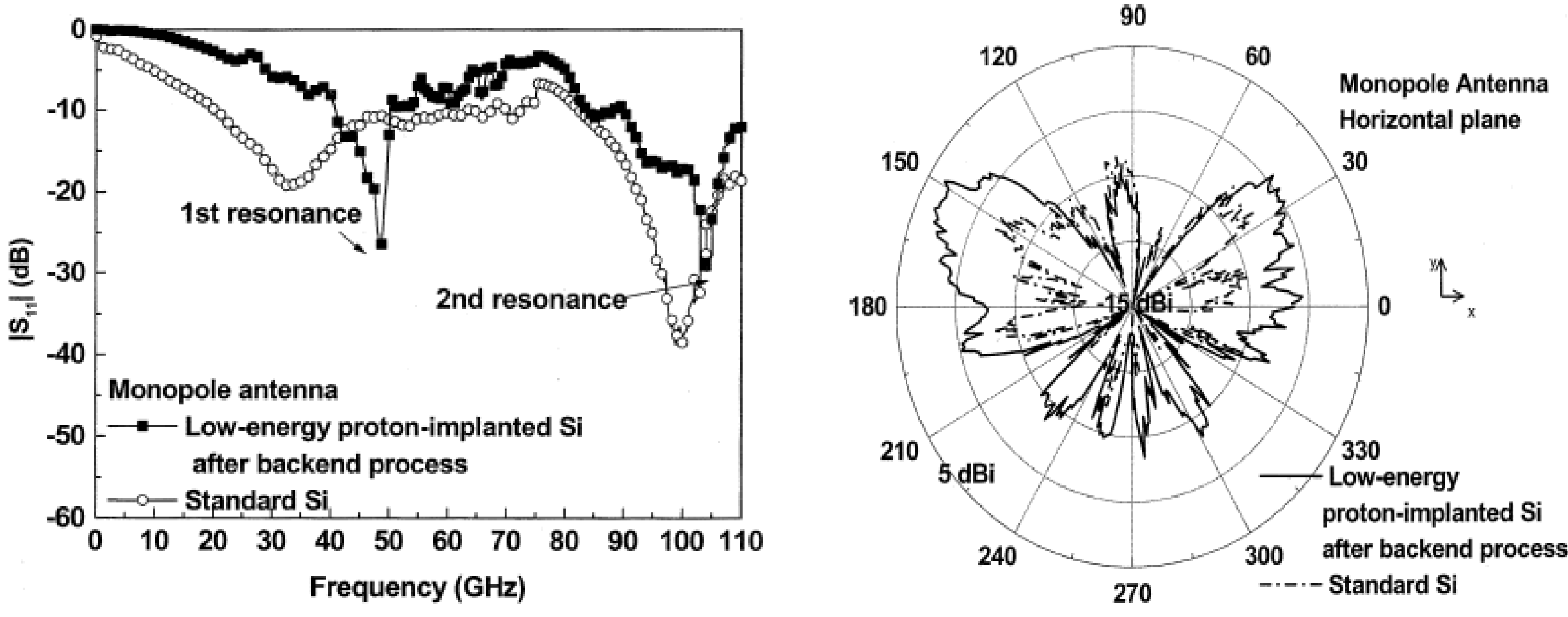


For L with H⁺ implant, Q-factor improves 60% with higher f_{SR}.

The filter w/o implant is failed. Using H⁺ implant, small 1.6 dB S_{21} insertion loss at 91 GHz and wide 10 GHz bandwidth are close to ideal EM-simulation (highest freq filter on Si).

Distributed Antenna & Inter-Chip Communication





K. T. Chan et al, IEEE MWCL.

Visibility & Job Connection

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2002畢業	C. L. Sun博士		中研院/National Research Council Canada
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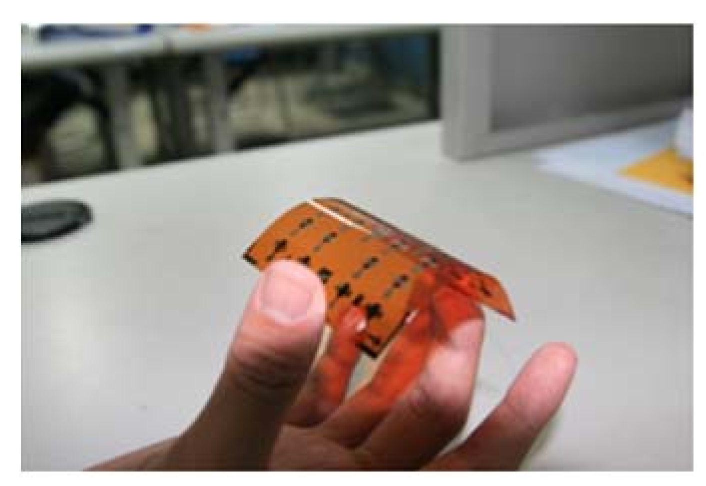
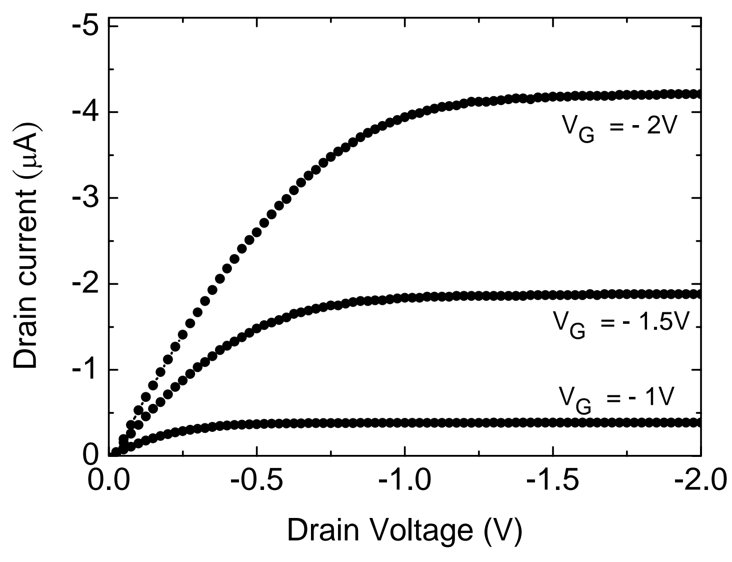
Organic Transistors

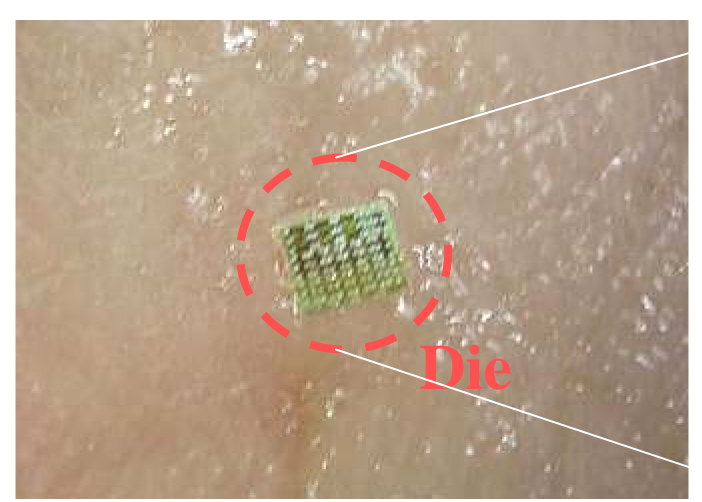


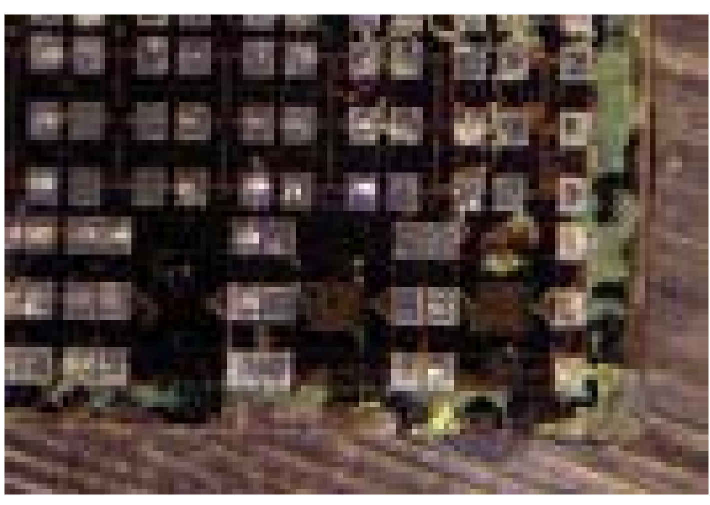


	HfLaO	LPCVD SiO_2	PECVD TEOS oxide	PECVD TEOS oxide
Gate dielectric	20 nm	80 nm [3]	60 nm [4]	40 nm [5]
Conduction channel	thermally evaporated pentacene	poly-Si by SPC	poly-Si by SPC	poly-Si by SPC
C_i (nF/cm^2)	950	43.1	57.5	86.3
V_T (V)	-1.3	5.6	8.14	Not extracted
μ_{FE} (cm^2/Vs)	0.71	20	12.44	3
SS (V/decade)	0.078	1.4	1.97	2.67
$\mu_{FE}C_i$ (nF/cm^2)	674.5	862.8	715.7	258.8
I_{on}/I_{off}	1.0×10^5	3.5×10^5	2.97×10^5	Not extracted

Record Best Organic Transistors, IEEE EDL, 2008.

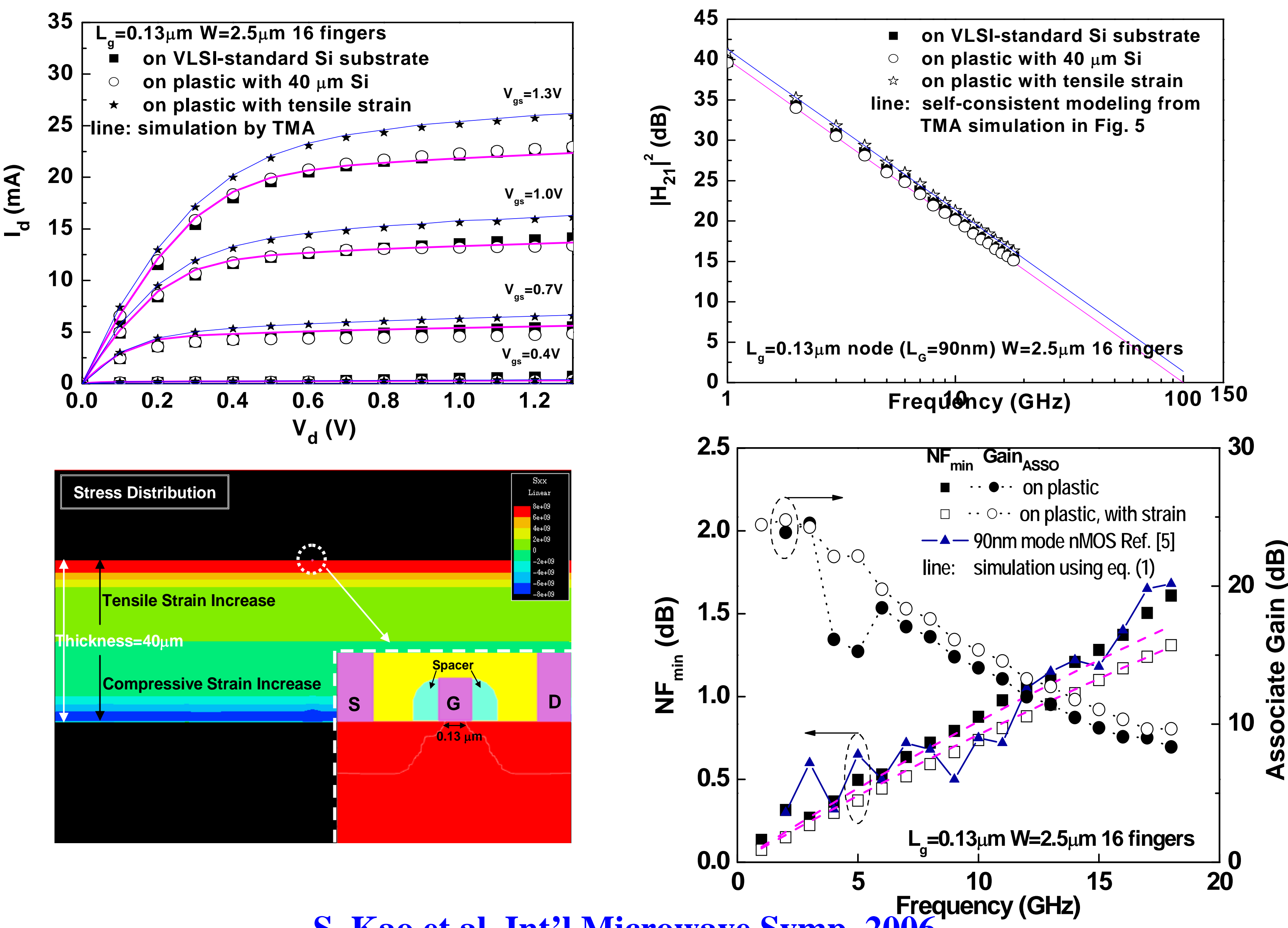
Flexible RF MOSFET on Plastic





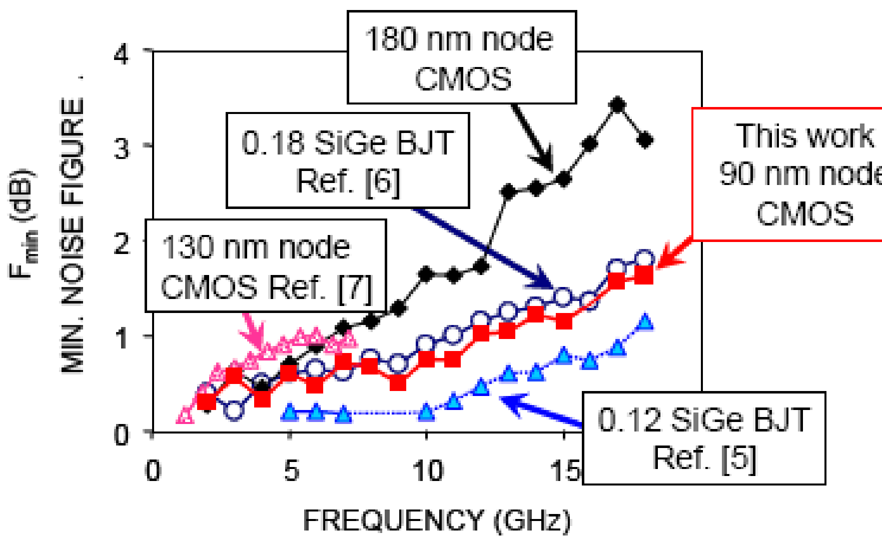
S. Kao et al, VLSI Symp. 2005, Novel device section

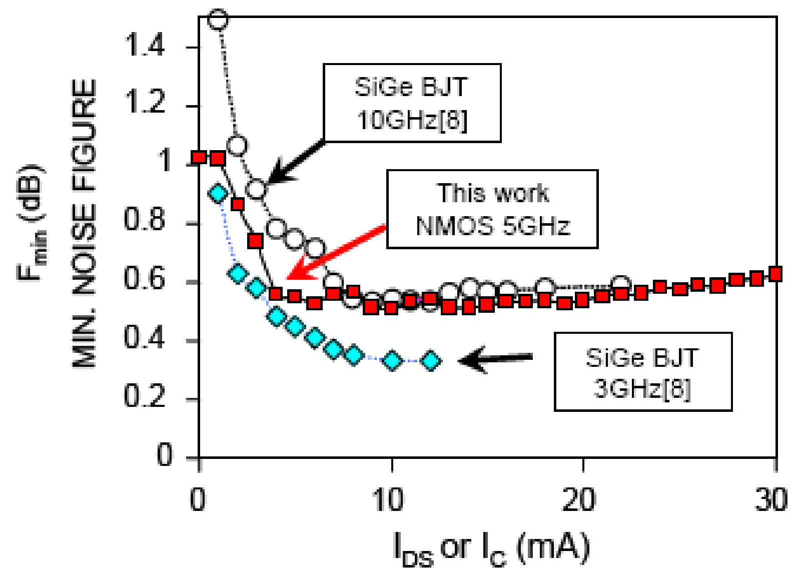
Flexible RF MOSFET on Plastic



S. Kao et al, Int'l Microwave Symp. 2006

Intel's Citation





[1] K. Kuhn et al., "A 90 nm communication technology featuring SiGe HBT transistors, RF CMOS, precision R-L-C RF elements and 1 μm^2 6-T SRAM cell," 2002 IEDM Digest, 8-11 Dec. 2002, pg. 73 -76.

[2] J.S. Rieh et al., "SiGe HBTs with cut-off frequency of 350 GHz" 2002 IEDM Digest, 8-11 Dec. 2002, pg. 771 -774.

[3] B. Jagannathan,et al., "Self-aligned site NPN transistors with 285 GHz f_{MAX} and 207 GHz f_T in a manufacturable technology," IEEE Electron Device Letters, IEEE, Vol. 23 No. 5, May 2002, pg. 258 -260.

[4] N. Zamdmer et al., "Suitability of scaled SOI CMOS for high frequency analog circuits," in Proc. ESSDERC 2002, to be published.

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[6] F. K. Chai, R. Reuter, T. Baker, D. Zupac, and J. Kirchgessner, "Outstanding noise characteristics of SiGe:C HBT allow flexibility in high-frequency RF design" IEEE RFIC Symposium, 8-10 June 2003, pg. 151 -154.

[7] C. H. Huang, et al., "The minimum noise figure and mechanism as scaling RF MOSFETs from 0.18 to 0.13 μm technology nodes," IEEE RFIC Symposium, 8-10 June 2003, pg. 373 – 376.

[8] D. Greenberg, et al., "Noise performance and considerations for integrated RF/analog/mixed-signal design in a high-performance SiGe BiCMOS technology" 2001 IEDM Digest, 2-5 Dec. 2001, pg. 22.1.1 - 22.1.4

K. Kuhn et al, Symp. On VLSI 2004. (Intel)

Summary

1. Hard working is useful, but not necessary leading to success.

2. Attending premier international conference is important for new ideas and direction.

3. Team work, group discussion, university-industry and international collaboration are essential for success.

4. Multi-disciplinary capability is the easy way to do high impact research.