High Work Function Ir_xSi Gates on HfAlON p-MOSFETs

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***Abstract*—We have fabricated the fully silicided Ir_xSi-gated p-MOSFETs on HfAlON gate dielectric with 1.7-nm equivalent oxide thickness. After 950 °C rapid thermal annealing, the fully Ir_xSi/HfAlON device has high effective work function of 4.9 eV, high peak hole mobility of 80 cm^2/V·s, and the advantage of being process compatible to the current VLSI fabrication line.**

***Index Terms*—HfAlON, IrSi, MOSFET.**

I. Introduction

METAL–gate/high-κ technology is required for future CMOS devices to reduce the gate leakage current and eliminate poly gate depletion [1]–[8]. However, one of the difficult challenges for metal–gate/high-κ MOS is the large threshold voltage (V_t) due to Fermi-level pinning. This is especially difficult for p-MOSFET [1], [6], since only Ni (5.15 eV), Ir (5.27 eV), and Pt (5.65 eV) in the periodic table [9] have work function close to the desired 5.2 eV used in conventional p^+ poly Si-gated p-MOS. Among them, the Ni-rich silicide (Ni_3Si) [7] or germanide [8] has reasonable high work function, but it is still needed to develop the Ir- or Pt-gated high-κ p-MOS due to the lowered effective work function $(\phi_{m,\text{eff}})$ by Fermi-level pinning. Unfortunately, large metal diffusion through high-κ dielectric was found to cause the CMOS devices failure [1], [10], [11]. To overcome this problem, in this letter we have used the robust HfAlON to reduce the metal diffusion through gate dielectric by adding high diffusion barrier Al_2O_3 and oxynitride [10]–[13] into HfO_2. Although the HfAlON has improved metal diffusion property, the Ir-gated HfAlON p-MOS still failed at temperature higher than 900 °C. To further improve the thermal stability, we have developed the Ir/Si-gated HfAlON p-MOSFET. After 950 °C rapid thermal annealing (RTA), the Ir_xSi/HfAlON p-MOS shows good device integrity of high $\phi_{m,\text{eff}}$ of 4.9 eV, small V_t of -0.1 V, and high hole mobility of 80 cm^2/Vs. These results are compatible with or better than the best reported metal–gate/high-κ p-MOSFETs [4].

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II. Experimental Procedure

N-type Si wafers with resistivity 1–10 Ω·cm were used in this study. After standard RCA clean, the HfAlO was deposited by plasma vapor deposition (PVD) followed by postdeposition anneal (PDA). The HfAlON was formed by applying NH_3 plasma surface nitridation on HfAlO and 800 °C PDA. Then ~25-nm amorphous Si and 60-nm Ir was deposited by PVD [14], [15], patterned and RTA annealed at 600–950 °C for 30 s to form the MOS capacitor. For comparison, Al-, Ir-, or TiIrN-gated devices on HfAlON or HfO_2 were also fabricated. The gate first p-MOSFET was fabricated by forming HfAlON, metal–gate deposition and patterning, Boron source/drain ion implantation at 25 keV, and activated at 950 °C RTA for 30 s. Note that this process is different from conventional salicide process, where the Ir_xSi was formed at the same time during RTA for ion implant activation. This can reduce the reaction of amorphous Si with high-κ dielectric to cause Fermi-level pinning, owing to the fast silicidation reaching to the Si/HfAlON interface in thin amorphous Si. The fabricated p-MOS devices were further characterized by *C–V* and *I–V* measurements.

III. Results and Discussion

Fig. 1(a) and (b) shows the *C–V* and *J–V* characteristics of different RTA temperature-annealed Ir_xSi/HfAlON, Ir/HfAlON, $TiN/Ti_{0.5}Ir_{0.5}N/HfO_2$, Ir_xSi/HfO_2, and control Al/HfAlON capacitors. We have chosen the Al-gated capacitor as a reference since the pure metal at low RTA temperature has little Fermi-level pinning on high-κ dielectric [5]. An equivalent oxide thickness (EOT) of ~1.7 nm is measured, while the shift of *C–V* curves with different gate electrodes are attributed to different work function. This is because the 800 °C PDA has already annealed out some defects and the Ir_xSi formation was also confirmed by X-ray diffraction (XRD) measurement. However, the Ir_xSi/HfO_2 device fails even after 800 °C RTA due to the reaction of amorphous-Si with HfO_2. The $TiN/Ti_{0.5}Ir_{0.5}N/HfO_2$ also fails at temperature higher than 800 °C that may be due to Ir diffusion into HfO_2. Thus, the using metal–nitride (IrN) is run out of solution to achieve both high work-function and good thermal stability. The thermal stability is largely improved to 900 °C by using HfAlON instead of HfO_2 even for Ir-gated capacitor, but still failed at higher temperature. The adding of additional ~25-nm amorphous Si to form the Ir_xSi on HfAlON

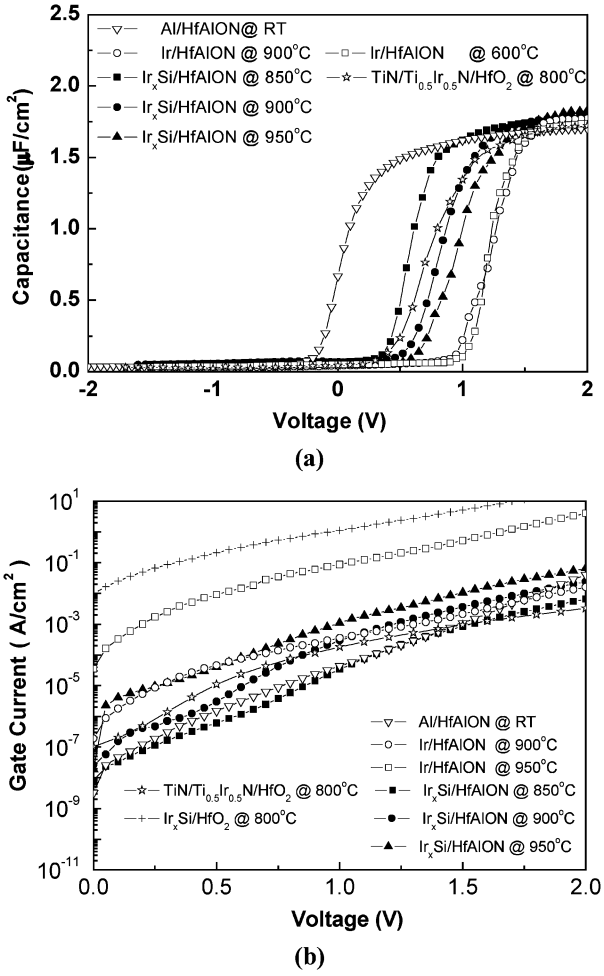

Fig. 1. (a) C–V and (b) J_g–V_g characteristics of Ir_xSi/HfAlON, Ir/HfAlON, Al/HfAlON, $TiN/Ti_{0.5}Ir_{0.5}N/HfO_2$,, and Ir_xSi/HfO_2 capacitors measured under accumulation. The device area is 100×100 μm.

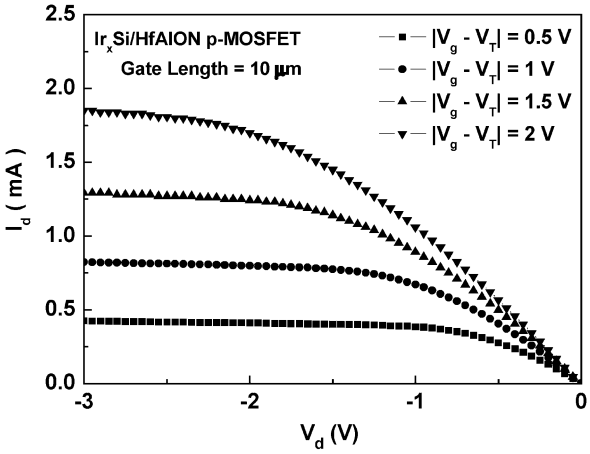

Fig. 2. I_d–V_d characteristics of Ir_xSi/HfAlON p-MOSFET. The gate length is 10 μm.

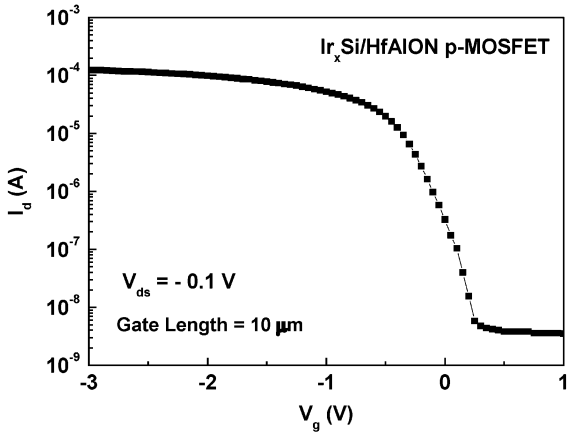

Fig. 3. I_d–V_g characteristics of Ir_xSi/HfAlON p-MOSFETs. The gate length is 10 μm.

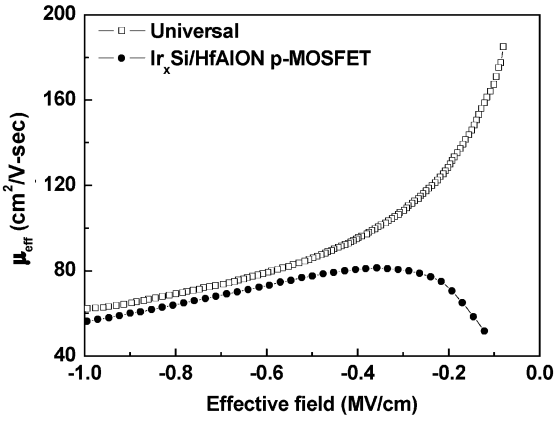

Fig. 4. Extracted hole mobility from I_d–V_d characteristics of Ir_xSi/HfAlON p-MOSFET.

can further improve the thermal stability to 950 °C with a reasonable leakage current. The increasing flat band voltage $(V_{\rm fb})$ with increasing RTA temperature of Ir_xSi/HfAlON capacitors may be due to more Ir diffusion toward HfAlON surface to increase the work function. However, the better thermal stability of Ir_xSi/HfAlON than Ir/HfAlON is traded by the lower work function. From C–V shift to Al control gate, the extracted $\phi_{m,\rm eff}$ of Ir_xSi/HfAlON and Ir/HfAlON are 4.9 and 5.3 eV, respectively. Therefore, good thermal stability of 950 °C RTA, reasonable high $\phi_{m,\rm eff}$ of 4.9 eV, and low gate dielectric leakage current can be simultaneously achieved in Ir_xSi/HfAlON MOS capacitors. It is important to note that although the $V_{\rm fb}$ tuning can also be obtained by dopant diffusion in FUSI/SiON, this method becomes less effective in high-κ metal–oxide due to the stronger interface reaction.

Fig. 2 shows the transistor I_d-V_d characteristics as a function of V_g–V_t for 950 °C RTA annealed Ir_xSi/HfAlON p-MOSFETs. The well-behaved I_d–V_d curves of Ir_xSi/HfAlON shows little device performance degradation using Ir_xSi gate.

Fig. 3 shows the I_d–V_g characteristics of Ir_xSi-gated p-MOSFETs with HfAlON film as the gate dielectric. A $V_{\rm th}$ as low as -0.1 V is obtained from the linear I_d–V_g plot, which is consistent with the large $\phi_{m,\rm eff}$ of 4.9 eV from C–V curves.

Fig. 4 shows the extracted hole motility versus gate electric field from measured I_d–V_g curves of p-MOSFETs. High hole mobility of 80 and 57 $cm^2/V{\cdot}s$ is obtained at peak value and 1 MV/cm effective field for Ir_xSi/HfAlON p-MOSFETs, respectively. This result also suggests low Ir diffusion through HfAlON even though excess Ir must be used to avoid unreacted amorphous Si and prevent gate depletion or Fermi lever pinning.

This indicates the successful integration of Ir_xSi on HfAlON p-MOSFETs with advantage of process compatible to current VLSI line.

IV. Conclusion

Good device performance of Ir_xSi/HfAlON p-MOSFET is shown by the high $\phi_{m,\mathrm{eff}}$, good thermal stability, and hole mobility close to universal mobility values with additional merit of process compatible to current VLSI line.

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