Computational Statistics Approach to Capacitance Sensitivity Analysis and Gate Delay Time Minimization of TFT-LCDs

Yiming Li and Hsuan-Ming Huang

Abstract In this paper, we practically implement a systematical method for thin-film transistor liquid-crystal display (TFT-LCD) design optimization and sensitivity analysis. Based upon a three-dimensional (3D) field solver and a Design of Experiments, we construct a second-order response surface model (RSM) to examine the capacitances' effect on the performance of an interested TFT-LCD pixel. The constructed RSMs are reduced using a step-wise regression. We verify the accuracy using the normal residual plots and their residual of squares. According to the models, we then analyze the sensitivity of the capacitances by considering the design parameters as changing factors (i.e., the size variation and the position shift) under an assumption of Gaussian distribution. Consequently, we further apply the models to optimize the designed circuit. The designing parameters of these models are selected and optimized to fit the designing target of the examined circuit by the genetic algorithm in our unified optimization framework. This computational statistics method predicts the capacitances' effects on the gate delay time and compares with full 3D simulation approaches, it shows the engineering practicability in display panel industry.

1 Introduction

Thin film transistors (TFTs) have found wide usage in active matrix liquid crystal displays [13]. The basic principle of operation of the liquid-crystal display (LCD) panel is to control the transparency of each pixel portion by bus lines to charge the pixel electrode. To obtain high display performance, the capacitance of each pixel plays very important role in display circuit design. However, the capacitance of a pixel is very hard to be analyzed in a computationally efficient way because of the three-dimensional (3D) complex geometry structure. In this paper, we complete a

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J. Roos and Luis R.J. Costa (eds.), *Scientific Computing in Electrical Engineering SCEE 2008*, Mathematics in Industry 14, DOI 10.1007/978-3-642-12294-1_30,

systematical method to analyze and optimize the capacitance of an interested TFT device, shown in Fig. 1, using a 3D technology computer aided design (TCAD) filed simulation [6], a computational statistic method and a genetic algorithm (GA). Figure 1(a) shows the equivalent circuit of TFT-LCD panel, which has 1280 × 1024

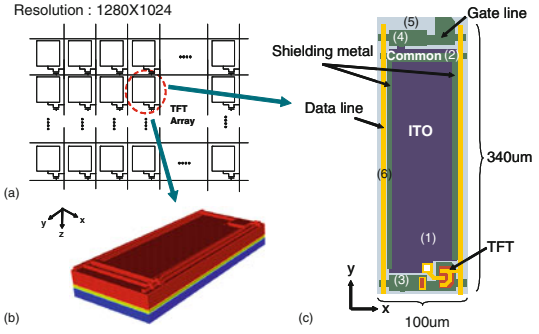

Fig. 1: a Equivalent circuit of TFT-LCD panel **b** 3D schematic plot of the TFT-LCD pixel **c** and perspective plot of the TFT-LCD pixel

Table 1: The upper and lower limits of the TFT-LCD designing parameters

Variable	Parameters	Variation range (μm)
	Size variation	
A	Gate line	[0,10] in y
B	Shield metal (left)	[0,3] in x
C	Shield metal (right)	[0,3] in x
D	Data line	[0,3] in x
E	ITO electrode	[0,5] in x
F	ITO electrode	[0,5] in y
	Position shift	
G	Shield metal (left)	[0,5] in x
H	Shield metal (right)	[-5,0] in x
I	ITO electrode	[-2,2] in y

resolution. The 3D schematic plot of the pixel in this panel, which has twelve layers, is shown in Fig.1(b) and the perspective plot is shown in Fig. 1(c). A computational statistics methodology is developed and implemented which consists of a Design of Experiment (DOE) setup and a second-order response surface model (RSM). By considering the designing parameters as changing factors (i.e., the size variation and the position shift), listed in Tab. 1, according to the DOE, we construct a RSM for the capacitances of TFT-LCD. Designing parameters such as the gate line, the shield metal, the data line and the ITO electrode are corresponding to the parts (4), (2), (6) and (1) as shown in Fig. 1(c), respectively. The RSM can explain the behavior of

capacitances on the investigated TFT-LCD pixel. We simplify the RSMs using a step-wise regression, and verify their accuracy by the residual of squares. Under a Gaussian distribution, the model allows us to analyze the sensitivity of capacitances in a TFT-LCD pixel with respect to the aforementioned factors efficiently. These models also enable us to optimize the designing targets of the tested TFT-LCD pixel.

The paper is organized as follows. In Sec. 2, we briefly describe the computational statistics approach for the structural analysis and design optimization of TFT-LCDs. In Sec. 3, the simulation results are discussed. Finally, we draw conclusions and suggest future work.

2 Computational Methodology

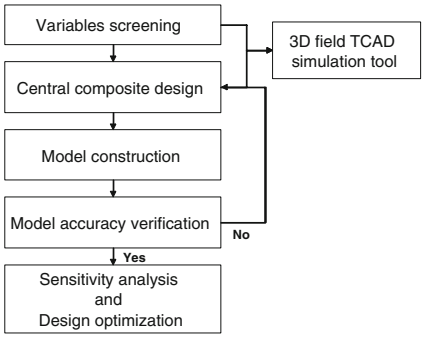

Fig. 2: A flowchart of the computational method

The computational statistics methodology that can be used to account for the characteristic sensitivity and circuit design optimization is depicted in Fig. 2. Variables selection is a procedure to find the significant factors from a list of many potential candidates. Alternatively, we use a screening design or empirical check to identify significant main effects, rather than interaction effects, the latter being assumed an order of magnitude less important. A Plackett-Burman [5, 12] design was used to determine major contrasts and interactions. Based on the results of the screening experiment, parameters in need of further study were identified. With a Central Composite Design (CCD) DOE technique, a 3D field TCAD simulation [6] is performed to calculate the passive components of the studied TFT-LCD structure. From this we constructed the RSM [2,5,7,11]; mathematically, the response surface models can be represented as second-order polynomials:

$$Y = \beta_0 + \sum_{i=1}^{k} \beta_i x_i + \sum_{i=1}^{k} \beta_{ii} x_i^2 + \sum_{i=1}^{k} \sum_{i \neq j}^{k} \beta_{ij} x_i x_j + \varepsilon, \tag{1}$$

where k is the number of input factors, x_i is the ith input factor, β_i is the ith regression coefficient, and ε represents model error. Several techniques, such as normality assumption and plot of residuals versus predicted value, to verify the adequacy of the RSM are then used [1–4, 11]. For the investigated structure, a 2^{nd} order model is established between capacitances (i.e., responses) and design parameters (i.e., factors). We notice that we didn't include scaling before the modelling. The details of the variables selection, the central composite design and the response surface model construction can be found in the reference [8].

Next, the sensitivity of the capacitances as approximately modeled by the RSM can be explored through a random procedure of statistics accordingly. Based upon our unified optimization framework (UOF) [9], we further develop a genetic algorithm (GA) [10] technique for the circuit design optimization. The flow of the GA evolutionary architecture is as follows. First, gene encoding is the way to encode the parameters into genes on the chromosome. Next step is to evaluate the fitness of each individual according to the stopping criteria. Then we select better chromosomes and breed a new generation through crossover and mutation. Finally, the fitness of the new generation is evaluated and the process is repeated for a specified number of generations or until achieving to desired targets. In the circuit design of TFT-LCD pixel, the capacitances in the SPICE netlist are encoded as optimization variables, and the fitness functions are constructed using an interested circuit performance. Here, the gate delay time of the studied whole display panel, shown in Fig. 1(a), is minimized. The designing parameters of RSMs for the capacitances that we have constructed are used to optimize the gate delay time of all TFT-LCD pixels in this study.

3 Results and Discussion

Among various designing parameters, variables screening has resulted in nine important factors as listed in Tab. 1. The table also shows the upper and lower limits of these designing parameters. We construct the 2nd order RSM using 149 runs with the CCD for the ten capacitances in a TFT-LCD pixel. We have constructed ten response surface models for different capacitances. Without loss of generality, here, we merely list two models for the most important capacitances C_{12} and C_{15}, which are the capacitance between the part (1) and the part (2) and the capacitance between the part (1) and the part (5), as shown in Fig. 1(c), respectively.

$$\begin{aligned}\log \mathbf{C_{12}} = {} & +2.57101 + 0.021036 \cdot B + 0.025445 \cdot C + 0.051072 \cdot E \\ & -0.10289 \cdot F - 0.021547 \cdot G + 0.022297 \cdot H - 0.025643 \cdot I \\ & +0.019341 \cdot E \cdot F + 3.46849 \cdot 10^{-3} \cdot E \cdot G - 5.22133 \cdot 10^{-3} \cdot E \cdot H \\ & +0.012046 \cdot E \cdot I - 4.20268 \cdot 10^{-3} \cdot F \cdot G + 3.78314 \cdot 10^{-3} \cdot F \cdot H \\ & +9.85079 \cdot 10^{-3} \cdot F \cdot I, \end{aligned} \tag{2}$$

and

$$\begin{aligned}\mathbf{1}/\sqrt{\mathbf{C_{15}}} = &+0.058861 + 1.16740 \cdot 10^{-4} \cdot B + 1.23106 \cdot 10^{-4} \cdot C \\ &-6.42761 \cdot 10^{-4} \cdot E + 9.38689 \cdot 10^{-4} \cdot F + 5.39816 \cdot 10^{-5} \cdot G \\ &-5.16325 \cdot 10^{-5} \cdot H - 2.69947 \cdot 10^{-5} \cdot I, \end{aligned} \tag{3}$$

where A to I are designing parameters as listed in Tab. 1. The residual of squares for the formulated C_{12} and C_{15} are 0.9141 and 0.9887, the others are listed in Tab. 2. Figure 3 shows the residual normal probability plot and the residuals versus the

Table 2: R-square of the constructed capacitance models

Response	R-Square	Response	R-Square
C_{12}	0.9141	C_{14}	0.9999
C_{15}	0.9887	C_{13}	0.9993
C_{56}	0.9939	C_{26}	0.9849
C_{35}	0.9976	C_{46}	0.9999
C_{16}	0.9823	C_{24}	0.9807

predicted plot for the capacitance $\log \mathbf{C_{12}}$, and Fig. 4 shows the model adequacy checking for $\mathbf{1}/\sqrt{\mathbf{C_{15}}}$. This examination highly reflects the modelling functionality for the RSM of these capacitances. The scatter plots of values calculated from the response surface models versus the simulated values obtained from the 3D field TCAD simulator for the models of these two capacitances, as shown in Fig. 5. The results show that there is a high linearity between the actual and predicted values. This confirms the accuracy of the constructed models. Figure 6(a) shows relationship between C_{12} and ITO size variation along the y direction (i.e., the parameter F), given in Tab. 1, where the other parameters are set to the nominal values, and under Gaussian distribution (with more than 10000 trails and 3σ, practically determined by the process variation, is about $0.25\,\mu$m). The standard deviation of the C_{12} and C_{15} due to the variation of the parameter F of the tested pixel TFT-LCD is shown in Fig. 6(b). The sensitivity analysis between the C_{15} and the parameter F is depicted in Fig. 7. It is found that 1.7385 fF increase of σC_{12} and 0.2157 fF of σC_{15} when the ITO size varies from $4\,\mu$m to $1\,\mu$m. The increase of σC_{12} and σC_{15} are mainly due to relatively large variations of the circuit performance when the ITO size variance decreases in the y direction. Besides, to the other designing parameters in this TFT-LCD pixel sensitivity analysis can be performed by exploiting the RSMs. The gate delay is one of the most significantly limiting factors for the large-screen-size and high-resolution TFT-LCD design. We successfully reduce the gate delay time from 2877.1 ns to 8.2289 ns by the GA on the platform of UOF. The optimized designing parameters of the whole display panel are listed in Tab. 3. We notice that this estimation should be subject to further investigation by individually constructing RSMs with respect to each TFT-LCD pixel. Therefore, the individual behavior can be further examined for this TFT-LCD pixel.

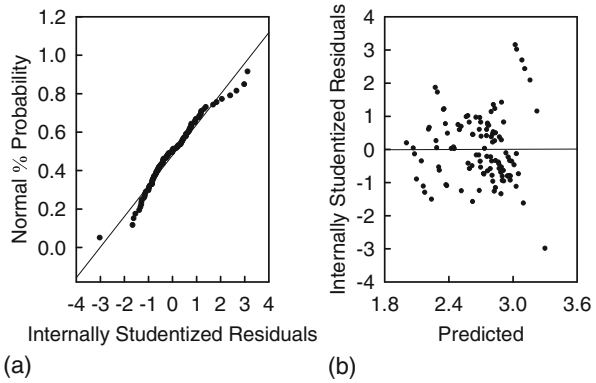

Fig. 3: a The residual normal probability plot and **b** the residuals vs. predicted plot for the response $\log \mathbf{C_{12}}$

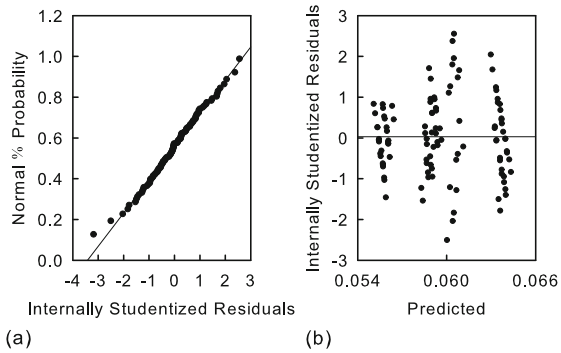

Fig. 4: a The residual normal probability plot and **b** the residuals versus the predicted plot for the response of $\mathbf{1}/\sqrt{\mathbf{C_{15}}}$

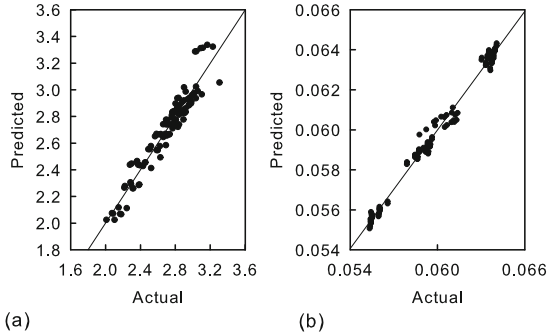

Fig. 5: Scatter plots calculated from the response surface model versus the simulated values obtained from the 3D field TCAD simulator for the **a** $\log \mathbf{C_{12}}$ and **b** $\mathbf{1}/\sqrt{\mathbf{C_{15}}}$

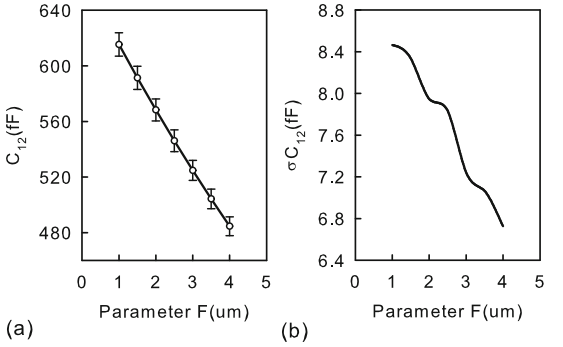

Fig. 6: **a** The relationship between the C_{12} and the parameter F. **b** The standard deviation of the C_{12} versus the parameter F

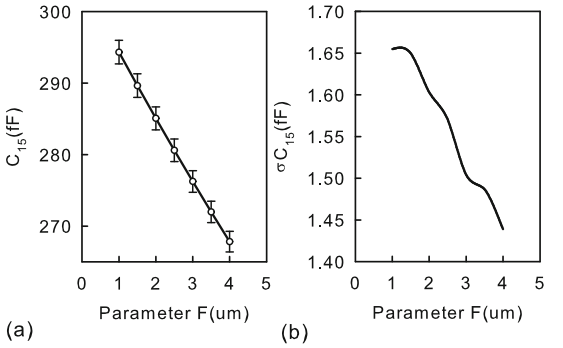

Fig. 7: **a** The relationship between the C_{15} and the parameter F. **b** The standard deviation of the C_{15} versus the parameter F

Table 3: A set of optimized designing parameters of the tested TFT-LCD pixel for the gate delay time minimization

	A	B	C	D	E	F	G	H	I	Gate delay time
Original	0	0	0	0	0	0	0	0	0	2887.1 ns
Optimized	4.919	0.0525	0.7985	2.2996	4.527	4.535	3.2022	-3.932	-0.6898	8.229 ns

4 Conclusions

In this work, we have successfully implemented a computational statistics technique for the capacitance sensitivity analysis of a TFT-LCD pixel and design optimization of the whole TFT-LCD circuit. Based on the 3D field solver and the central composite design method, the second-order response surface models have been constructed for the structural capacitances. Consequently, the constructed models were applied

to study the sensitivity of capacitance with respect to the structural designing parameters and optimal design of the gate delay time of the tested TFT-LCD circuit in a computationally effective way, compared with a full 3D TCAD simulation. This approach can be incorporated into CAD tools for TFT-LCD design and can benefit the design automation of display panels.

Acknowledgements This work was supported by National Science Council (NSC),Taiwan under Contract NSC-97-2221-E-009-154-MY2 and Contract NSC-96-2221-E-009-210, and by the Innolux Display Corp., Chu-Nan, Taiwan under a 2006-2008 grant.

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