CHARGE TRANSFER AND STORAGE IN MAOS STRUCTURES

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Abstract

Metal/Aluminum-oxide/Silicon-oxide/Silicon (MAOS) structures consisted of 900 Å thick Al_2O_3 films deposited by rf reactive sputtering on thermally grown SiO_2 layers 70-500 Å thick, were made and demonstrated switching and charge storage capabilities using the capacitance-voltage technique. With positive voltage applied to the metal gate, negative charge is easily introduced into the oxide system. The removal of the negative charge from the system and/or introduction of positive charge into the system can be accomplished by applying negative voltage to the metal. However, the charge transfer in the latter process is not as easily accomplished as those in the former process. The memory retention characteristics of the MAOS structure were also investigated. MAOSFET was fabricated. It demonstrats the threshold voltage can be easily changed.

I. INTRODUCTION

There has been considerable interest in the double-layered insulator structures in Si devices because of their application to non-volatile insulated-gate field-effect memory transistors. In particular, the MNOS (Metal/Silicon-nitride/Silicon-oxide/Semiconductor) and MAOS (Metal/Aluminum-oxide/Silicon-oxide/Semiconductor) systems[1]-[12] with very thin oxide ($<$50 Å) has been examined in detail.

MAOS system is essentially a Metal/Oxide/Semiconductor (or Metal/Insulator/Semiconductor) structure. The characteristics of the MOS structure is best described by its capacitance-voltage curve. The position of the C-V curve depends upon the effective amounts of charge presented in the oxide. For convenience, the flat-band voltage (V_{FB}), which represents the amount of voltage needed to be applied at the MOS's metal plate in order to bring about the flat energy band condition within the semiconductor up to the surface, has been commonly used as a reference voltage.

It is presumed that some trapping states exist at the interface between these two oxide layers, and these traps can communicate with the silicon when a field is applied across the insulators. Therefore, by applying an appropriate positive voltage to the metal gate, electrons in the semiconductor can be injected through the SiO_2 thin layer and get trapped at the trapping

states. In this way, the C-V curve shifts its position toward positive voltage direction. On the other way, if an appropriate negative voltage is applied, the trapped charges can be tunneled back to the semiconductor, so that the C-V curve shifts back toward negative voltage direction.

During the past several years, the Al_2O_3 layers of the investigated MAOS structures were prepared by various deposition techniques. These include various chemical vapor depositions: reactive evaporation of Al in O_2[7], pyrolysis of trimethyl-Al in O_2 at 450°C[2], or of Al-isopropoxide in O_2 at 420°C[8], pyrolysis of $AlCl_3$ in CO_2-H_2 at 850°C[9], or of $AlBr_3$ in NO-forming gas mixture at 900°C[10]; rf sputtering[11]; and plasma anodization[12]. Although some authors[7],[9] have not mentioned the occurance of SiO_2 in their insulator system, it appears likely that in all cases a layer of natural thin oxide (about 10-20 Å thick) was present on the silicon wafer used as substrates for Al_2O_3 deposition. All these structures showed similar switching phenomena to those of MNOS. However, MAOS structure does have some advantages; the dielectric constant of Al_2O_3 is larger than that of Si_3N_4, which causes a higher proportion of the applied field to appear initially across the SiO_2 layer resulting in the lower applied voltage to initiate charge accumulation and the conductivity of Al_2O_3 is lower than that of Si_3N_4 under the similar conditions, resulting in the slower discharge of the stored charge in the film.

In this work, charge storage and memory properties in MAOS systems with Al_2O_3 deposited onto a relatively thick thermal oxide (~300 Å) by rf reactive sputtering were investigated and the results are herewith reported.

II. EXPERIMENTAL TECHNIQUES

Polished (111) oriented n-type silicon wafers of 10 ohm-cm resistivity were used as substrates in the fabrication of the test samples. Prior to any processing, the silicon wafers were cleaned in a 1:1:1 solution of acetone, isopropyl alcohol, and trichloroethylene, and rinsed in ultrasonically agitated, flowing, deionized water for at least 10 minutes. Thick (≥300 Å) silicon oxide layers were grown in dry oxygen at 1100°C. Thinner oxides were grown at 910°C. Subsequently, the Al_2O_3 films were deposited by rf reactive sputtering. A conventional diode-type rf sputtering system was employed for this purpose. The rf generator operating at 13.56 MHz was used as the source of power which was coupled to the target electrode. The cathode was a pure aluminum disk 5 inches in diameter. The substrate

was set on a grounded plate which was situated about 4 cm below the cathode. The depositions were performed in a pure oxygen atmosphere at pressure of 10 mtorr and with 0.8 watt/cm^2 input power density. The rate of deposition was about 20 Å/min. Although the support plate was preheated, the nominal substrate temperature did not exceed 200°C. After deposition, the aluminum oxide films were annealed in helium for one hour at 900°C.

Aluminum gate electrodes were applied to the oxide films by means of electron bean evaporation and photomasking. Gate areas were 3.44×10^{-3} cm^2 (26 mil diameter aluminum dot). Individual devices were diced out, and bonded to TO-5 headers using ultrasonic bonders.

Voltage pulses of various amplitudes and lengths were applied, and the state of charging of MAOS systems was evaluated from its flatband voltage obtained from a capacitance-voltage measurement made at 1.7 MHz.

III. EXPERIMENTAL RESULTS

Generally, we observed that the voltage applied to a MAOS structure must be higher than a certain critical voltage before the capacitance-voltage curve starts to show any observable shift of position. Figure 1 shows a

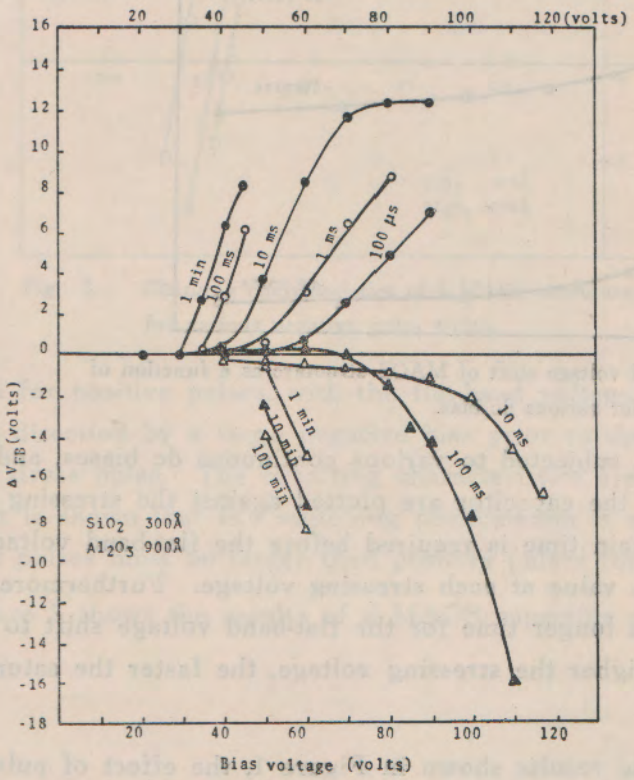

Fig. 1 Flat band voltage shift of MAOS structure as a function of applied bias for different pulse widths.

typical flat-band voltage shift as a function of applied bias with the pulse width as parametr. The curves in the upper half of the figure represent those subjected to positive bias, while the curves in the lower half are for negative bias. The dimensions of this particular MAOS structure are 900 Å of Al_2O_3 deposited on a 300 Å thick SiO_2. It is seen that negative bias required a higher amplitude and longer pulse width to induce the same amount of flat-band voltage change as compared to those of the positive bias. Further, the MAOS structure can exhibit a saturation of flat-band voltage change as shown in Figure 1 by the 10 ms curve for positive voltage stress. This is more clearly indicated in Figure 2, where the same

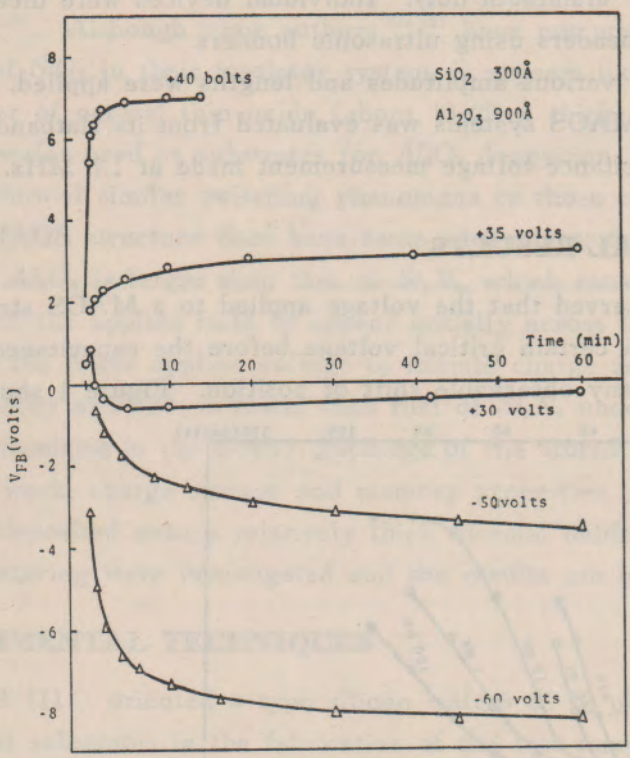

Fig. 2 Flat-band voltage shift of MAOS structure as a function of time under various dc bias.

MAOS capacitor was subjected to various continuous dc biases, and the flat-band voltages of the capacitor are plotted against the stressing time. It is seen that a certain time is required before the flat-band voltage reaches its saturation value at each stressing voltage. Furthermore, the negative bias needs a longer time for the flat-band voltage shift to reach saturation, and the higher the stressing voltage, the faster the saturation will be reached.

In addition to the results shown in Figure 1, the effect of pulse width and pulse amplitude on the charge transfer characteristics was further investigated as follows. The MAOS capacitor was subjected to a large

positive voltage long enough to cause a saturated flat-band voltage shift in the positive direction. A negative pulse of known amplitude and duration was then applied and the corresponding flat-band voltage was measured. After each negative pulse, the flat-band voltage was returned to its previous value and the procedure repeated. The resulting V_{FB} vs. applied voltage pulse characteristics are shown in Figure 3. The same procedure was

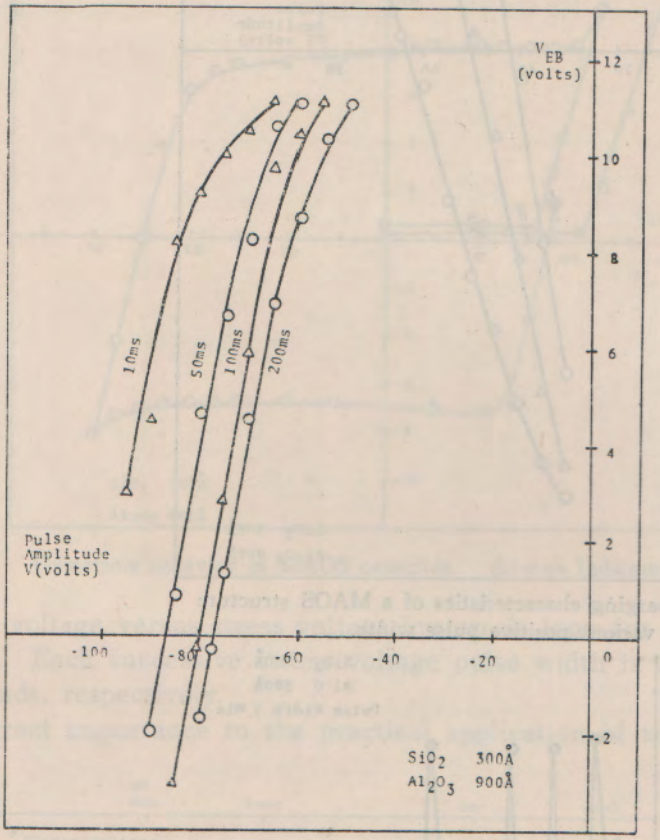

Fig. 3. Charging characteristics of a MAOS structure for various negative pulse width.

repeated for positive pulses, with the flat-band voltage first shifted in the negative direction by a large negative bias prior to the application of each positive stress pulse. The resulting characteristics are shown in Figure 4. Again, it is shown that the switching phenomenon is asymmetric in that negative pulses must be larger than positive pulses for the same shift.

Figure 5 shows the results of a MAOS capacitor subjected to alternative

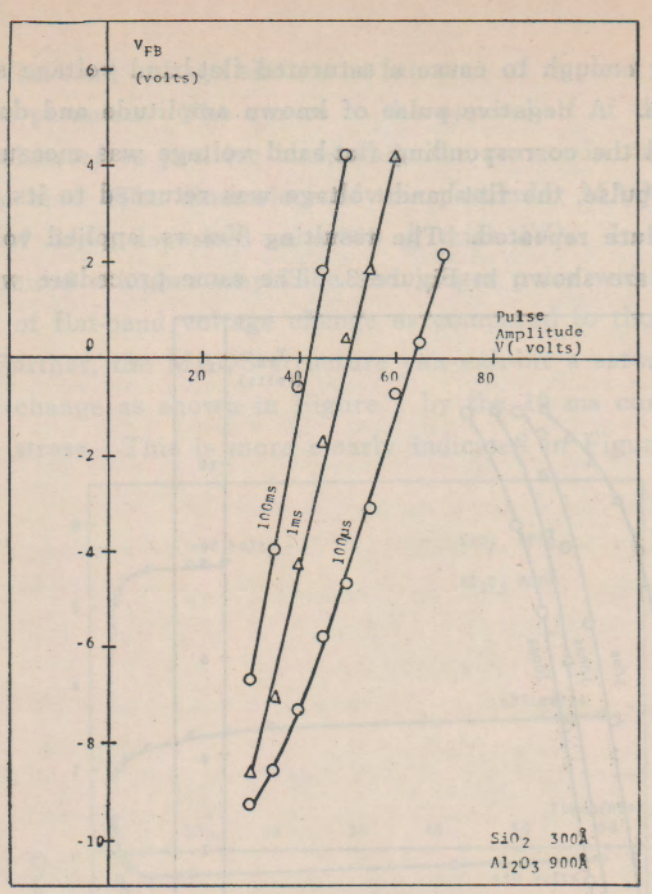

Fig. 4 Charging characteristics of a MAOS structure of various positive pulse width.

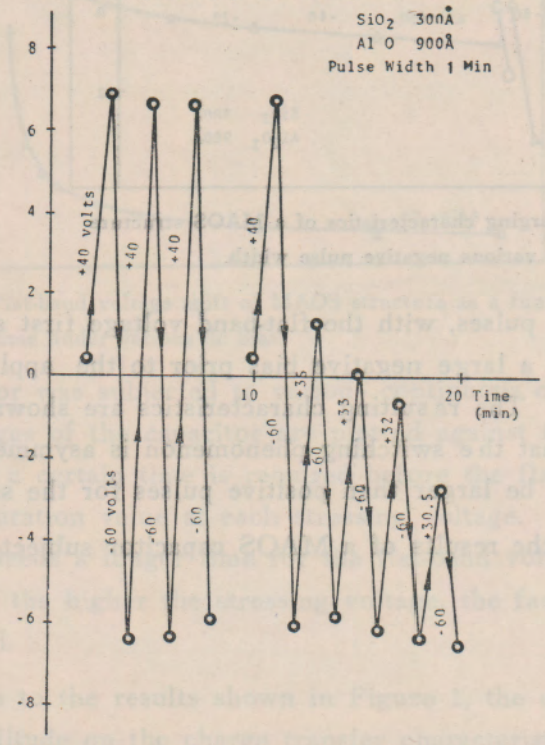

Fig. 5 MAOS structure subjected to alternative positive and negative stressing voltage of various amplitude; bias duration is one minute.

positive and negative voltage stress at a given amplitude of 1 minute pulse width. We see that the final V_{FB} value for a stressing voltage of -60 volts is not sensitive to the starting position of V_{FB}. In Figure 6, a typical

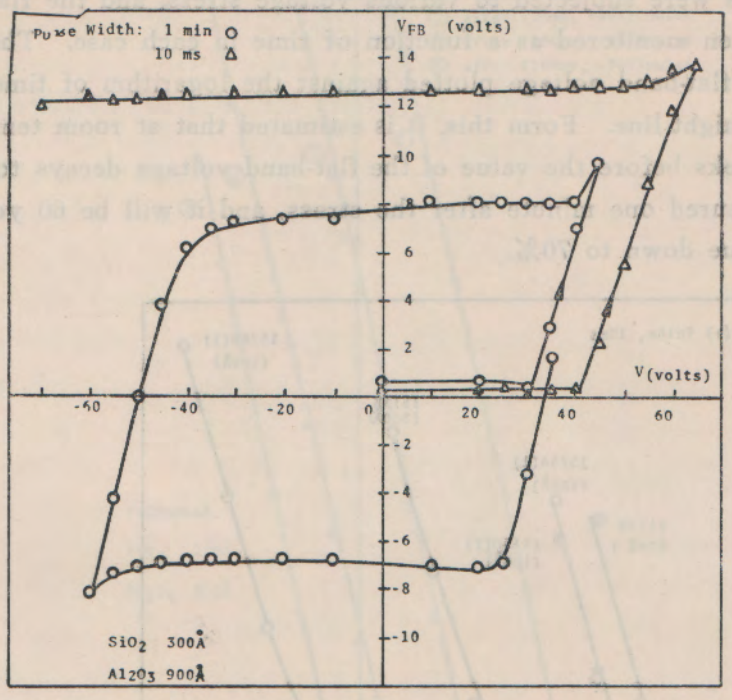

Fig. 6 Hysteresis behavior of MAOS capacitor. Arrows indicate direction of stressing.

flat-band voltage versus stress voltage hysteresis loop for a MAOS structure is shown. Each successive stress voltage pulse width is 1 minute and 10 milliseconds, respectively.

Of great importance to the practical application of the MAOS memory

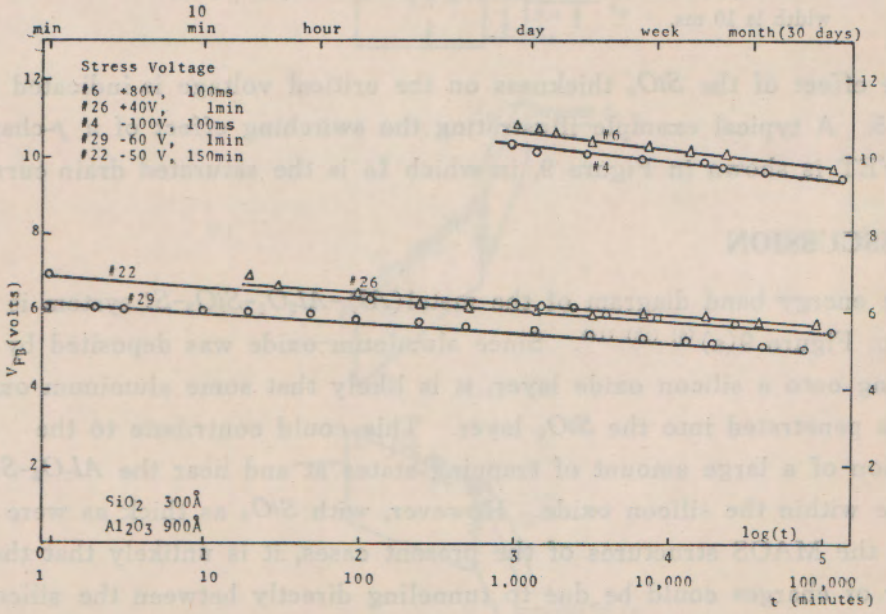

Fig. 7 Charge retention characteristics of a MAOS structure.

structures is the long term retention of the stored charge. Figure 7 shows the results of flat-band voltage decay as a function of time. Individual MAOS samples were subjected to various voltage stress, and the flat-band voltage was then monitored as a function of time in each case. The results show that the flat-band voltage plotted against the logarithm of time turns out to be a straight line. Form this, it is estimated that at room temperature it takes 10 weeks before the value of the flat-band voltage decays to 80% of the value measured one minute after the stress, and it will be 60 years before the value down to 70%.

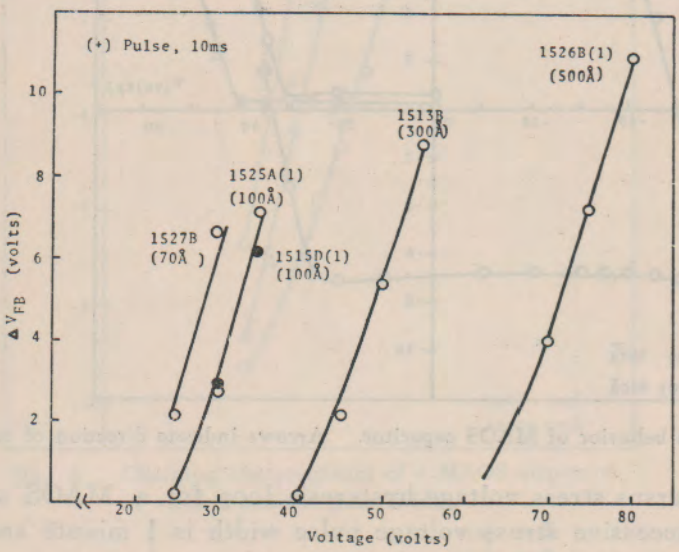

Fig. 8 Flat band voltage shift vs bias voltage for MAOS structure with various thickness of thermally grown SiO_2 films. The numbers in parenthesis are thickness of SiO_2 in each structure. Pulse width is 10 ms.

The effect of the SiO_2 thickness on the critical voltage is indicated in Figure 8. A typical example illustrating the switching effect of a *p*-channel MAOSFET is shown in Figure 9, in which I_D is the saturated drain current.

IV. DISCUSSION

The energy band diagram of the metal(Al)-Al_2O_3-SiO_2-Si system is shown in Figure 9(a)[6] [13] [14]. Since aluminum oxide was deposited by sputtering onto a silicon oxide layer, it is likely that some aluminum oxide particles penetrated into the SiO_2 layer. This could contribute to the generation of a large amount of trapping states at and near the Al_2O_3-SiO_2 interface within the silicon oxide. However, with SiO_2 as thick as were used in the MAOS structures of the present cases, it is unlikely that the transfer of charges could be due to tunneling directly between the silicon and the traps, even for the case of 70 Å thick SiO_2. Direct tunneling can

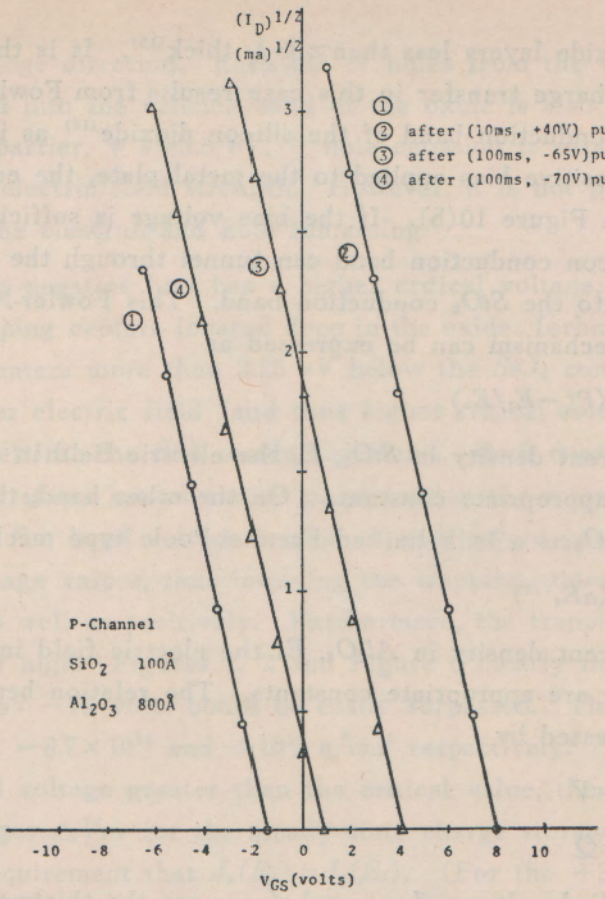

Fig. 9 Switching effect of a p-channel MAOSFET. I_D is the saturated drain current. V_{GS} is the applied voltage on the gate.

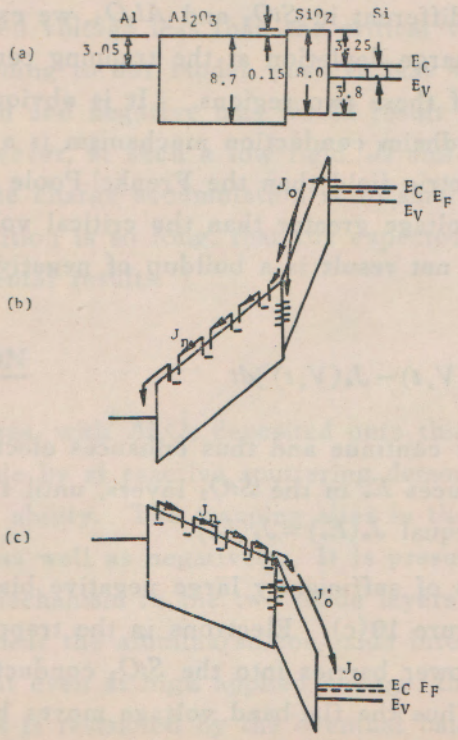

Fig. 10 Energy band diagram of MAOS structure under (a) no bias, (b) positive bias, and (c)negative bias.

occur in silicon dioxide layers less than≈35 Å thick[15]. It is therefore presumed that the charge transfer in this case results from Fowler-Nordheim tunneling into the conduction band of the silicon dioxide[13] as is shown in Figure 10. With positive bias applied to the metal plate, the energy-band diagram is shown in Figure 10(b). If the bias voltage is sufficiently high, electrons at the silicon conduction band can tunnel through the narrowed triangular barrier into the SiO_2 conduction band. This Fowler-Nordheim current transport mechanism can be expressed as

$$J_o = J_{oo} E_o^2 EXP(-E_1/E_o) \tag{1}$$

where J_o is the current density in SiO_2, E_o the electric field in SiO_2 layer, and J_{oo} and E_1 are appropriate constants. On the other hand, the current transport in the Al_2O_3 is a bulk limited Frenkel-Poole type mechanism[11]

$$J_a = J_{aa} EXP(\alpha E_a^{1/2}) \tag{2}$$

where J_a is the current density in Al_2O_3, E_a the electric field in Al_2O_3 layer, and J_{aa} and α are appropriate constants. The relation between E_0 and E_a can be expressed by

$$E_o d_o + E_a d_a = V \tag{3}$$

$$E_o \varepsilon_o - E_a \varepsilon_a = Q \tag{4}$$

where V is the applied voltage, d_o, ε_o and d_a, ε_a are the thickness and dielectric constant of the SiO_2 and Al_2O_3 layer, respectively. Since the transport mechanism is different in SiO_2 and Al_2O_3, we expect changes in the charge storage or charge depletion at the trapping centers located at and near the interface of these two regions. It is obvious from Eqs. (1) and (2) that Fowler-Nordheim conduction mechanism is a much more sensitive function of electric field than the Frenkel-Poole type conduction. Presumably at applied voltage greater than the critical voltage, J_o is larger than J_a. Therefore, the net result is a buildup of negative charge near the Al_2O_3/SiO_2 interface.

$$Q(V,t) = -\int_o^t [J_o(V,t) - J_a(V,t)]dt \tag{5}$$

This charge buildup will continue and thus enhances electric field strength E_a in the Al_2O_3 and reduces E_o in the SiO_2 layers, until the current density in each oxide becomes equal $J_o(E_o) = J_a(E_a)$.

With the application of sufficiently large negative bias, the energy band diagram is shown in Figure 10(c). Electrons in the trapping sites now tunnel through the narrower barrier into the SiO_2 conduction band and return to the silicon. Thus the flat-band voltage moves back toward the

negative voltage direction. Emission of holes from the valence band of the silicon into the valence band of the oxide is also possible. Because of the high barrier, $\phi_{sh}=3.8\ eV$,[13] hole emission is expected to be smaller at the same electric field strength. However, it is not possible to distinguish the electron and hole tunnelling.

Since the negative bias has a higher critical voltage, it would be clear that the trapping centers located deep in the oxides forbidden gap. Electrons trapped at centers more than 3.25 eV below the SiO_2 conduction band would require higher electric field (and thus higher critical voltage under negative bias) to tunnel into the SiO_2 conduction band. Both donor type and acceptor type trapping states are presumed to present at the interface, owing to the fact that the flat band voltage can be shifted toward positive as well as negative voltage values, thus implying the trapping states can be charged negatively as well as positively. Furthermore, the trapping states density must be very high. Figures 1, 2 and Figure 6 clearly indicate $V_{FB}=+14$ volts and $V_{FB}=-16$ volts could be easily surpassed. The above data is equivalent to -8.7×10^{12} and $+10^{13}$ q/cm^2 respectively. Therefore, at a given applied voltage greater than the critical value, the saturated flat-band voltage changes $\triangle V_{FB}$ (or the steady state charge storage or depletion) is set by the requirement that $J_a(E_a)=J_o(E_o)$. (For the +30 volts stress in Figure 2, the reason for the negative flat-band voltage shift during the first few minutes is not clear).

With the applied voltage less than the critical value, it is presumably that $J_o<J_a$. According to our model, positive bias would result in positive charge accumulation and negative bias would result in negative charge accumulation. However, at such a low field, J_o and J_a are very small, so that the steady state charge accumulation is so small and the time required to reach such condition is so long, that the expected effect did not show up in our experimental results.

V. CONCLUSION

MAOS structures, with Al_2O_3 deposited onto thick (300 Å and more) thermal silicon oxide by rf reactive sputtering demonstrate charge transfer and charge storage ability. The trapping sites in the structure can be charged positively as well as negatively. It is presumed that different current transport mechanism in the two oxide layers accounts for the buildup of charge near the alumina/silicon-oxide interface. The trap density is very high, so that even at high applied voltage, the charge buildup at the interface trap states is restricted by the eventual balance of the current

densities in the two oxides. Together with the long term charge retention property, the MAOSFET would render favorable application as non-volatile memory device.

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