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SEMICONDUCTOR MEMORIES

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Abstract—*Integrated semiconductor memories have many advantages in performance and cost and are threatening the dominance of magnetic cores for random-access memory. Both MOS and bipolar integrated circuits can be used to advantages. There are at present the read-write memory, read-only memory and alterable read-only memory. Other interesting semiconductor memory developments include the non-volatile memories, the charge coupled devices and "Bucket Brigade" shift registers, and amorphous glass.*

INTRODUCTION

Semiconductor memories offer many advantages over magnetic memories: (a) simpler interfacing between the central processor and the memory because same type of circuits (e.g. TTL) can be used; (b) higher speed; (c) non-destructive readout and (d) lower cost.

There are two basic types of storage elements used in semiconductor memories: (a) flip-flop; (b) charge-storage device such as a capacitor. The information stored in a flip-flop is permanent unless the power supply is cut off. The information stored in a capacitor will leak off in time. The permanent flip-flop storage element can be fabricated in a number of ways by connecting two inverters in cascade. Simplicity in circuitry is important to conserve area.

Memories can be classified into serial memories and random-access memories. In the serial memory, information is written into and read out from a long shift register sequentially. The circuit is usually simple and terminals are few, but the access time is long. Unlike the sequential memory, the random access can be written in and read out at any time. The operation is much faster. Since speed is one of the attributes of semiconductor memories, it is in this application where semiconductor memories show the greatest promise.

BIPOLAR SHIFT REGISTERS

Shift-register functions can be obtained by using flip-flops in conjunction with some logic gates. Shift-register bits are shown in Figure 1. Bipolar shift registers are capable of high speed but occupy large

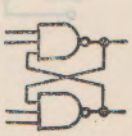


Fig. 1. Registers and Shift Registers

chip area due to circuit complexity in the master-slave scheme and the large capacitor area in the capacitor steered shift register.

MOSFET SHIFT REGISTERS

MOSFET'S can be used to perform shift-register functions in a manner similar to that of bipolar transistors. A *p*-channel shift-register bit is shown in Fig. 2(a). Logic information is introduced to the flip-flop through Q_1, Q_2 and Q_3 are caused to conduct to latch the flip-flop. Because of the unique isolated control of the transmission switches[1] no complicated steering scheme such as that used in bipolar shift registers is required. Thus the area is smaller.

For low-power operation, the complementary MOSFET shift register as shown in Fig. 2(b) may be used. Note that complementary transmission switches are shown to permit the use of clock pulses having the same amplitude as the supply voltage. Due to the absence of standby power the dissipation is very low.

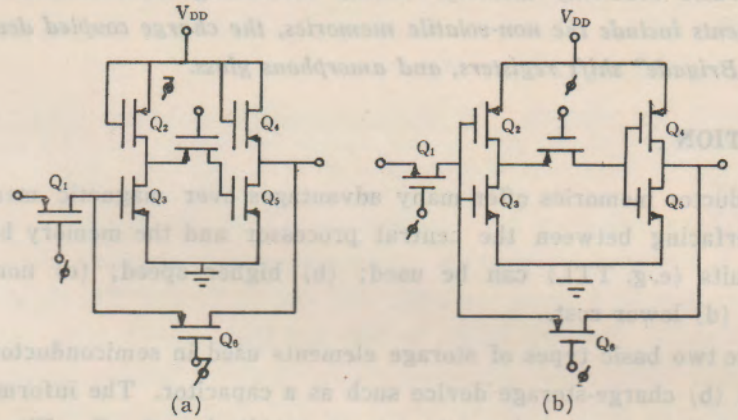


Fig. 2. MOSFET Shift Register

DYNAMIC SHIFT REGISTERS

In dynamic shift registers, the information is stored in a capacitor instead of a flip-flop. The basic scheme is shown in Fig. 3. The chip area is generally smaller than in a flip-flop register. However, the information must be refreshed or transferred before the capacitors discharge significantly. The successive storage capacitors are isolated with transmission switches and inverters. The purpose of the inverter

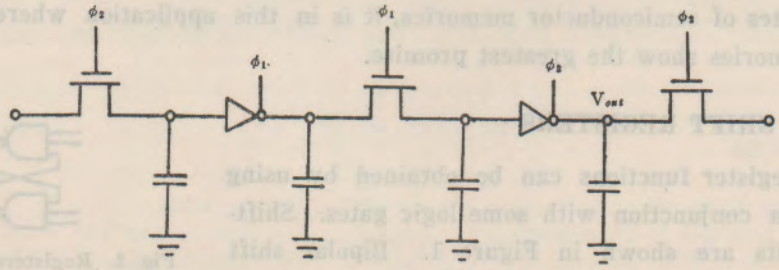


Fig. 3. Basic Dynamic Shift Register

is to provide some gain in the interstage, as otherwise the voltage levels across the following capacitors would decrease due to charge division. For this reason, there is a minimum clock frequency that can be used. The following are some typical shift registers:

Two-Phase Ratioed Shift Register. Fig. 4(a) shows a two-phase ratioed shift register. The channel resistance of the load device Q_2 should be made larger than that of the active device Q_1 so as to increase the low-state noise margin. Ratioed integrated circuits have the drawback that (i) the chip area is large, and (ii) the tolerance on geometry is tight. Figs. 4(b) and (c) indicate the control voltages used to activate the transmission switches. Fig. 5 shows a modified two-phase shift register in which the load device is clocked. Individual parts of this figure can be

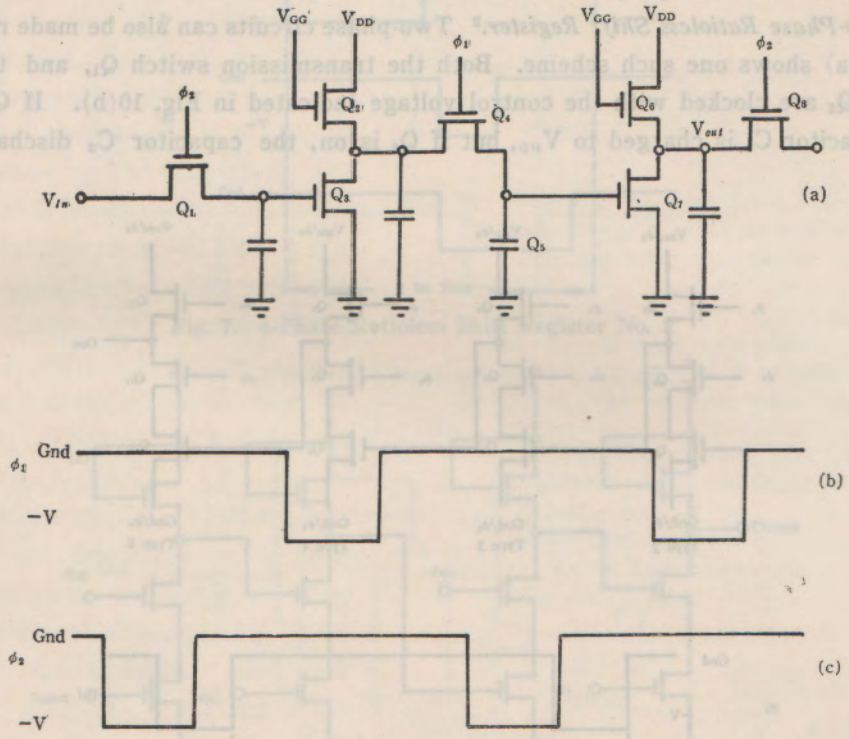


Fig. 4. 2-Phase Ratioed Shift Register

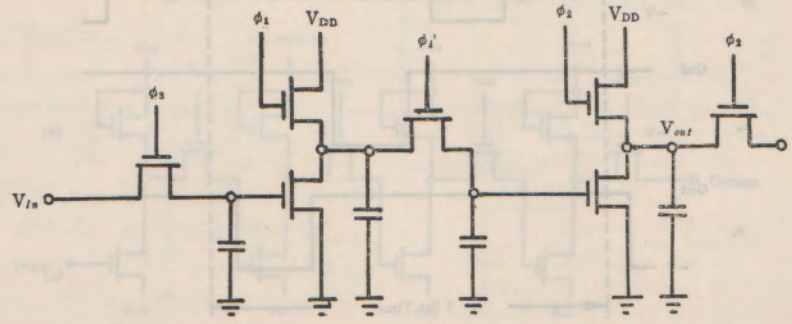


Fig. 5. 2-Phase Ratioless Shift Register

compared directly with similar parts of Fig. 4.

Four-Phase Ratioless Shift Register. One way to achieve a minimum geometry device (ratioless) circuit is to use the four-phase dynamic shift register. One versin of the four-phase shift register is shown in Fig. 6(a). The clock controles ϕ_1, ϕ_2, ϕ_3, ϕ_4, shown in Figs. 6(b), (c), (d) and (e) are sequentially applied. After the completion of the clock signals, the information at the input has been shifted to the output. Since the Q_1, Q_2, and Q_3 devices in the two left-hand branches are never on at the same time, there is no voltage-divider action and hence the devices can all be of minimum size. The generation of a four-phase clock is inconvenient, and often limits the speed. Other four-phase ratioless shift registers are also shown in Figs. 7, 8 and 9. Note that no $d-c$ power supply is used for the last three circuits. This is true with many dynamic circuits.

Two-Phase Ratioless Shift Register.[3] Two-phase circuits can also be made ratioless. Fig. 10(a) shows one such scheme. Both the transmission switch Q_1, and the load device Q_2 are clocked with the control voltage indicated in Fig. 10(b). If Q_3 is off, the capacitor C_3 is charged to V_{DD}, but if Q_3 is on, the capacitor C_3 discharges to

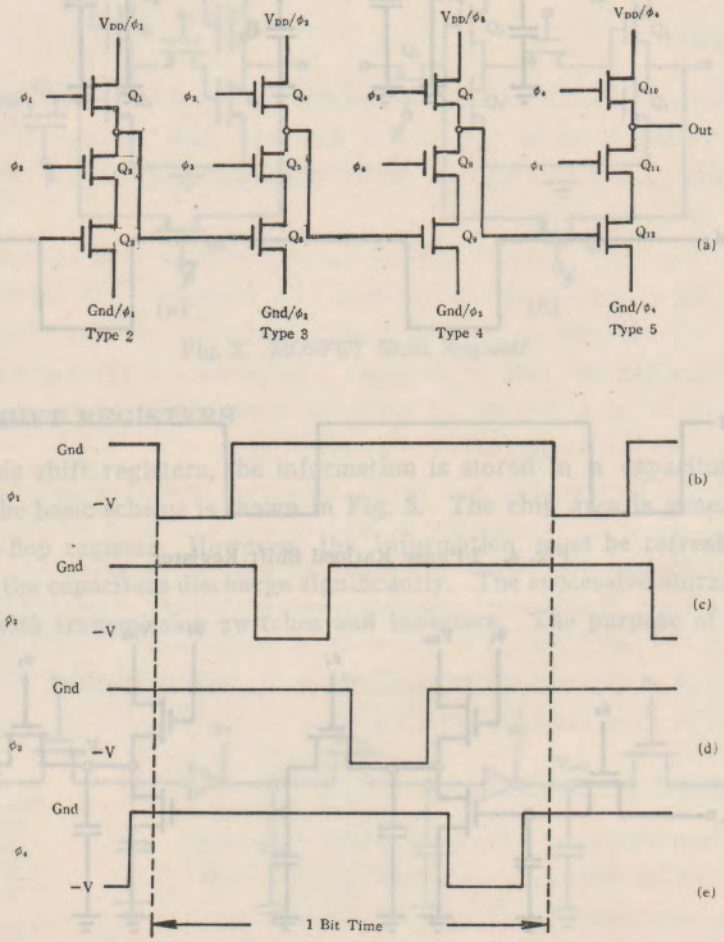


Fig. 6. 4-Phase Ratioless Shift Register No. 1

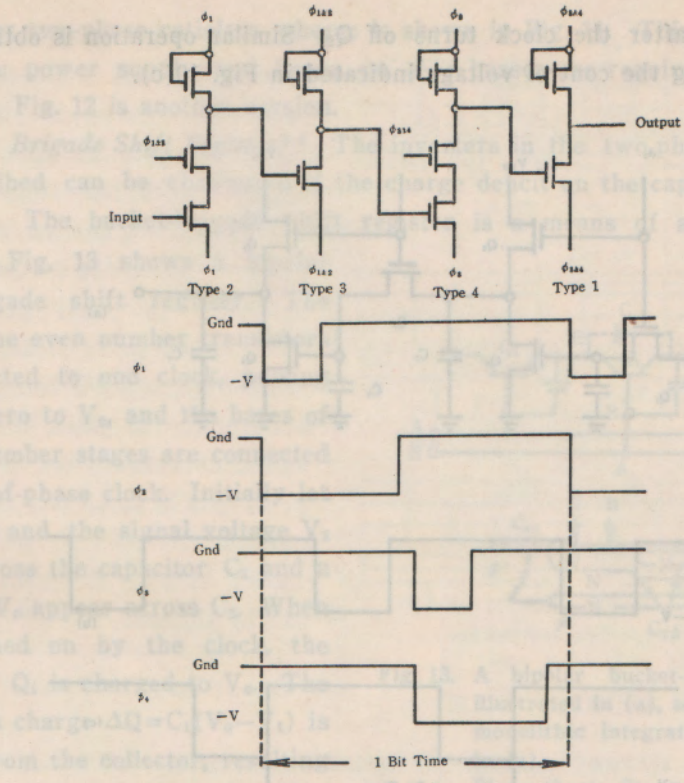


Fig. 7. 4-Phase Ratioless Shift Register No. 2

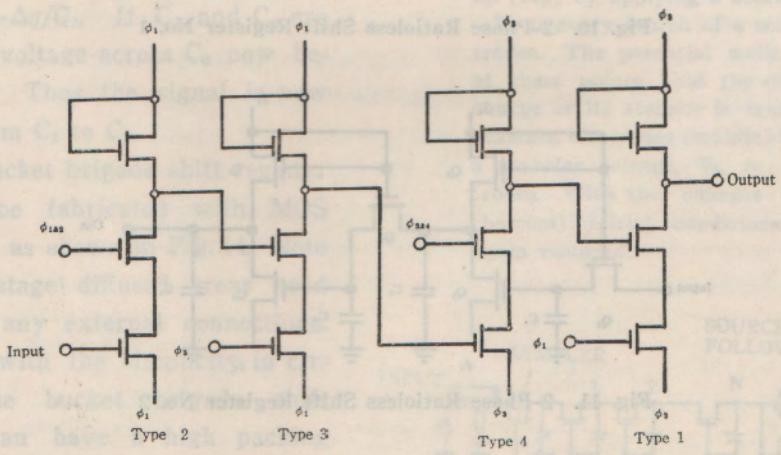


Fig. 8. 4-Phase Ratioless Shift Register No. 3

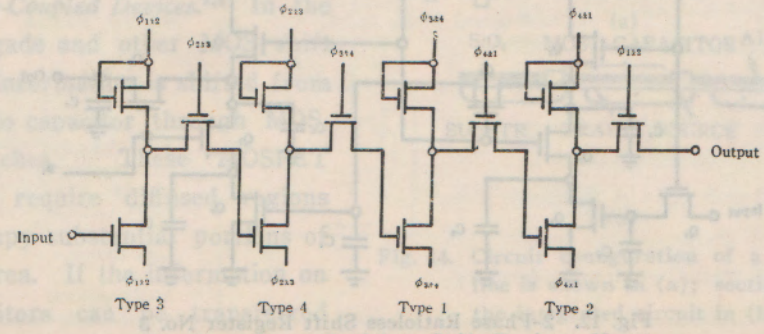


Fig. 9. 4-Phase Ratioless Shift Register No. 4

ground potential after the clock turns off Q_2. Similar operation is obtained with Q_4, Q_5 and Q_6 using the control voltage indicated in Fig. 10(c).

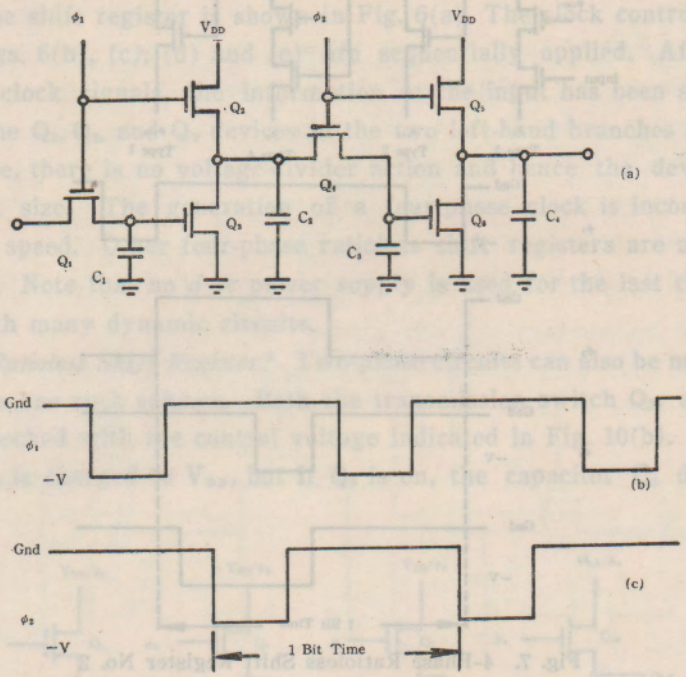


Fig. 10. 2-Phase Ratioless Shift Register No. 1

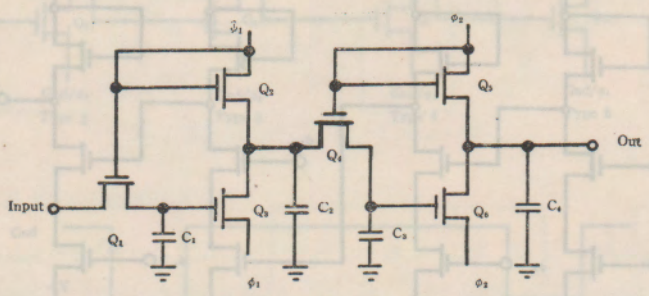


Fig. 11. 2-Phase Ratioless Shift Register No. 2

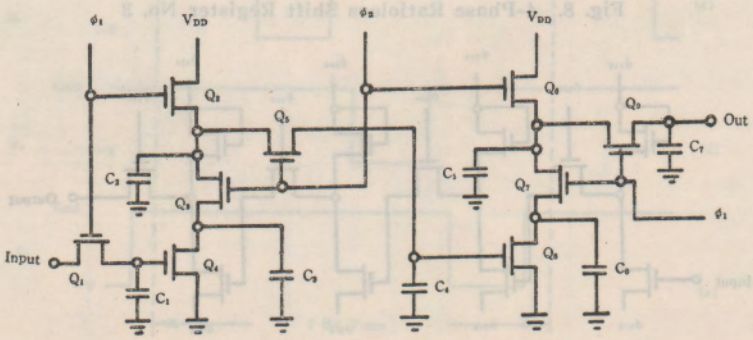


Fig. 12. 2-Phase Ratioless Shift Register No. 3

Another two-phase ratioless scheme is shown in Fig. 11. This scheme does not use a $d-c$ power supply and hence no $d-c$ busses are required, thereby saving chip area. Fig. 12 is another version.

Bucket Brigade Shift Register.[3,4] The inverters in the two-phase shift register just described can be eliminated if the charge deficit on the capacitors can be replenished. The bucket-brigade shift register is a means of accomplishing this function. Fig. 13 shows a bipolar bucket-brigade shift register. The bases of the even number transistors are connected to one clock, pulsing between zero to V_0, and the bases of the odd number stages are connected to an out-of-phase clock. Initially let Q_1 be off and the signal voltage V_1 appear across the capacitor C_1 and a voltage $+V_0$ appear across C_2. When Q_1 is turned on by the clock, the emitter of Q_1 is charged to V_0. The increase in charge $\Delta Q=C_1(V_0-V_1)$ is supplied from the collector, resulting in the discharge of C_2 from a voltage V_0 to $V_0-\Delta q/C_2$. If C_1 and C_2 are equal, the voltage across C_2 now becomes V_1. Thus the signal is now shifted from C_1 to C_2.

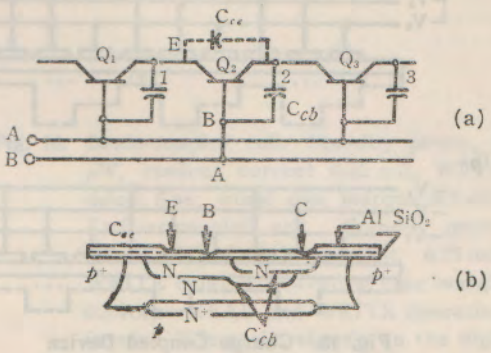


Fig. 13. A bipolar bucket-brigade circuit is illustrated in (a), sectional view of one monolithic integrated bucket is shown in (a).
Phase three. Storage conditions are set up (top) by applying a storage voltage, $-V_2$ to every fourth of a series of electrodes. The potential wells that form at these points hold the charge. The charge or its absence is transferred to adfacent electrodes (middle) by applying a transfer voltage, V_3, to those electrodes. With the charges transferred (bottom) initial conditions are once again restored.

The bucket brigade shift register can also be fabricated with MOS transistors as shown in Fig. 14. Note that interstage diffused areas need not have any external connections. Together with the simplicity in circuitry, the bucket brigade shift register can have a high packing density.

Charge-Coupled Devices.[3,5] In the bucket-brigade and other MOS shift registers, information is shifted from capacitor to capacitor through MOSFET switches. These MOSFET structures require diffused regions which occupy substantial portions of the chip area. If the information on the capacitors can be transferred

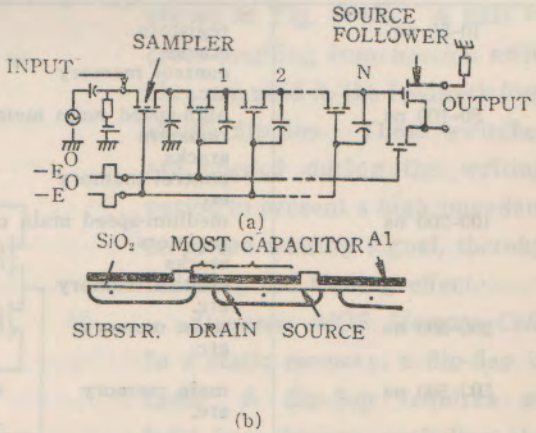


Fig. 14. Circuit configuration of a MOS delay line is shown in (a); sectional view of the integrated circuit in (b).

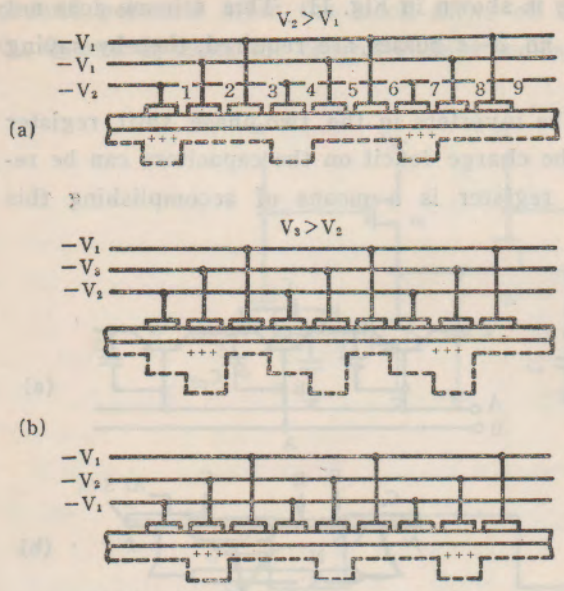


Fig. 15. Charge Coupled Device

directly without any switches, then there is a saving in area. This approach is used in the charge-coupled device as shown in Fig. 15(a). MOSFET shift registers contain only gates but no diffused regions. The gates are sequentially connected to multi-phase clocks. The clocked gates create depletion regions and hence a voltage minima underneath the gates. The charges stored underneath the neighboring gates tend to move into the voltage minima. By phasing the clocks as shown in Fig. 15(b), the charges can be shifted.

RANDOM ACCESS MEMORY (RAM)

Random access memory[6] can further be subdivided into: (a) read-write RAM, where the information can be written into and read out from the memory at high speed; (b) read-only memory, where the memory content is fixed but can be read out at random; (c) alterable read-only memory (also read-mostly memory), where writing is slow and infrequent but the reading time is fast. Table 1 shows the speed range of these memories.

Table 1. Random Access Memories

Speed Range	Typical Use	Technology
10-50 ns	registers stacks control memory etc.	bipolar silicon
50-100 ns	high-speed main memory registers stacks control memory etc.	bipolar silicon
100-200 ns	medium-speed main memory registers stacks control memory etc.	bipolar silicon
200-300 ns	main memory etc.	bipolar silicon MOS/bipolar silicon plated wire
300-500 ns	main memory etc.	bipolar silicon MOS silicon plated wire fast cores
500 ns and up	main memory etc.	cores MOS silicon

Bipolar Flip-flop. Fig. 16(a) shows a basic bipolar memory cell. For coincident addressing, two emitters are used. One emitter can be connected to the word line and the other line to the bit line. When the voltage on the word line is higher than the bit line, information from the bit line can be written into the cell. When the voltage on the word line is lower than the bit line, information from the bit line cannot be written into cell.

This type of cell usually uses the collector region as the load resistance to conserve area as shown in Fig. 16(b) due to the absence of isolation and the high resistivity of the epitaxial layer.

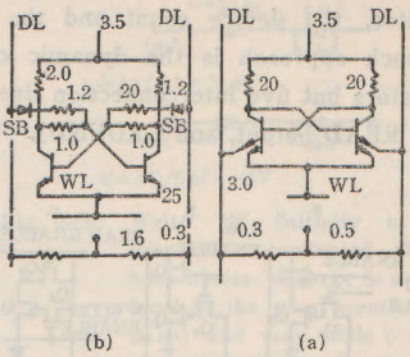


Fig. 16. Diode-coupled cell. Standby power, 65 μW, readout current 0.32 mA, WRITE delay, 5 ns; worst case margin, 0.2 volt. Emitter-coupled cell. Standby power, 800 μW, READOUT current, 0.15 mA; WRITE delay, 20 ns; worst case margin, 0.3 volt. READ and WRITE operations involve differential signals on the digit-line pair (DL, DL). Resistances are expressed in kilohms.

A modified version of the bipolar cell in conjunction with Schottky diodes[8] is shown in Fig. 16(b).

Static MOS Memory Cell.[9] The MOS memory cell can be constructed out of a simple DCTL flip-flop as shown in Fig. 17(a). Transmission switches are used to write and read information into and out of the memory cell and are controlled by addressing signals. Another version as shown in Fig. 17(b) uses two transmission switches for each cell to effect a push-pull action.

The complementary MOS memory can be formed in a similar fashion as shown in Fig. 17(c). Another version of the CMOS memory cell[10] is shown in Fig. 17(d). A pair of cross-coupling transmission switches are used in the feedback loop of the flip-flop. These switches are opened during the writing period to present a high impedance to the writing signal, thereby reducing the loading effect.

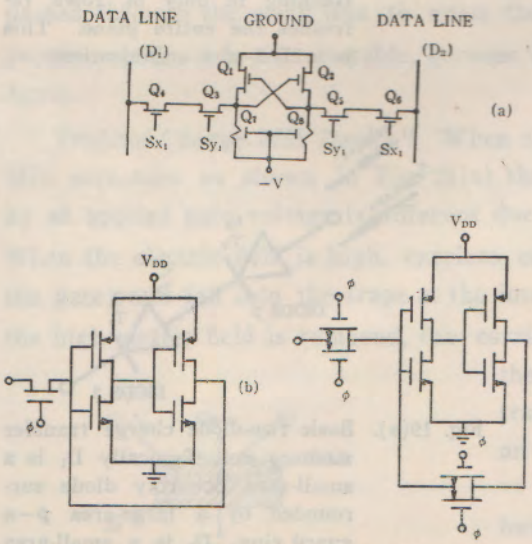


Fig. 17. Schematic for one bit of 64-bit MOS array

Dynamic MOS Memory Cell. In a static memory, a flip-flop is used. A flip-flop requires at least four devices excluding the selecting switches. If the information can be stored in a

capacitor, the device count and the circuit complexity can be much reduced. One such approach is the dynamic cell[11] shown in Fig. 18(a), using only three transistors but five interconnection lines (READ SELECT, WRITE SELECT, DATA input, READ output, and GROUND). The READ and WRITE SELECT lines can be combined into one common line to conserve area as shown in Fig. 18(b). However, the last memory cell requires a trilevel signal to drive the SELECT line: the first level is off, the intermediate level is for reading and the third level is for writing into the cell.

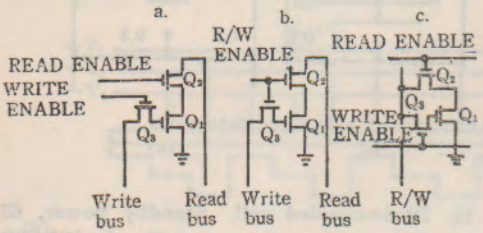


Fig. 18(a). Dynamic charge-storage MOS cells. Transistor Q_1 is the charge storage element in a. Transistor Q_2 connects Q_1 to the read bus when the READ ENABLE signal activates it. Transistor Q_3 provides a write path to the charge storage node when activated by the WRITE ENABLE signal. Periodic refreshing of data is also done through Q_3. In this process, we rewrite (or reinforce) the charge (or no charge) condition of the charge storage node from an on-chip refresh amplifier A typical memory array is shown in Fig. 18(b) where each column of bits has its own refresh amplifier. Other cells use similar charge-storage concepts. In b and c, there are some differences in cell conditions or periphery designts, but each is a three-transistor memory cell.

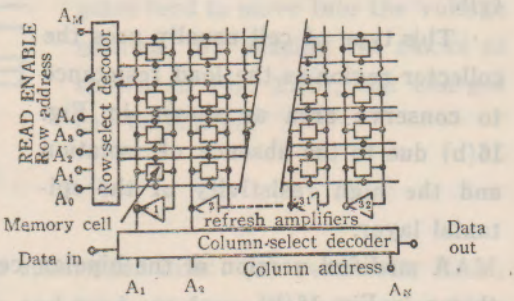


Fig. 18(b). MOS memory array. Activating any one of the M READ ENABLE signals will write the content of the N MEMORY cells in that row into their respective refresh amplifiers. This followed by the WRITE ENABLE command on that same row refreshes all memory cells in that row. Refreshing in only M rows refreshes the entire plane. This is a 2D 2-wire organization.

Two-diode Charge Transfer Memory Cell.[12] A small area Schottky diode is surrounded by a relatively large area $p-n$ junction guard ring. This compound diode is connected in series with a small-area diffused $p-n$ junction diode with lower capacitance but larger storage time constant than the Schottky diode as shown in Fig. 19(a). Information is written into the cell as forward current. Charge is accumulated in the $p-n$ junction. By reversing the polarity

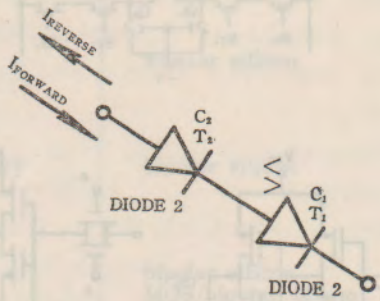


Fig. 19(a). Basic two-diode charge transfer memory cell Typically D_1 is a small-area Schottky diode surrounded by a large-area $p-n$ guard ring. D_2 is a small-area $p-n$ junction.

this charge is transferred to the large capacitance of the Schottky diode as stored information (see Fig. 19(b)) ($\Delta V = \Delta Q/C$). For selection, this memory cell is used as a cross-point in an X−Y matrix.

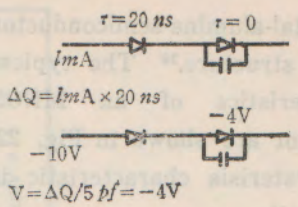


Fig. 19(b). Write "1" Initially a 1-mA current is conducted through both diodes. Charge is accumulated in the $p-n$ junction ($\tau = 20$ ns) and very little ($\tau = 0$) in the other diode. By reversing the polarity of the drive this charge represents a stored "1".

READ ONLY MEMORY (ROM)

A READ only memory[13] is a fixed memory. The memory is determined by the interconnection pattern. A diode or transistor matrix is the usual form as shown in Fig. 20. The base and the emitter are connected or not connected to the cross-point of an X−Y selection matrix. If the stored information of the ROM is to be changed, one must change the interconnection pattern.

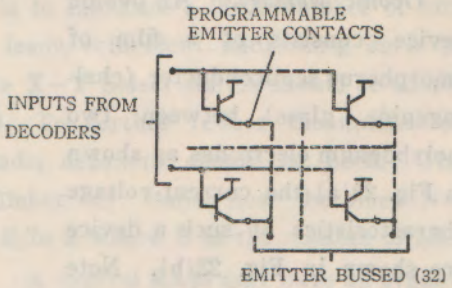


Fig. 20. Memory-cell array

ALTERABLE READ ONLY MEMORY

An alterable READ Only memory is also known as READ Mostly memory, and Programmable READ Only memory. Three different approaches are being used:

Fusable Links. The emitter connections are made of very thin narrow metal links (such as nichrome). Before the memory is programmed, all the emitters are connected to the links. If it is desired to open the emitter, a heavy current is passed through the weak link to open the connection. Although the memory is programmable, it is not alterable, because once the link is fused it cannot be closed again.

Trapped Charge MIS Device.[14] When two layers of dielectrics are used in an MIS structure as shown in Fig. 21(a) the electric fields in the two layers created by an applied gate voltage is different due to the difference to dielectric constants. When the electric field is high, carriers can be pulled from the substrate (or from the gate) and fall into the traps at the interface between the two dielectrics. After the high eletric field is removed, the carriers in the trap can affect the surface of the semiconductor substrate. For instance, trapped electrons can induce a p-channel in an n-type substrate.

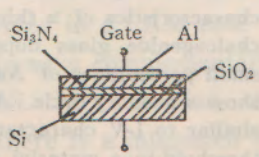


Fig. 21(a). MNOS Structure

The charge-trapping structures which have been investigated are the metal-nitride-oxide-semiconductor (MNOS) structure and

the metal-alumina-semiconductor (MAS) structure.[15] The typical characteristics of an MNOS transistor are shown in Fig. 22. The hysterisis characteristic is nonvolatile.

Fig. 21(b) shows a memory matrix[16] using charge trapping MIS device. Note that only one MNOS transistor is used for each bit. The density of this kind of memory is high.

Ovonic Memory.[17] An ovonic device consists of a film of amorphorus semiconductor (chalcogenide glass) between two molybdenum electrodes as shown in Fig. 23(a) the current-voltage characteristics of such a device are shown in Fig. 23(b). Note that the film has a high-resistance state and a low-resistance state. When such a film is connected in series with a silicon diode and place at the cross-point of X- and Y-SELECT lines, as indicated in Fig. 23(c), a random access memory is obtained.

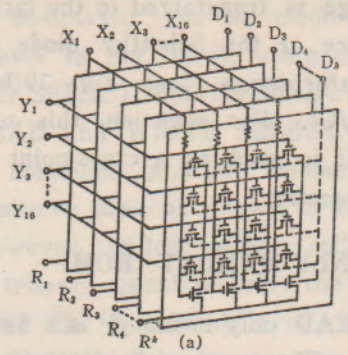


Fig. 21(b). 3-D-type READ-ONLY memory (a) Memory stack

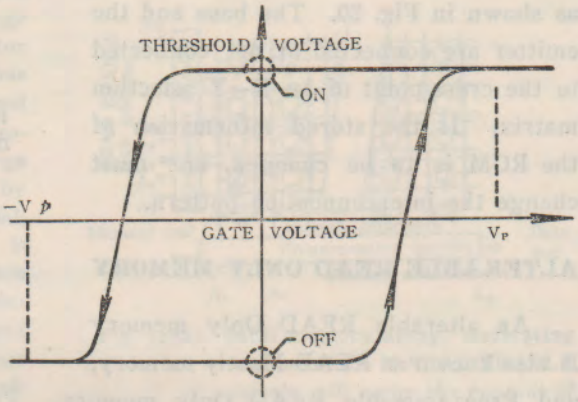


Fig. 22. Threshold Voltage Characteristics

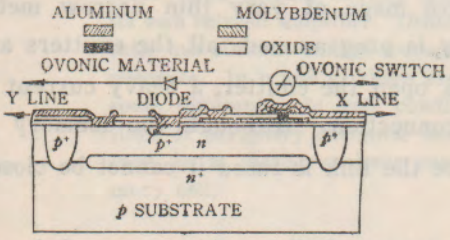


Fig. 23(a). Winning combination. Each read-mostly memory cell contains a thin-film of amorphous semiconductor material deposited on a single-crystal silicon substrate in series with a silicon diode. The metal stripes- the *x*-address lines-connect the doughnut-shaped Ovonic switches. Running perpendicular to the stripes the *y*-address lines buried in the silicon connect the figure-eight-shaped silicon diodes. The diagram at top details the cross section of a complete memory cell.

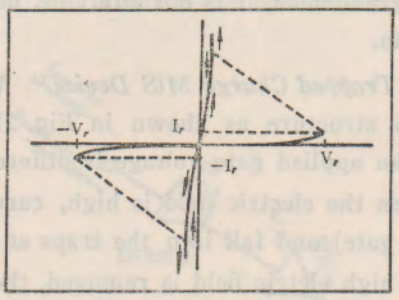


Fig. 23(b). Good memory. Current-voltage characteristics of a thin film of chalcogenide glass doped with small percentages of As and Sb show a memory cycle. Although similar to I-V characteristics of threshold-type material, no holding voltage is necessary.

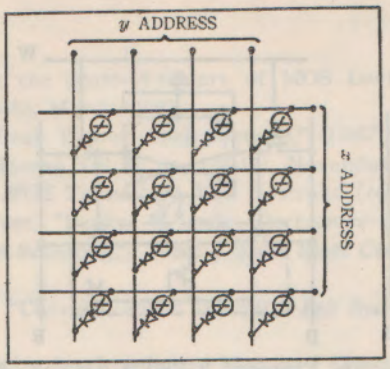


Fig. 23(c).

MEMORY ORGANIZATION

The tendency in semiconductor memories is to fabricate a large number of bits on a single chip. To conserve the number of leads, coincident addressing such as the X–Y Select matrix should be adopted. To further reduce the number of leads, decoders should be used. The number of leads now becomes N= lnB/ln 2 where B is the number of bits.

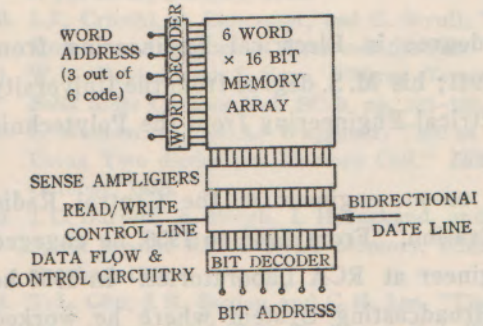
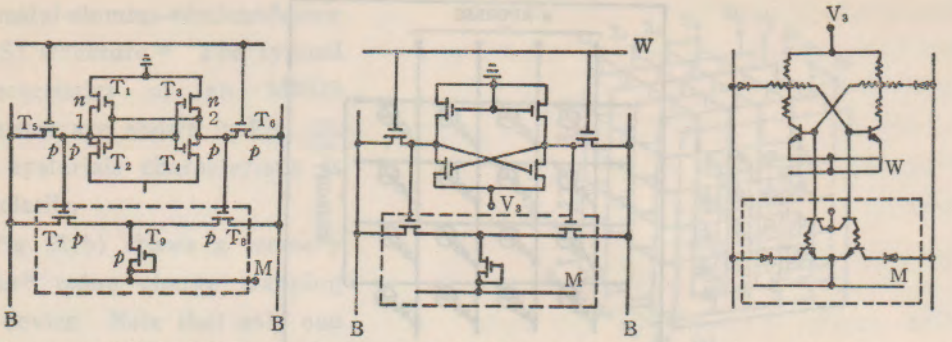


Fig. 24. Block diagram of 4100 256-bit memory component

A typical RAM may have an organization[18] as shown in Fig. 24. The complements $\bar{A}$ of the addressing signals A should be derived from a set of inverters before A's and $\bar{A}$'s are used to drive the decoders. The decoders are logic gates with N/2 inputs and the number of logic gate is equal to 2^N in the X SELECT line and 2^N in the Y SELECT lines. The input and output signals can be fed from the same line. A CHIP SELECT should be incorporated to enable or disable the chip. In practice buffers amplifiers are used in many parts of the circuits where large capacitive loadings are encountered such as the I/O buffer, the address input buffers, etc.

CONTENT ADDRESSIBLE MEMORIES (ASSOCIATIVE MEMORIES)[19]

In a content addressible memory (CAM), every word in the memory is searched to determine whether a portion of the word contains the selected pattern or key. To perform the CAM function, each memory cell is compared with a given bit information and matching signals are produced. Thus a matching circuitry must be provided in a CAM cell. Fig. 25(a) shows a *p*-channel MOSFET CAM cell, Fig. 25(b) shows a complementary MOS cell and Fig. 25(c) shows a bipolar transistor CAM cell. In each case, the match line M normally remains at reference voltage unless there is a mismatch between the information being searched and that stored in the cell.



(a) Proposed CIGFT CAM cell (b) Proposed IGFET CAM cell (c) Proposed bipolar transistor CAM cell

Fig. 25. Content Addressible Memory

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