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電子束蒸鍍在矽上鈦酸鋇之電氣特性
Electrical Properties of Electron Beam Evaporated Barium Titanate Film on Silicon

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ABSTRACT — The electrical properties of barium titanate films approximately from 1000A° to 5000A° thick, prepared by electron beam evaporation onto silicon (n or p) substrates in high vaccum system were investigated. The effects of substrate heating during deposition, different temperature and gases annealing process after deposition were also studied. The electrical characteristics of the film, including the dielectric constant, loss tangent, conductivity, metal-insulator-semiconductor surface properties, and ferroelectricity were also investigated. It was found that the room temperature substrate deposition and the annealing temperature below 120°C, would give the relative dielectric constant up to 1000 for both n-and p-type silicon substrate. The ferroelectric transition of barium titanate-silicon MIS structure was observed. The hysteresis behavior of barium titanate silicon MIS structure was first demonstrated and seemed promising to be used as non-volatile memory devices.

I. Introduction

Barium titanate ($BaTiO_3$) is a unique and interesting dielectric material, which in crystalline form exhibits ferroelectricity with a curie temperature of 120°C, a high dielectric constant, piezoelectricity, pyroelectricity and optical birefringence [1,2]. The thin-film form of barium titanate was expected to be highly technological interest with the increasing trend toward microelectronics and the advances in thin film preparation techniques. Considerable effort has been expended recently to prepare thin barium titanate [3,4] ferroelectric films. Until now, elaborate methods were used to insure proper crystallinity and stoichiometry, among these are vacuum evaporation [3], sputtering [4,5] and chemical vapor deposition [6]. Unfortunately, there are many inherent difficulties with

these techniques, the origin of the difficulty lies in the nature of ferroelecticity itself. Ferroelectricity is a cooperative phenomenon which depends critically on the delicate balance of ionic forces. Consequently, small deviations in the lattice parameter and stoichiometry are enough to severly reduce or even destroy the ferroelectricity. In general, the vacuum evaporation is plagued with the problem that the films are always deficient in the most volatile component such as oxygen [3]. Sputtering is difficult because the several elements in barium titanate compounds have different sticking coefficient [4,5]. In order to obtain the correct film stoichiometry, the oxygen enviroment should be provided to make up the oxygen deficiency during the deposition. But until now, sputtering techniques does not show to get the ferroelectric thin film on silicon [4,5]. Since silicon is one of the leading substrate in microelectronics, the unique dielectric and hysteretic properties of ferroelectric materials can be prepared in thin film form on the silicon, then a variety of nonvolatile memory devices can be fabricated by incorporating the semiconductor integrated circuit technology. It is the main motivation of this paper to present some electrical properties of barium titanate thin film on silicon prepared by the high energy electron beam evaporation techniques which to our knowledge have not yet been reported. In section 2, the electron beam evaporation techniques will be described. The electrical properties of barium titanate thin film MIS structure will be given in the section 3. Discussions and conclusion remark will be given in the last section.

II. Preparation of Barium Titanate Films on Silicon

The apparatus used for the deposition of barium titanate thin films by electron beam technique, consisted of 4KW electron gun with multiple sources. The distance between the evaporator source and wafer holder can be adjusted to give a desired uniform deposition, the substrate wafer can be back heated by a ring configuration of tungstun filaments with separate power control, the substrate temperature is then monitored by means of pt-pt: 10% Rh surface thermo couple. Silicon wafers with doping concentration of $9x10^{15}/cm^3$ n-type phosphorus doped <100> surface orientation and $4x10^{14}/cm^3$ n-type phosphorus doped <111> surface orientation, and $10^{16}/cm^3$ p-type boron doped <100> surface orientation, were used as the deposition

substrate. The high pure barium titanate piezoelectric crystal is used as the evaporation source. After the strict cleaning of the silicon substrate wafer and the barium titanate crystal, they were put into the vacuum system. The pressure was kept at 10^{-6} torr during the run. During the evaporation, the substrate was kept at various constant temperature ranged from room temperature to $600^{o}C$. Target to substrate distance was kept at 10 cm, and the power of electron-gun was adjusted at low level ranged from 10 W to 40 W. Typical deposition rate of 10 W power is about $540A^{o}$/min with substrate kept at room temperature. After the deposition, the barium titanate thin films on silicon were subjected to different annealing processes with different temperature, time and gas flows. It was found out that the deposition and annealing temperature are lower, the adhesion of $BaTiO_3$ film to silicon is poor, hence the temperature of deposition and annealing should be raised to improve the adhesion problem. When the annealing temperature is above 600° C, there are many recrystalized region "spots" shown in the barium titanate film. Among the various processes of annealing, the annealing temperature is $100^{o}C$ higher than the deposition temperature, the colors of the films will change and the film will become thinner, which appeared to be larger in crystalline size.

The thickness of the barium titanate films after annealing treatments was measured by interference microscope and ranged between $1000A^{o}$ and $5000A^{o}$. Most of the electrical evaluation involved the fabrication of MIS capacitor structures. These were prepared by evaporating aluminum or gold field plate through M_o metal mask. Aluminum was used to prepare the gate and back side contact of p-type silicon MIS structure, gold (0.1% Sb) was used to prepare the back side contact of n-type silicon samples. After finishing the above stated processes, the sample was scribed and mounted on TO-5 header for package, the capacitance-voltage, conductance-voltage and current-voltage characteristics were measured.

III. Electrical Measurements and Results

The electrical properties of barium titanate thin films on silicon MIS structure were measured by C-V, G-V and I-V characteristics. The capacitance-voltage and conductance-voltage relations were measured simultaneously by HP4270A Auto-Capacitance Bridge and HP2402A integrating Digital Voltmeter, and I-V characteristics were

measured by Tektronix 576 Curve Tracer. The relative dielectric constant of barium titanate thin film was deduced at the accumulation region of the barium titanate MIS structure. The relative dielectric constant of the barium titanate film on silicon deposited by electron beam technique for different deposition substrate temperature and annealing temperature, is shown in Fig. 1, where shows the typical silicon n-type <100> surface orientation with doping concentration of $N_D=9.0\times10^{15}/cm^3$. From Fig. 1, the general picture of relative dielectric constant is quite clear, which indicates that the increasing of annealing temperature and substrate deposition temperature will decrease the relative dielectric constant. The maximum dielectric constant of 1000 can be obtained at the condition of a room temperature substrate deposition and annealing at temperature below 120°C which is used to insure good adhesion. It was found that the substrate doping and substrate surface orientation did not give much difference in dielectric constant. The general tendency of annealing and substrate temperature variations are shown in Fig. 2. Different type of substrate doping concentration does give the different relative dielectric constant as shown in Fig. 3. When the very thin silicon oxide film of approximate 100A° is intentionally grown on the silicon substrate before barium titanate deposition, the measured relative dielectric constant will be lowered as shown in Fig. 4, where doposition temperature is 154°C. For higher temperature doposition (454°C), the relative dielectric constant is almost the same for barium titanate film with and without silicon dioxide layer. These characteristics are quite self-consistent with the observation before that the relative dielectric constant was decreased as the annealing temperature and the substrate temperature were increased, which are mainly due to the formation of thin silicon oxide layer on the silicon surface during the higher temperature substrate heating and oxygen ambient annealing processes. In general, the formation of amorphous silicon dioxide layer on silicon will cause the top-on barium titanate film to be more amorphous phase than the ferroelectric phase, which will give the lower relative dielectric constant. Also the series combination of the barium titanate capacitor film with the low dielectric constant of the amorphous silicon dioxide film will give the lower effective relative dielectric constant.

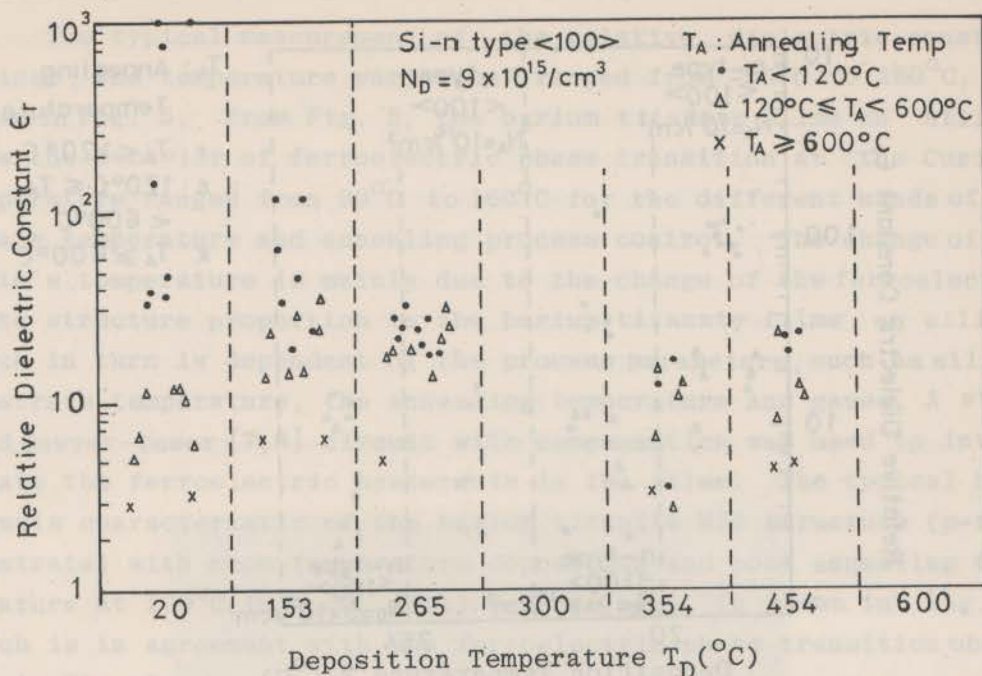

Fig. 1 Relative dielectric constant of barium titanate thin film on n-type Si <100> against the deposition temperature T_D for different annealing temperature T_A.

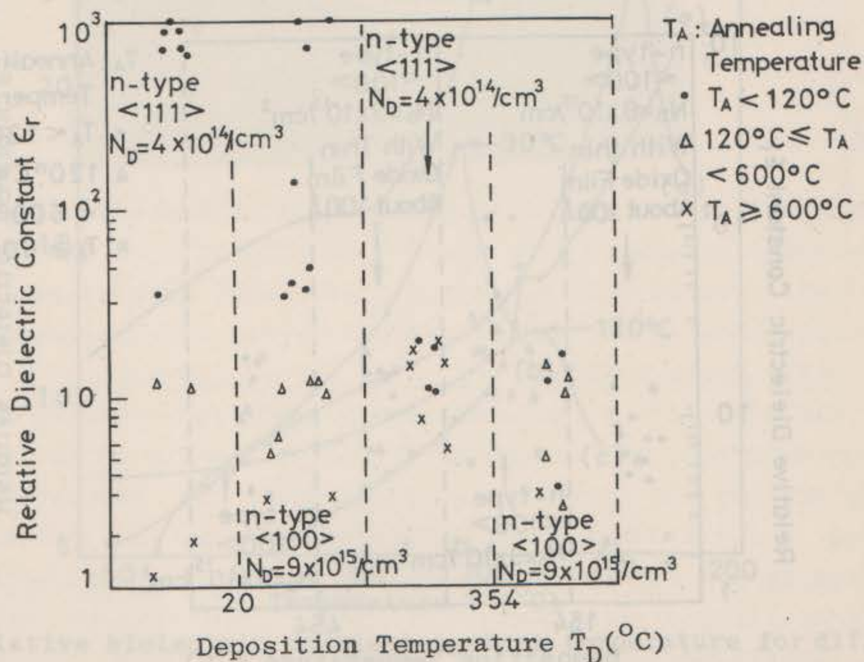

Fig. 2 Relative dielectric constant of barium titanate thin film on n-type silicon with different doping concentration against the deposition temperature T_D for different annealing temperature T_A.

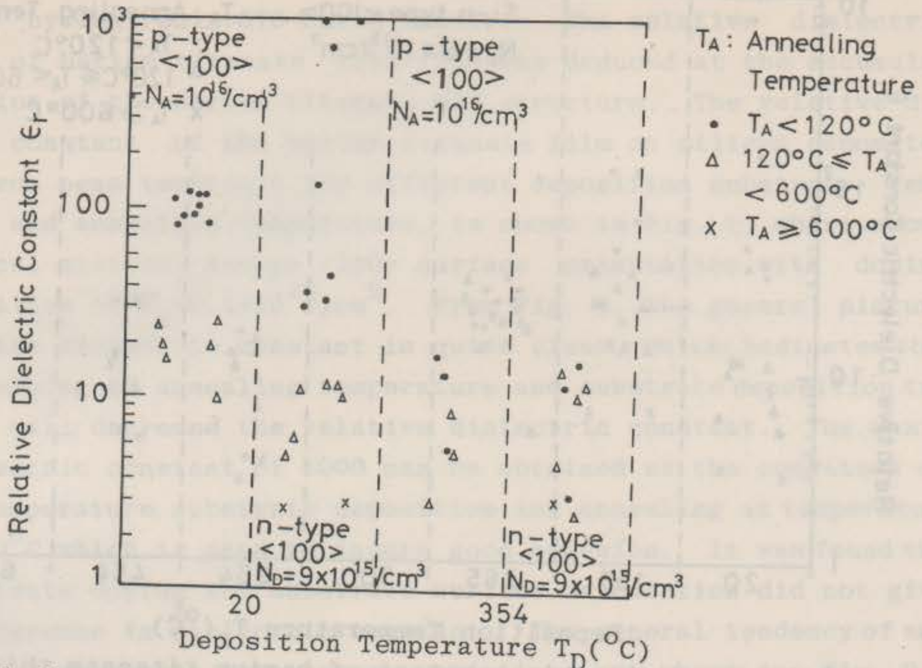

Fig. 3 Relative dielectric constant of barium titanate thin film on n and p-type Si with the same surface orientation against the deposition temperature T_D for different annealing temperature T_A.

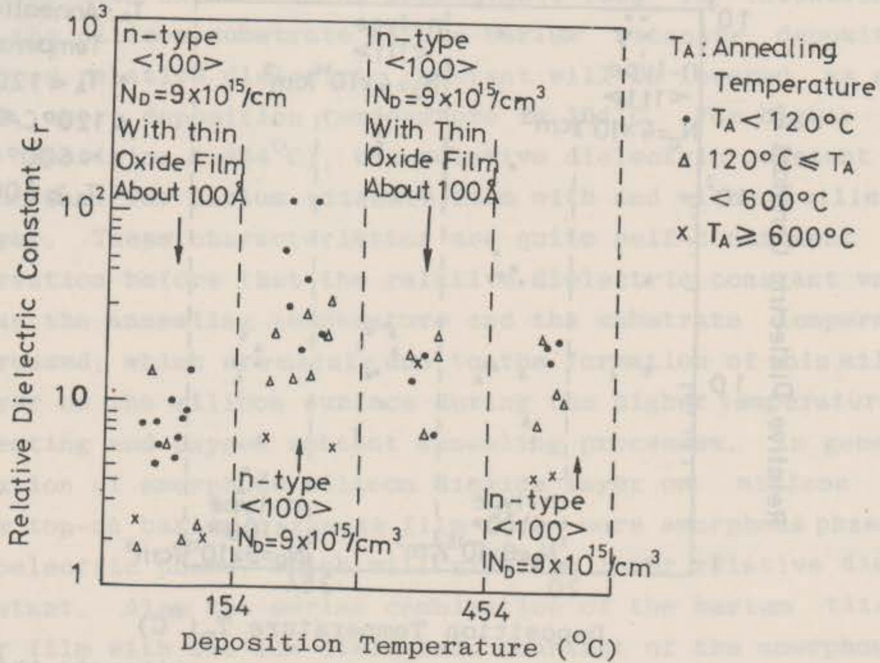

Fig. 4 Silicon oxide thin film (100A°) effects on the relative dielectric constant of barium titanate MIS structure against the deposition temperature T_D for different annealing temperature T_A.

The typical measurement of the relative dielectric constant against the temperature variation ranged from $-55^{o}C$ to $180^{o}C$, are shown in Fig. 5. From Fig. 5, the barium titanate films on silicon show the behavior of ferroelectric phase transition at the Curie's temperature ranged from $90^{o}C$ to $160^{o}C$ for the different kinds of substrate temperature and annealing process control. The change of the Curie's temperature is mainly due to the change of the ferroelectric state structure proportion in the barium titanate films on silicon which in turn is dependent of the process parameters, such as silicon substrate temperature, the annealing temperature and gases. A standard Sawyer-Tower [7,8] circuit with compensation was used to investigate the ferroelectric hysteresis in the films. The typical hysteresis characteristic of the barium titanite MIS structure (p-type substrate) with room temperature deposition and post annealing temperature at $100^{o}C$ in $N_2:O_2$ (5:1) for one hour, is shown in Fig. 6, which is in agreement with the ferroelectric phase transition observed in Fig. 5.

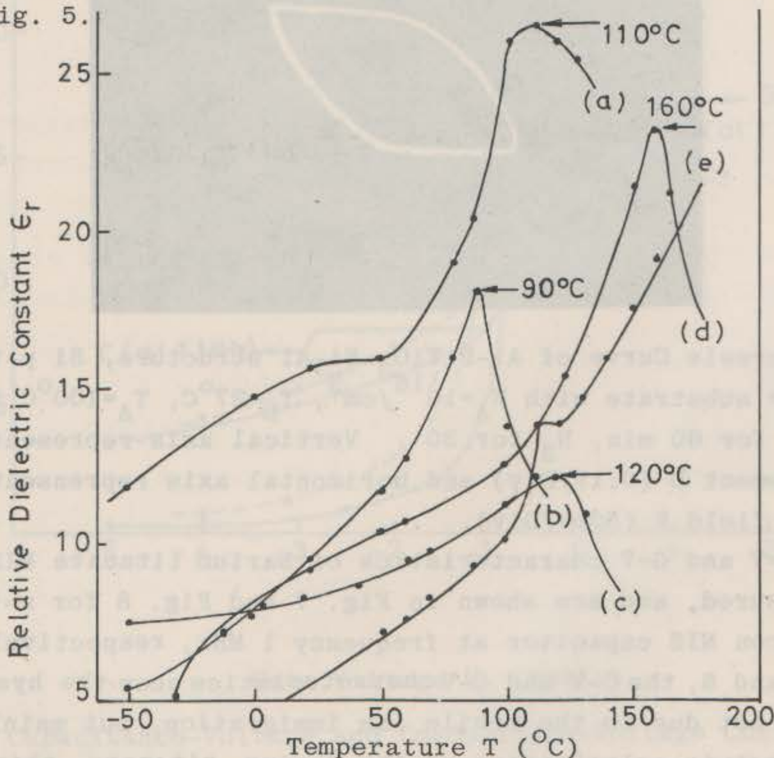

Fig. 5 Relative eielectric constant against temperature for different deposition and annealing conditions

(a) Al-$BiTiO_3$-Si-Au structure, $BiTiO_3$ thickness=4200A^{o}, Si n-type <100> substrate with $N_D=9\times10^{15}/cm^3$, $T_D=265^{o}C$, $T_A=300^{o}C$

in $N_2:O_2$=5:1 for 20 min. and N_2 for 100 min. f=1 MHz.

(b) Al-BiTiO$_3$-Si-Al structure, BiTiO$_3$ thickness=1400A^o, Si p-type <100> substrate with $N_A=10^{16}/cm^3$, $T_D=27^oC$, $T_A=100^oC$ in $N_2:O_2$=5:1 for 30 min and N_2 for 50 min, f=1 MHz.

(c) Al-BaTiO$_3$-Si-Au structure, BiTiO$_3$ thickness=1767±210A^o, Si n-type <100> substrate with $N_D=9x10^{15}/cm^3$, $T_D=27^oC$. $T_A=300^oC$ at N_2 for 2 hr., f=100 Hz.

(d) Al-BaTiO$_3$-Si-Au structure, BaTiO$_3$ thickness=1400A^o, Si n-type <111> substrate with $N_D=4x10^{14}/cm^3$, $T_D=27^oC$, no heat treatment, f=1 MHz.

(e) Same as (d), but $T_A=100^oC$ in $N_2:O_2$=5:1 for 30 min and N_2 for 50 min.

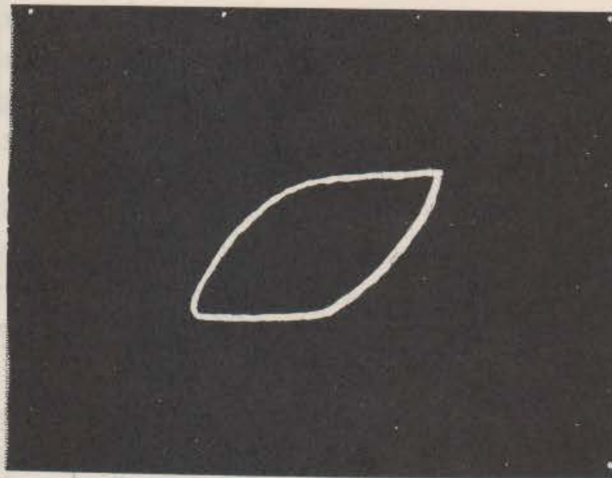

Fig. 6 Hysteresis Curve of Al-BiTiO$_3$-Si-Al structure, Si p-type <100> substrate with $N_A=10^{16}/cm^3$, $T_D=27^oC$, $T_A=100^oC$ in $N_2:O_2$ =5:1 for 60 min, N_2 for 30'. Vertical axis represents displacement D (0.1V/Div) and horizontal axis reprensents electric field E (50mv/Div).

The C-V and G-V characteristics of barium titanate MIS structure are measured, and are shown in Fig. 7 and Fig. 8 for n-type and p-type silicon MIS capacitor at frequency 1 MHz, respectively. From the Fig. 7 and 8, the C-V and G-V characteristics show the hysteresis shifting is not due to the mobile ion immigration, but mainly due to the ferroelectric polarization of the barium titanate thin films which is self-evident with the previous observation. The higher conductance of the MIS capacitor structure for both n and p-type silicon substrate is purely due to the band structure of barium titanate thin film on silicon, which tends to show the more crystalline struc-

ture of the barium titanate film, where the inversion layer carrier can inject through the barium titanate surface barrier and the deep depletion occurs in C-V measurements. When the deposition temperature or the annealing temperature is high, the injected current across the barium titanite will be lowered, the formation of silicon dioxide is possible on the silicon surface, then the injected current will be automatically reduced and the relative dielectric constant will be lowered as observed in the previous results.

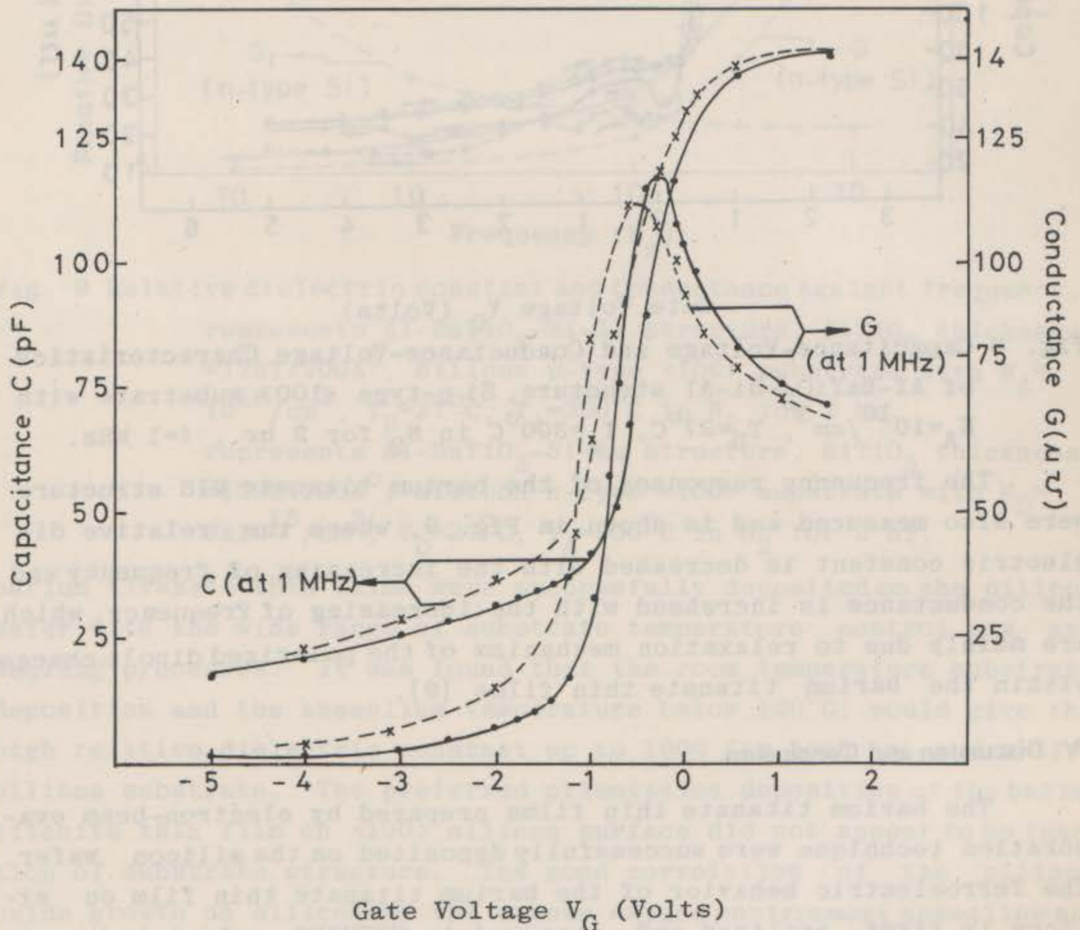

Fig. 7 Capacitance-Voltage and Conductance-Voltage Characteristics of Al-$BaTiO_3$-Si-Au structure, $BiTiO_3$ thickness=1300±120A°, Si n-type <100> substrate with N_D=9x10^{15}/cm^3, T_D=27°C, T_A=300°C in N_2 for 2hr., f=1 MHz.

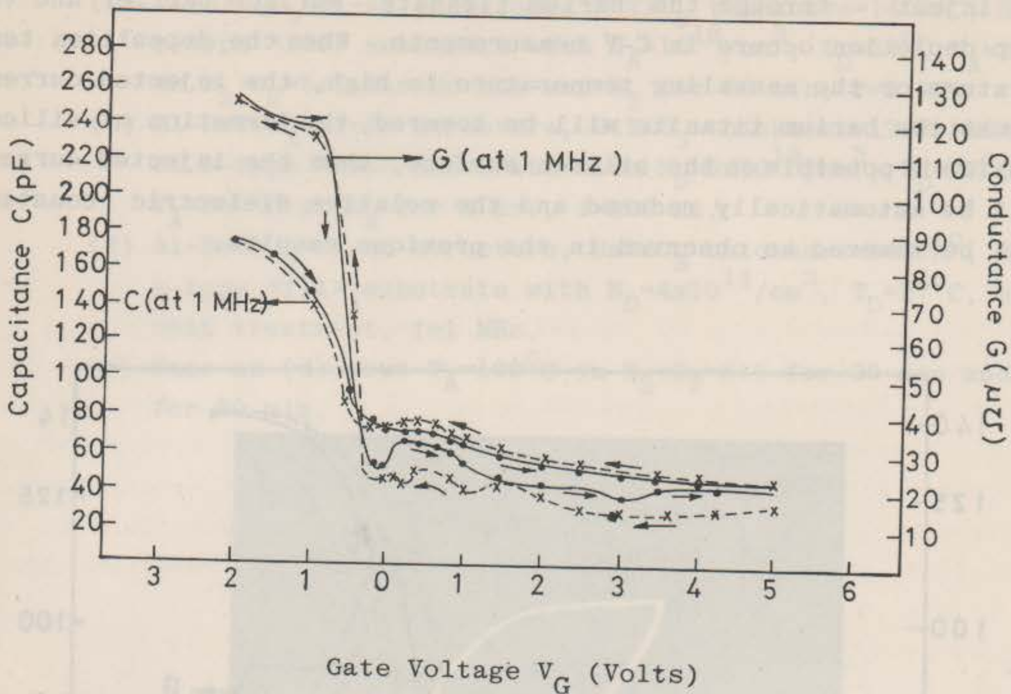

Fig. 8 Capacitance-Voltage and Conductance-Voltage Characteristics of Al-$BaTiO_3$-Si-Al structure, Si p-type <100> substrate with $N_A=10^{16}/cm^3$, $T_D=27^oC$, $T_A=300^oC$ in N_2 for 2 hr., f=1 MHz.

The frequency responses of the barium titanate MIS structure were also measured and is shown in Fig. 9, where the relative dielectric constant is decreased with the increasing of frequency and the conductance is increased with the increasing of frequency, which are mainly due to relaxation mechanism of the polarized dipole charge within the barium titanate thin films [9].

IV. Discussion and Conclusion

The barium titanate thin films prepared by electron-beam evaporation technique were successfully deposited on the silicon wafer. The ferroelectric behavior of the barium titanate thin film on silicon is first realized and observed in NCTUSRC, which had never been successfully observed and published to our knowledge on silicon substrate. The previous elaborate study [4,5] of the barium titanate thin films on silicon by RF sputtering techniques, failed to observe the ferroelectric behavior, was mainly due to the excess oxygen molecules appeared in the RF sputtering enviroment and the higher substrate temperature heating by the plasma. In this paper the

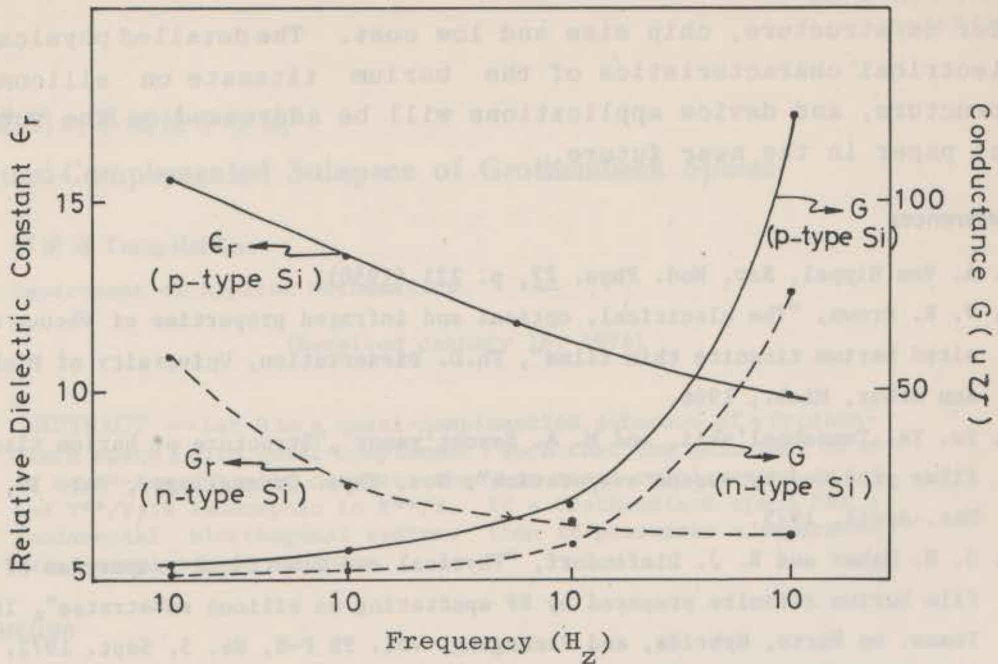

Fig. 9 Relative dielectric constant and Conductance against frequency, represents Al-$BaTiO_3$-Si-Al structure, $BiTiO_3$ thickness $=1767\pm200A^o$, Silicon p-type <100> substrate with $N_A = 10^{16}/cm^3$, $T_D = 27^oC$, $T_A = 300^oC$ in N_2 for 2 hr. represents Al-$BaTiO_3$-Si-Au structure, $BiTiO_3$ thickness $=1300\pm120A^o$, Silicon n-type <100> substrate with $N_D = 9x10^{15}/cm^3$, $T_D = 27^oC$, $T_A = 300^oC$ in N_2 for 2 hr.

barium titanate thin films were successfully deposited on the silicon wafer with the wide range of substrate temperature control and annealing processes. It was found that the room temperature substrate deposition and the annealing temperature below 120^oC, would give the high relative dielectric constant up to 1000 for both n- and p-type silicon substrate. The preferred orientation deposition of the barium titanite thin film on <100> silicon surface did not appear to be function of substrate structure. The good correlation of the silicon oxide growth on silicon by the excess oxygen environment annealing and high substrate temperature deposition, was justified to give the lower relative dielectric constant which is mainly due to the amorphous phase of the silicon dioxide on silicon.

In the present stage, the barium titanate thin film on silicon MIS structure seems promising to be used as the memory device by incorporating the present silicon planar technology, which is much sim-

pler in structure, chip size and low cost. The detailed physical and electrical characteristics of the barium titanate on silicon MIS structure, and device applications will be addressed on the subsequent paper in the near future.

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