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短通道 V 型場效電晶體研製和其電氣特性

Short Channel V-MOSFET Fabrication & Its Electrical Properties

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ABSTRACT — Short Channel n-VMOS and p-VMOS field effect transistors are designed and fabricated by using anisotropic etching solution of hydrazine and water mixture. The modified first order theory is developed for V-groove MOS structure to account for the non-uniform gate oxide thickness. It is found that the developed theory is in excellent agreement with the experimental data. VMOS fabrication techniques are discussed and the electrical properties of the fabricated discrete n-VMOS and p-VMOS devices are measured and examined.

I. Introduction

The general trend in MOS digital integrated circuits has been toward producing the monolithic large scale integration (LSI) with high chip yields, low cost and high speeds. In order to achieve this goal, the short channel MOSFET with non-critical dimensional alignment tolerances is required to give the higher packing density and the higher speed of circuit operation. For conventional MOSFET fabrication technology, the short channel length usually gives the large overlap capacitance between the gate region and the source and drain. This is the main limitation of MOS device to have the higher speed of circuit operation. Recently, a variety of fabrication technologies have been developed to minimized the parasitic capacitances, among them are: silicon gate, planox, isoplanar and ion implantation. In general, the higher complexity of fabrication steps will give lower yields and higher cost. The more recently developed V-Groove MOS (VMOS) technology [1,7] seems to be capable of producing MOSFETs with short channel, small overlap capacitances (Cgd, Cgs), high breakdown voltage, and can result in the higher packing density

of digital integrated circuits. All these advantages can be achieved by using non-critical alignment tolerance which in turn is a direct result of the orientation dependent etch (ODE) process [2,3,4,6]step.

The ODE process (or called anisotropic etch process) had been developed as a technique for dielectric isolation in integrated circuit fabrications, the new device structure which takes advantage of V-groove technology is still under development [1,5,7].

In section 2, a simplified one-dimensional theory will be developed for VMOS to account for the non-uniform oxide thickness, and some design parameters are given. The fabrication technique of V-MOS will be described and the measurements on the test device to confirm the theory will be given in section 3. Discussions and further applications of V-MOS technology will be given in the last section.

II. Theory

The basic cross sectional structure of the aluminum gate V-groove MOSFET is shown in Fig. 1. The structure is similar to that of a planar MOS transistor, except that the channel extends along the V-groove. If we choose the x-axis to be perpendicular to the V-groove plane, and y-axis to be parallel to the V-groove plane. Then, the total current flows along the channel can be written as

$$I_D=-Z\,\bar{\mu}_n Q_n(y)\frac{\partial V}{\partial y} \qquad (1)$$

where $\bar{\mu}_n$ is the average effective mobility along the channel, and is defined as

$$\bar{\mu}_n = \frac{\int_o^{d(y)} \mu_n n(x,y)dx}{\int_o^{d(y)} n(x,y)dx} \quad ;$$

$Q_n(y)$ is the inversion layer electron charge density per unit area, and is defined as $Q_n(y)=-q\int_o^{d(y)} n(x,y)dx$; Z is the width of the inversion layer channel; d(y) is the depth of the inversion layer channel and is a function of surface potential along the V-groove. It should be noted that Eq.(1) is derived under the conditions of the depletion approximation, and by neglecting the diffusion current term in the conventional current flow equation.

From the charge neutrality condition of MOS capacitor structure, the total effective metal gate charge should be equal to the

induced charges in the semiconductor which includes the total inversion layer charge and the depletion layer space charge, i.e.,

$$Q_{MT}=S_M Q_M=-S_S(Q_n+Q_B) \tag{2}$$

where Q_{MT} is the total metal charge; Q_M, Q_n, Q_B are the metal gate, inversion layer, depletion layer charge density per unit area, respectively. S_M and S_S is the effective cross sectional area of metal gate and semiconductor inversion layer, respectively.

The total metal charge Q_{MT} can be written in term of the applied effective voltage across the MOS capacitor, i.e.,

$$Q_{MT}=S_M Q_M=-\bar{C}_o(V_G-V_{FB}-\phi_S(y)) \tag{3}$$

where V_G is the gate voltage; V_{FB} is the flat band voltage which can include the metal-semiconductor work function difference, oxide charges and mobile ions in the oxide or interface; $\phi_S(y)$ is the semiconductor surface potential; $\bar{C}_o$ is the average effective oxide capacitance for the inversion layer channel, which includes the effects of the non-uniform oxide thickness over the channel and the non-equal area of metal gate and the effective channel surface area.

So the inversion layer electron density per unit area can be written as

$$Q_n(y)=-\frac{\bar{C}_o}{S_S}(V_G-V_{FB}-\phi_S(y))-Q_B(y) \tag{4}$$

Following the conventional MOS calculations, the surface potential for strong inversion and the depletion layer change can be separately written as

$$\phi_S(y)=V(y)+2\phi_{fp} \tag{5}$$

$$Q_B(y)=\sqrt{2K_S\varepsilon_o qN_A[V(y)+2\phi_{fp}]} \tag{6}$$

where ϕ_{fp} is the Fermi potential of the substrate, and V(y) is the reverse bias between the elemental section of the channel and the substrate. Putting Eq. (4), (5), (6) into Eq. (1) and integrate once along the channel, we get

$$I_D L(y)=\frac{Z\bar{\mu}_n}{S_S}\bar{C}_o\{[V_G-V_{FB}-2\phi_{fp}-\tfrac{1}{2}V_D(y)]V_D(y)-\frac{2}{3}\frac{S_S}{\bar{C}_o}\sqrt{2K_S\varepsilon_o qN_A}$$
$$[(V_D(y)+2\phi_{fp})^{3/2}-(2\phi_{fp})^{3/2}]\} \tag{7}$$

Eq. (13) is similar to the conventional MOS equation, except that the non-uniform oxide thickness $\bar{C}_o$ is taking into account.

(1) For linear region (triode region)

For very small drain voltage $V_D << 2\phi_{fp} < (V_G - V_{FB} - 2\phi_{fp})$, we let y=0, $V_D(o)=0$ at the source contact and y=L, $V_D(L)=V_D$ at the drain contact, then Eq. (13) becomes

$$I_D = \frac{Z}{L}\bar{\mu}_n \frac{\bar{C}_o}{S_S} [V_G - V_T] V_D \qquad (8)$$

where $V_T = V_{FB} + 2\phi_{fp} + \frac{S_S \sqrt{2K_S \varepsilon_o q N_A (2\phi_{fp})}}{\bar{C}_o}$ is the average turn on voltage of the channel. Since the oxide at the tip point B is thicker than the sloping wall by 1.74 time, which causes a reduced surface electric field in the semiconductor near this point and thus controls the threshold voltage of the VMOST. If the substrate is tied to the source, the threshold voltage V_T' of the tip point B is given by

$$V_T' = V_{FB} + 2\phi_{fp} + \frac{\sqrt{2K_S \varepsilon_o q N_A (2\phi_{fp})}}{C_{ob}} \qquad (9)$$

where C_{ob} is the tip point capacitance per unit area. Eq. (9) is similar to the case which considers the uniform oxide thickness of the tip point magnitude $t_p = 1.74\, t_o$ (t_o is the side wall oxide thickness) with area of S_S, so $C_{ob} = K_S \varepsilon_o \frac{1}{t_p}$. When the gate voltage is larger than V_T', Eq. (8) with effective average capacitance $\bar{C}_o$ is more accurate to account for the non-uniform oxide thickness. The conductance and transconductance can be easily calculated for the linear region as

$$g_m = \frac{\partial I_D}{\partial V_G}\Big|_{V_D=\text{const}} = \frac{Z}{L}\frac{\bar{C}_o}{S_S}\bar{\mu}_{FE} V_D \qquad (10)$$

where $\bar{\mu}_{FE} = \bar{\mu}_n + (V_G - V_T)\cdot\frac{\partial \bar{\mu}_n}{\partial V_G}$ = field effect mobility.

$$g_d = \frac{\partial I_D}{\partial V_D}\Big|_{V_G} = \frac{Z}{L}\frac{\bar{C}_o}{S_S}\bar{\mu}_n (V_G - V_T) \qquad (11)$$

(2) Saturation region

With increasing drain to source voltage (for a fixed V_{GS}) the device enters the saturation region and channel pinch-off occurs initially at point B where the oxide is thicker, and then the depleted

region spreads mostly along the BC wall of the groove. So letting $L(y)=\frac{L}{2}$, $V_D=V_{D,sat}$ in Eq. (13) for saturation condition, we get

$$I_D=\frac{2Z\bar{\mu}_n}{L}\frac{\bar{C}_o}{S_S}\{[V_G-V_{FB}-2\phi_{fp}-\tfrac{1}{2}V_{D,sat}]V_{D,sat} - \frac{2}{3}\frac{S_S}{\bar{C}_o}\sqrt{2K_S\varepsilon_o qN_A}[(V_{D,sat}+2\phi_{fp})^{3/2}-(2\phi_{fp})^{3/2}]\} \quad (12)$$

where the saturation voltage $V_{D,sat}$ can be calculated by setting $Q_n(\frac{L}{2})=0$ which gives

$$V_{D,sat}=V_G-V_{FB}-2\phi_{fp}+\frac{K_S\varepsilon_o qN_A}{\bar{C}_o^2}\left[1-\sqrt{1+\frac{2\bar{C}_{ob}^2(V_G-V_{FB})}{K_S\varepsilon_o qN_A}}\right] \quad (13)$$

The transconductance in the saturation region is

$$g_{m,sat}\doteq\frac{2Z\bar{\mu}_n}{L}\frac{\bar{C}_o}{S_S}\left[V_G-V_{FB}-2\phi_{fp}+\frac{K_S\varepsilon_o qN_A}{\bar{C}_{ob}^2}\left(1-\sqrt{1+\frac{2\bar{C}_{ob}^2(V_G-V_{FB})}{K_S\varepsilon_o qN_A}}\right)\right] \quad (14)$$

Eq. (14) is slightly different from the conventional result by using $\bar{C}_o$, $\bar{C}_{ob}$ in stead of C_o, and effective channel length $L'=\frac{L}{2}$.

The magnitude of $\bar{C}_o$ can not be easily calculated, but the approximate magnitude should be estimated. Let the average oxide capacitance be written as

$$\bar{C}_o\doteq K_S\varepsilon_o\frac{\bar{S}}{\bar{d}} \quad (15)$$

where $\bar{S}$ is the average surface area of oxide capacitor, $\bar{d}$ is the average oxide thickness. If we take the first order approximation, then letting $\bar{S}=\frac{1}{2}(S_M+S_S)$ and $\bar{d}\doteq\frac{1}{2}(t_o+t_p)$, Eq.(15) can be written as

$$\bar{C}_o=K_S\varepsilon_o\frac{S_S}{t_o}\frac{1+\frac{S_M}{S_S}}{1+(\frac{t_p}{t_o})} \quad (16)$$

where S_M and S_S represent the effective surface area of gate capacitor contact for metal and semiconductor, respectively. t_o and t_p represent the sloping wall oxide thickness and tip point oxide thickness, respectively. From the V-groove structure in Fig. 1, the aver-

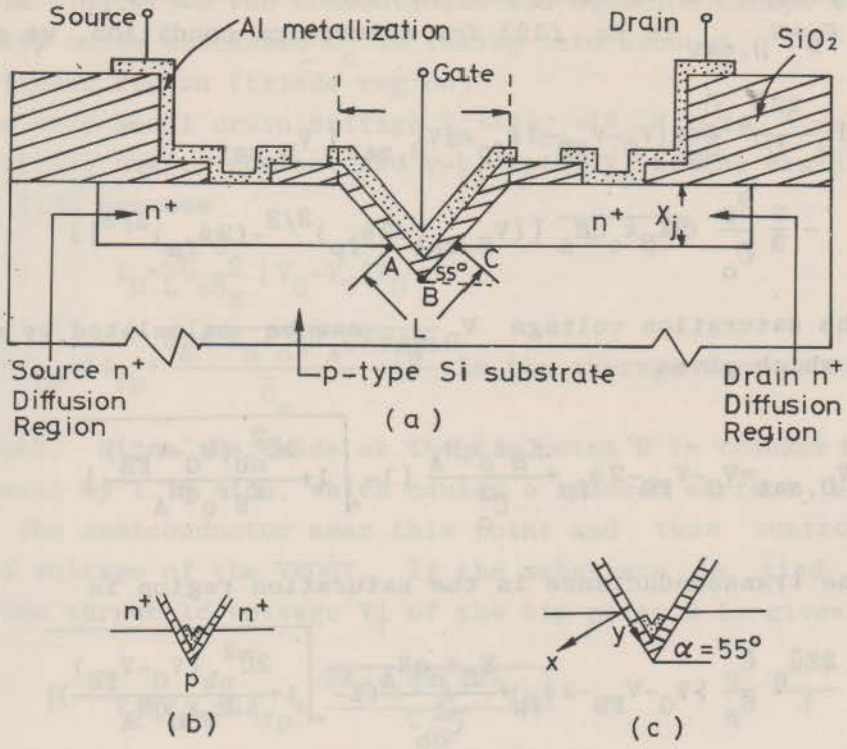

Fig. 1 (a) Schematic structure of a n-VMOS (b) Very short channel structure (c) Long channel structure

age capacitance can be written as

$$\bar{C}_o = 0.7291\ C_o\left(1-\frac{t_o}{L}\times 1.4281\right) \qquad (17)$$

where $C_o = K_S \varepsilon_o \frac{S_S}{t_o}$ = uniform oxide capacitance with cross section area S_S and the thickness t_o. From Eq. (17), we see that the correction of the oxide capacitance is strongly dependent of the ratio $\frac{t_o}{L}$, the average oxide capacitance is smaller than C_o at least by a factor of 0.7291, the smaller the channel length will give the lower capacitance. It should be noted that the analytical expression of Eq.(17) is only quantitative valid for short channel length. For longer channel length, the correction due to tip point thick oxide effect on $\bar{C}_o$ is negligible.

III. Fabrication Techniques and Measurements

The test samples of V-groove n- and p-channel were fabricated

by four mask technology with channel width of Z=55μ and V-groove window W of 5μ, 7.5μ,10μ and 12.5μ. The <100> surface orientation of Si substrate with resistivity of n-type 0.5-1.15Ω-cm and p-type 3-5 Ω-cm for n channel and p-channel respectively, were chosen. Junction depth of source and drain diffusion were controlled about 2.5μ and 2.8μ for p- and n-channel, respectively. The main process steps are listed as followed:

1. Strictly clean the Si <100> wafer surface.
2. Thermally grow a layer of SiO_2 about 8000A°.
3. Use the 1st mask to define the source and drain diffusion region photo-lithographically.
4. Boron predeposition for p-channel (phosphorus predeposition for n-channel).
5. Remove Boron glass (Remove phosphorus glass).
6. Source-drain drive-in.
7. Use the 2nd mask to define the V-groove etching window.
8. V-groove etch by hydrazine-water mixture (2:1 by volume ratio) heated to 100°C.
9. Wafer surface cleaning.
10. Thermally grow the gate oxide (1000A°) by using dry O_2.
11. Annealing and gettering.
12. Use the 3rd mask to open the source and the drain ohmic contact.
13. Al metallization.
14. Use the 4th mask to define the metallization pattern.
15. Sintering.

The typical I_D-V_{DS} characteristics of n- and p-channel are shown in Fig. 2 and Fig. 3, respectively. For n-VMOS, the channel length L is 4μ, the threshold voltage V_T is 1.55 volt (enhancement), the breakdown voltage is about 35 volt. For p-channel, the channel length L is 2μ, the threshold voltage V_T is 5.3 volt, and the breakdown voltage is about 50 volt. In order to fully characterize the process and the resulting devices, the n- and p-channel of VMOS were fabricated with channel length ranged from 0.2μ to 10μ. Measurements carried out on the test devices include I-V characteristics, threshold voltage, transconductance at the linear region and saturation region, breakdown voltage and field effect mobility. The transconductance at saturation region for p-channel VMOS with four channel length L= 0.2μ, 2μ, 7μ, 8μ, are shown in Fig. 4, the linear region transconduc-

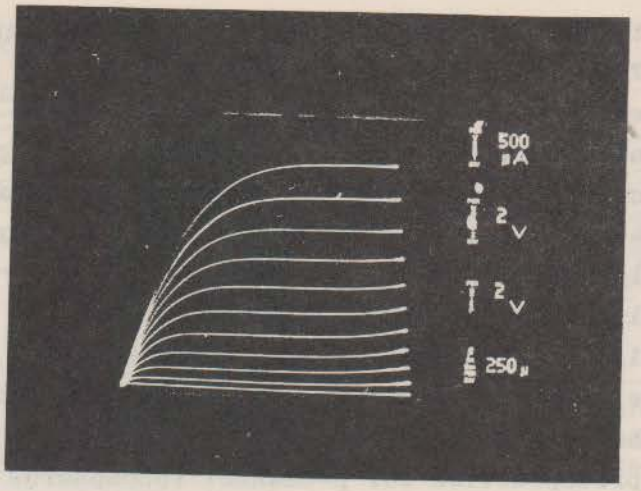

Fig. 2 I_D-V_{DS} characteristic of a typical n-VMOS, Z=55μm, L=4μ , V_T=1.55 volt, V_{BD}=35 volt.

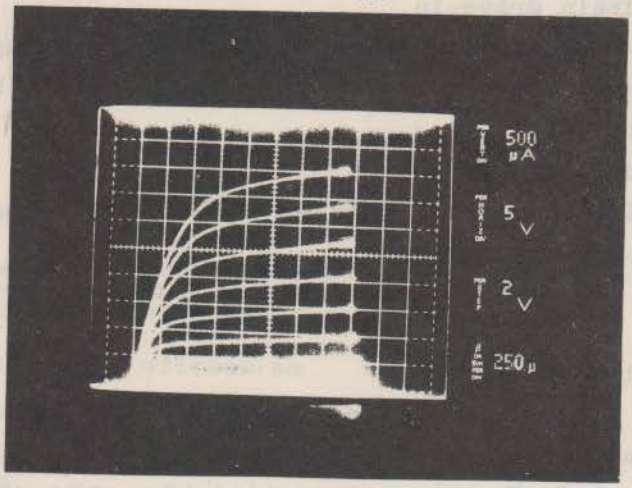

Fig. 3 I_D-V_{DS} characteristics of a typical p-VMOS, Z=55μm, L=2μm, V_T=5.3 volt, V_{BD}=50 volt.

tance versus (V_G-V_T) curves were measured with source and drain voltage kept at V_{DS}=200 mV to maintain the surface channel as uniform as possible, then the field effect mobility was deduced by Eq. (10) with the effective oxide capacitance $\bar{C}_o$ equal to the side wall oxide capacitance $\bar{C}_o$ (thickness t_o=1000A°). The field effect mobility curves are shown in Fig. 5. The gate voltage dependent mobility shows the similar shape by comparing with the conventional planar MOS mobility, but the field effect hole mobility is strongly dependent of the channel length, i.e., the shorter the channel length the lower the field effect hole mobility will be. If the channel length

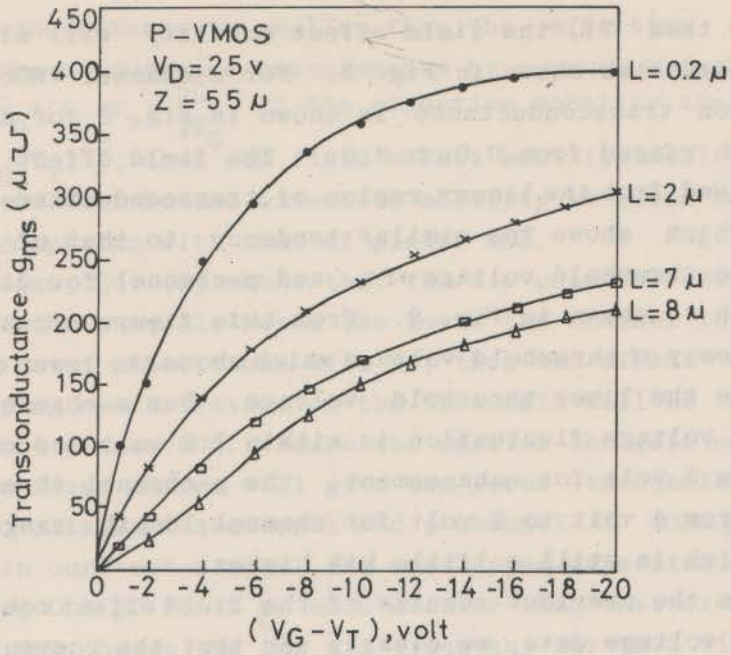

Fig. 4 p-channel saturation region transconductance g_m v.s. gate voltage (V_G-V_T) for different channel length L=8μ, 7μ, 2μ, 0.2μ.

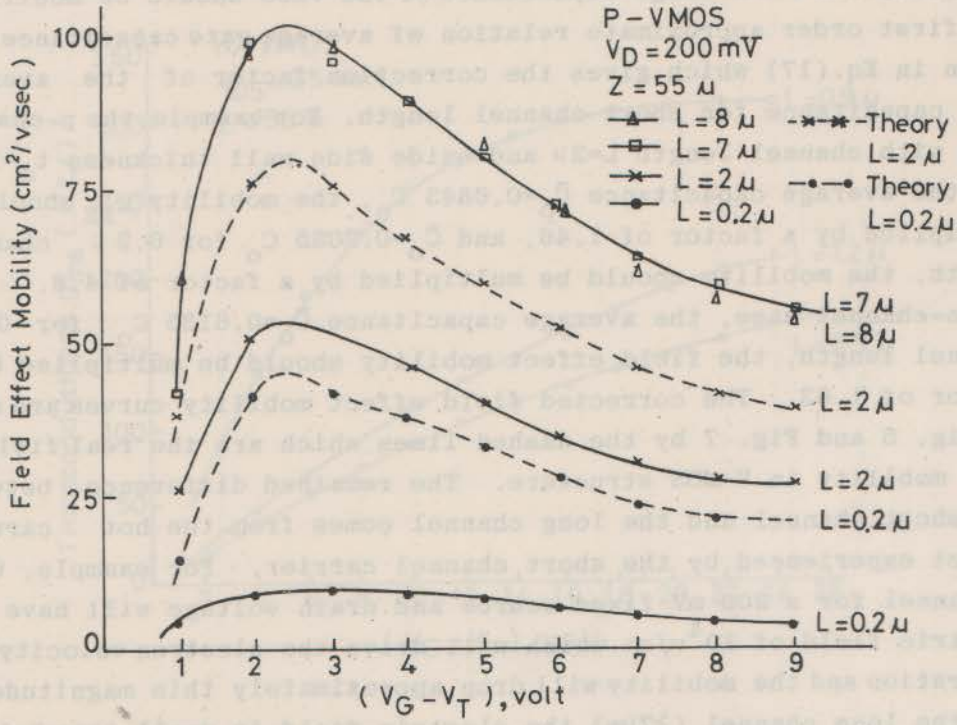

Fig. 5 Field effective hold mobility μ_{FE} v.s. gate voltage (V_G-V_T) for different channel length L=8μ, 7μ, 2μ, 0.2μ.

is larger than 7μ, the field effect mobility will almost give the some magnitude as shown in Fig. 5. For n-channel VMOS, the saturation region transconductance is shown in Fig. 6 for different channel length ranged from 0.9μ to 8.9μ. The field effect electron mobility deduced from the linear region of transconductance, is shown in Fig. 7, which shows the similar tendency to that of the p-channel VMOS. The threshold voltage of n- and p-channel for different channel length is shown in Fig. 8. From this figure we can see the general tendency of threshold voltage which shows the lower channel length will give the lower threshold voltage. For n-channel VMOS, the throshold voltage fluctuation is within 1.5 volt and can be controlled below 3 volt for enhancement, the p-channel threshold voltage changes from 4 volt to 9 volt for channel length ranged from 0.2μ to 8μ, which is still a little bit higher.

From the previous results of the field effect mobility and the threshold voltage data, we clearly see that the conventional standard MOS theory does not give a proper feature of VMOS. The modified theory developed in section two, should be examined. We have shown in Eq.(7)that the average capacitance of the VMOS should be modified, the first order approximate relation of average gate capacitance was given in Eq.(17) which gives the correction factor of the average gate capacitance for short channel length. For example, the p-channel VMOS with channel length L=2μ and oxide side wall thickness t_o=1000 A^o, the average capacitance $\bar{C}_o$=0.6843 C_o, the mobility μ_{FE} should be multiplied by a factor of 1.46, and $\bar{C}_o$=0.2085 C_o for 0.2 μ channel length, the mobility should be multiplied by a factor of 4.8. For the n-channel case, the average capacitance $\bar{C}_o$=0.6135 C_o for 0.9 μ channel length, the field effect mobility should be multiplied by a factor of 1.63. The corrected field effect mobility curves are shown in Fig. 5 and Fig. 7 by the dashed lines which are the real field effect mobility in V-MOS structure. The remained difference between the short channel and the long channel comes from the hot carrier effect experienced by the short channel carrier. For example, 0.2μ p-channel for a 200 mV fixed source and drain voltage will have the electric field of 10^4v/cm which will drive the electron velocity into saturation and the mobility will drop approximately this magnitude[10]. For the long channel (>7μm), the electric field is small than $3x10^2$V/cm (V_{DS}=0.2V), hence the mobility is still at the low electric field value. It should be noted that the field effect mobility deduced

from the transconductance is smaller than the effective mobility deduced from the conductance measurements by a constant factor. From Eq. (18) $\bar{\mu}_{FE}=\bar{\mu}_n+(V_G-V_T)\frac{\partial\bar{\mu}_n}{\partial V_G}$, if the effective mobility can be written as $\mu_n=\alpha(V_G-V_T)^{-\beta}$, then the field effect mobility will be $\bar{\mu}_{FE}=(1-\beta)\bar{\mu}_n$ where $0<\beta<1$. So the effective mobility is quite reasonable magnitude by comparing with that of planar MOS. As regard to the threshold voltage, Eq. (9) shows that the tip point of VMOS controls the turn-on of the channel, hence the lower the channel length, the lower the tip point capacitance will be, then the effect of fixed charge and doping concentration on the threshold will be stronger. than that of the planar MOS. Hence the smaller the gate oxide thickness and oxide fixed charge will give the lower threshold voltage. The breakdown voltage of n-channel and p-channel is always larger than 30 volt in our test sample, the overlapped capacitance is only at the order of 0.4 pF which is much smaller than that of the conventional planar MOS, hence the cut off frequency for VMOS will be 400 MHz.

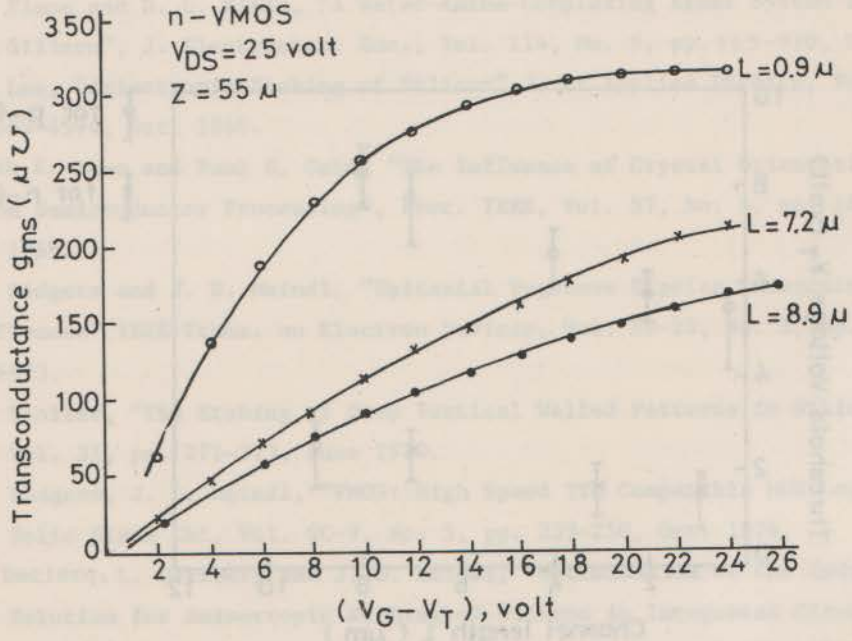

Fig. 6 n-channel saturation region transconductance g_m v.s. gate voltage (V_G-V_T) for different channel length L=8.9μ, 7.2μ, 0.9μ.

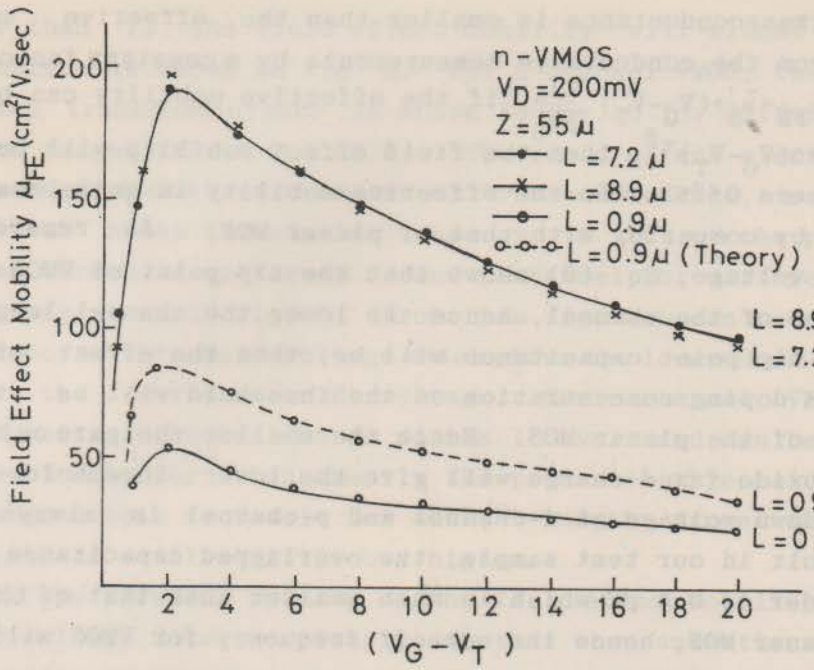

Fig. 7 Field effect electron mobility μ_{FE} v.s. gate voltage (V_G-V_T) for different channel length L=8.9μ, 7.2μ, 0.9μ.

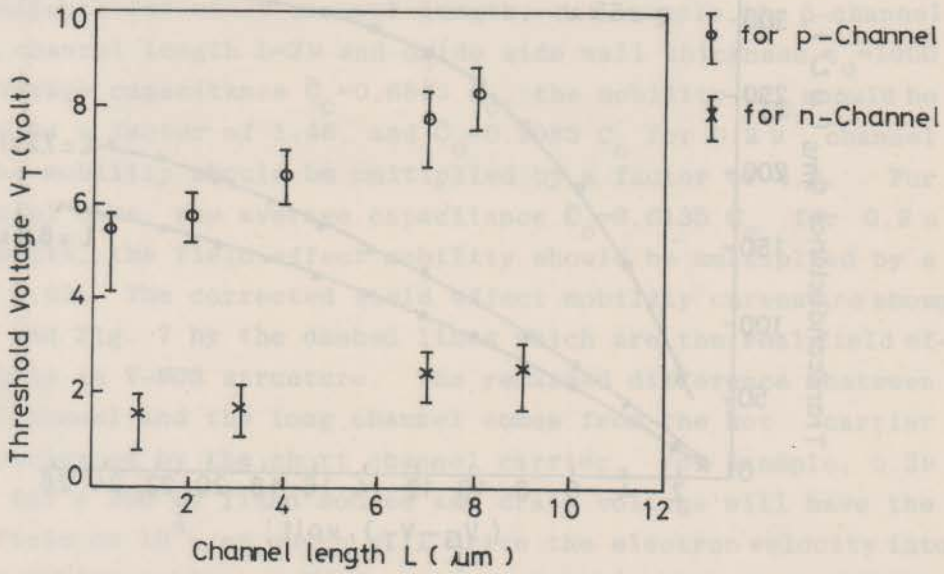

Fig. 8 Threshold voltage V_T v.s. channel length L for n-channel and p-channel.

IV. Conclusion

V-groove n- and p-channel MOSFET are fabricated by using anisotropic etching solution of hydrazine and water mixture. The ultra-short channel length for both n-channel (0.9μm) and p-channel (0.2μm) are realized by using the non-critical alignment tolerance of V-groove technology. The process results in a short channel, low output conductance, high transconductance, small gate capacitance, and hence high cut-off frequency by comparing with the conventional planar MOS technology.

The modified first order theory is now developed for VMOS, which is in excellent agreement with the phenomena observed in short channel VMOSFETs operation. Some designed parameters of VMOS are given in the text. VMOS technology is not only capable of high speed operation, but also will give the high packing density of integrated circuits.

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