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積體注入邏輯元件之參數與性能研究
I^2L Device Parameters and Performance Investigation

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Abstract—— The optimized mask design and process consideration of I^2L are presented which can achieve good flip-flop and ring oscillator performance. Detailed DC and AC experimental analysis for the discrete structure has been investigated. Standard Bipolar Process is used which is compatible to other bipolar design. A new layout and process technique, Washed Emitter, is introduced which achieve to improve extrinsic and intrinsic efficiency greatly although there is some drawbacks in yield.

I. Introduction

Since its introduction in 1971, Integrated Injection Logic (I^2L) has received a large amount of industrial development effort. Attractive features of this logic form are compatibility with isolated bipolar junction transistor (BJT) processing for linear circuitry or current mode logic onchip, easy of layout and high packing density, and very efficient medium speed performance. Only BJT-compatible I^2L is considered here, as opposed to the 4-mask form used for some LSI memories and microprocessors. The standard bipolar process (SBP) schedule, table 1, is used as a basis for studying the effect of process parameter vaviation on device characteristics. This yields information on the capabilities of I^2L available to the circuit designer "as is" using a proven process, and also establishes a standard of comparison for advanced BJT-compatible structures now under consideration.

Table 1

Standard Bipolar Process

Substrate <100> p type 1-5 Ωcm "J" material

Arsenic buried layer predep 1 hr dry O_2 at 1200°C, drive-in 1 hr dry 0_2 at 1200°C

Epitaxial layer 2½ μ to 6 μ

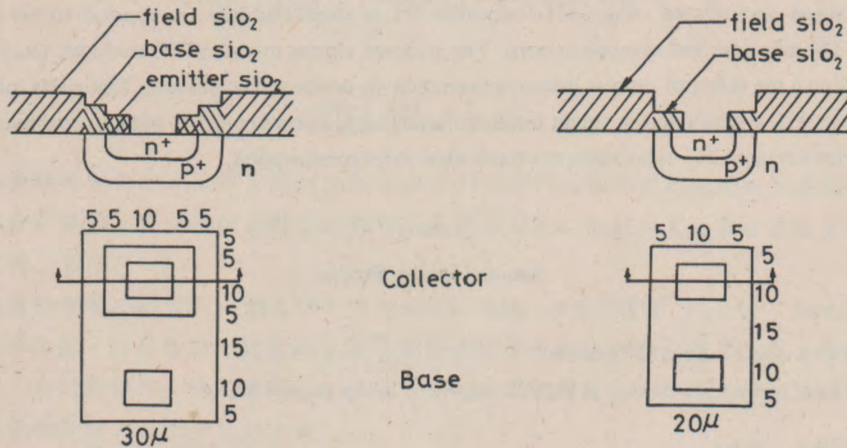
As doped 1050°C	12 min doped, 3 min undoped
	AsH_3 = 11 glass ball
	SiH_4 = 35 cc/min
	0_2 = 15 glass
	N_2 = 9.5 stainless steel ball, main & diluent

Isolation oxidation	1200°C 10/25/5/5 min dry 0_2, wet 0_2, dry 0_2, dry N_2
Isolation predep	1100°C B_2H_6 60 min
Isolation drive-in	1200°C 85/5 min dry 0_2, dry N_2

Base predep 950°C B_2H_6 30 min, 0_2

Base drive-in 1000°C 45/60/5/10/2 min, dry O_2, wet O_2, dry O_2, dry N_2
Emitter predep 1025°C $POCL_3$ (15min)
Emitter drive-in 900°C 10/10/10/2 min dry N_2, wet N_2, dry N_2
.1 μ E-beam Al

The SBP-I^2L investigation is divided into study of device and circuit design by way of mask layout, and study of the effect of process variation on devices and circuits. By devising a complete test mask set, a controlled set of experiments results. Process ambiguities are eliminated by consideration of different devices on a given chip in the former case, and layout ambiguities are eliminated by consideration of identical device and circuit topologies for several wafers in the latter case. The 40 pin limit necessitated laying out two metallization interconnection patterns to access all devices and circuits of the single mask set. The metallization patterns were interleaved at photorepetition to permit adjacent fabrication of all the structures on pairs of chips across a wafer. Test devices with fanout of one, two, and three, with base contact adjacent to or away from the injector bar, and with lateral pnp base width = 7.5, 10, and 15 μ are included. Also present are vertical NPN and a lateral PNP geometries to permit comparison to existing device data. Several ring oscillators (RO) are included to provide realistic measurement of dynamic on-chip performance in the absence of external parasitic loading. Separate-injector I^2L buffers driving on-chip emitter followers are used to measure ring oscillator speed with an oscilloscope. Fanout of one and fanout of two RO's are present. In addition is included an RO using the emitter wash technique (Fig. 1) borrowed from microwave device processing. This is an attempt to achieve improved extrinsic and intrinsic efficiency through reduced gate size, by using the same minimum-feature oxide window for both collector diffusion and contact hole (Fig. 1).



(emitter contact hole is minimum feature size)
gate bottom area=1650 μm^2
n^+ bottom area=400 μm^2
$\frac{A_c}{A_E} \doteq \frac{1}{4}$ (sidewall neglected)

(emitter is minimum feature size)
gate bottom area=900 μm^2
n^+ bottom area=100 μm^2
$\frac{A_c}{A_E} \doteq \frac{1}{9}$

Utilize side diffusion of emitter (0.8xj $\doteq$ .7 μm here) to allow use of minimum feature size emitter diffusion. C_{BC} is reduced. 2:1 A_E is reduced. $\frac{A_C}{A_E}$ goes down $\doteq$ 2:1 so that β_u requirement is increased.

Figure 1 Washed Emitters

A six gate toggle flip-flop design is incorporated on the test chip to investigate I^2L performance on a circuit of practical importance. This design is borrowed from the 7400 series TTL D-type flip-flop.

The SBP was used with several permutations of epitaxial resistivity and thickness. All wafers received identical pre- and post-epitaxy processing. Two permutations, wafer No. 11 and No. 12 were chosen for detailed analysis. Low forward NPN current gain of about 50 resulted on both wafers due to unexpected variation of phosphorus pre-deposition furnace transient response characteristic. Two wafers from a previous high β process run, No. 1, and No. 2 were included in the testing procedure to provide additional data. Process information for these four wafers is summarized in the inset of figure 2.

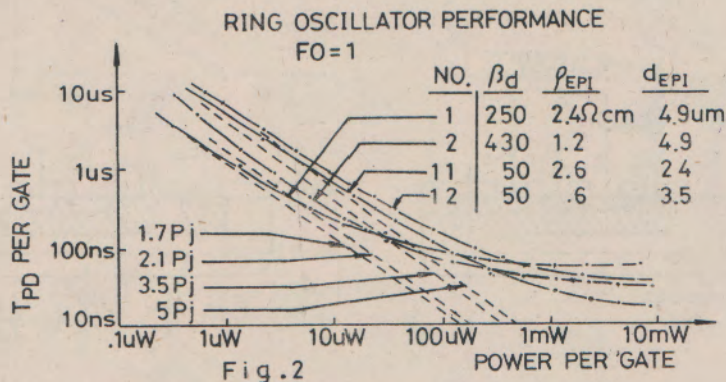


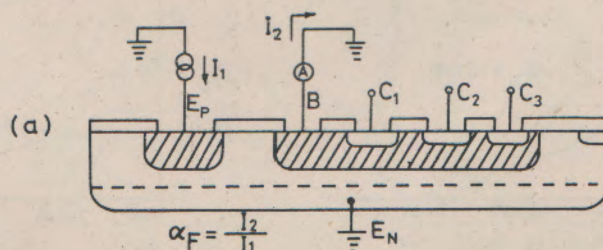
Fig.2

II. Device Electrical Parameters

The lateral PNP and inverse-mode vertical NPN transistor electrical parameters are presented below. Individual device characterization is of central importance both in understanding I^2L operation and limitations, and in allowing accurate computer simulation.

1. Lateral PNP (Injector) Transistor.

The injector region forms a lateral PNP transistor with the base of the NPN device of the I^2L gate. The injector is almost always operated at a constant forward bias condition, so the major electrical parameters are the forward and reverse DC current transfer ratios α_F and α_R, and the saturation current I_S. Parameter α_F and α_R can be measured on a curve tracer, with the lateral PNP device operated in the common-base connection and the measurement carried out at zero collector-base voltage (Fig. 3 a,b). It may be measured in a common-base DC test set-up; a voltage source and variable resistor (typically 100k to 1G) provides base drive, and a voltage source is connected in series with a current measuring electrometer at the collector node. Zero collector-base voltage was used for the



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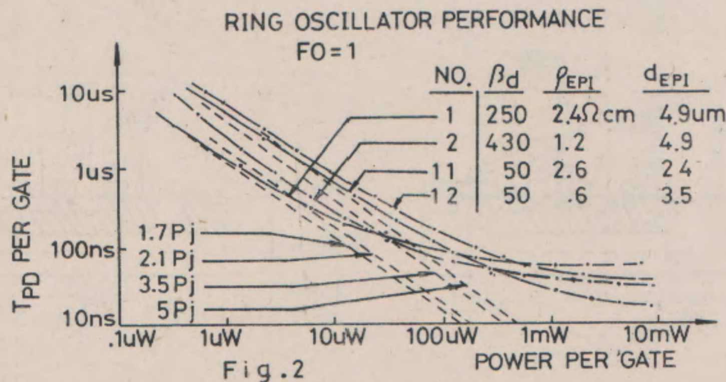

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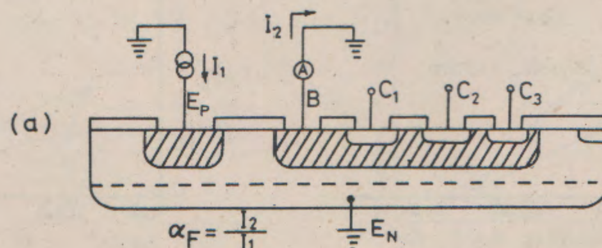

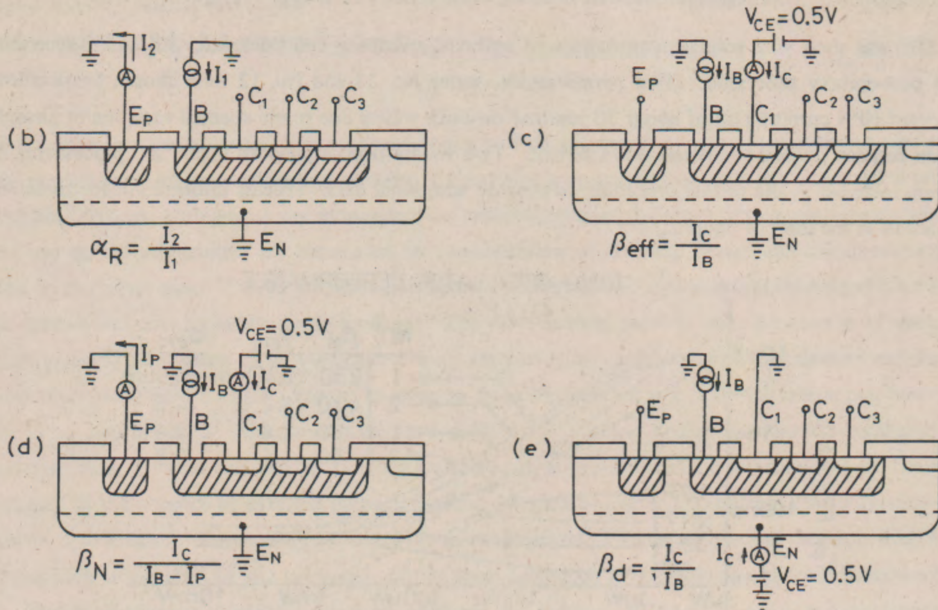

Figure 3 Measurement setup for α_F, α_R, α_{eff}, β_N and β_d.

measurement. A digital voltmeter is used to monitor the emitter-base voltage V_{BE}. The logarithm I_C is plotted with respect to V_{BE} over a wide range of collector currents (five orders of magnitude or more), allowing extrapolation of the resulting straight line plot to $V_{BE} = 0$ giving I_S.

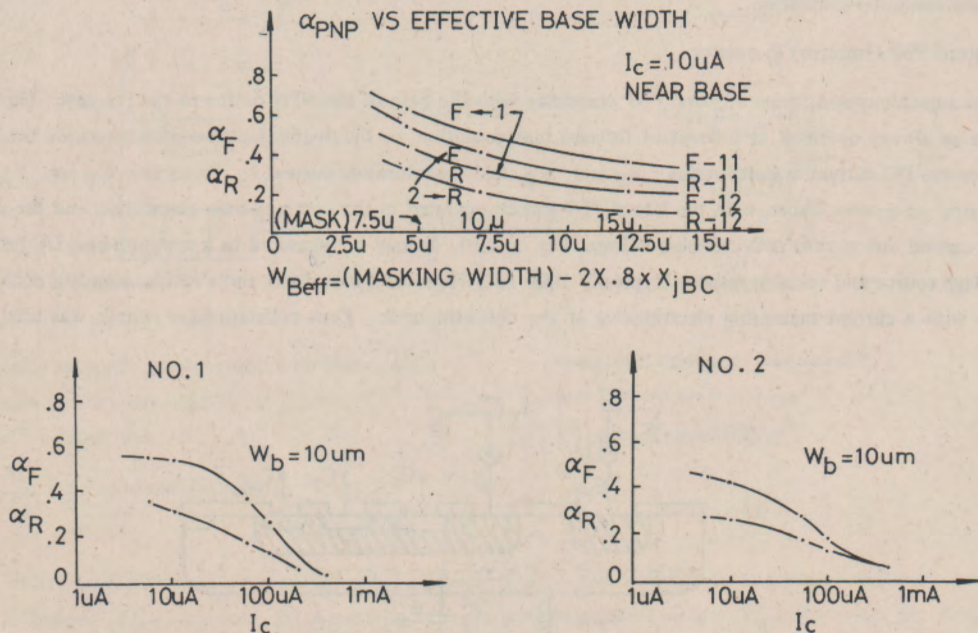

Fig. 4

Figure 4 through 6 show α_F and α_R plotted as a function of collected current I_C and typical extrapolation I_S plots are shown in Figure 7.

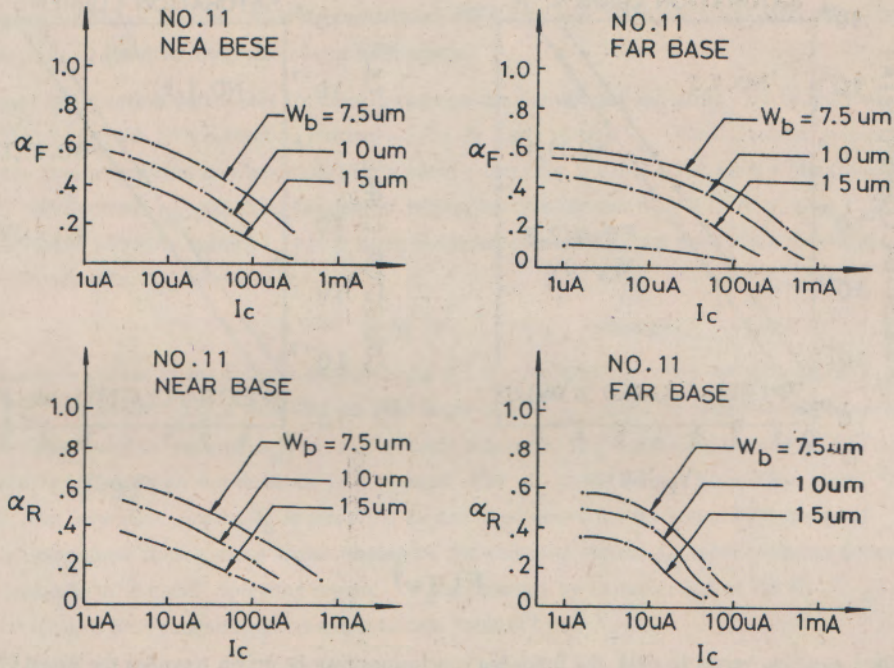

Fig.5

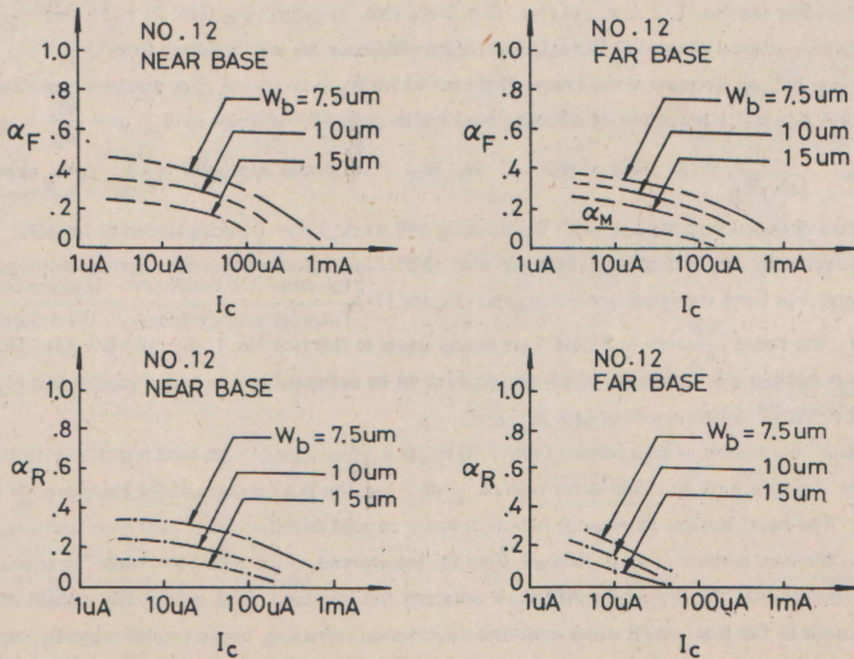

Fig.6

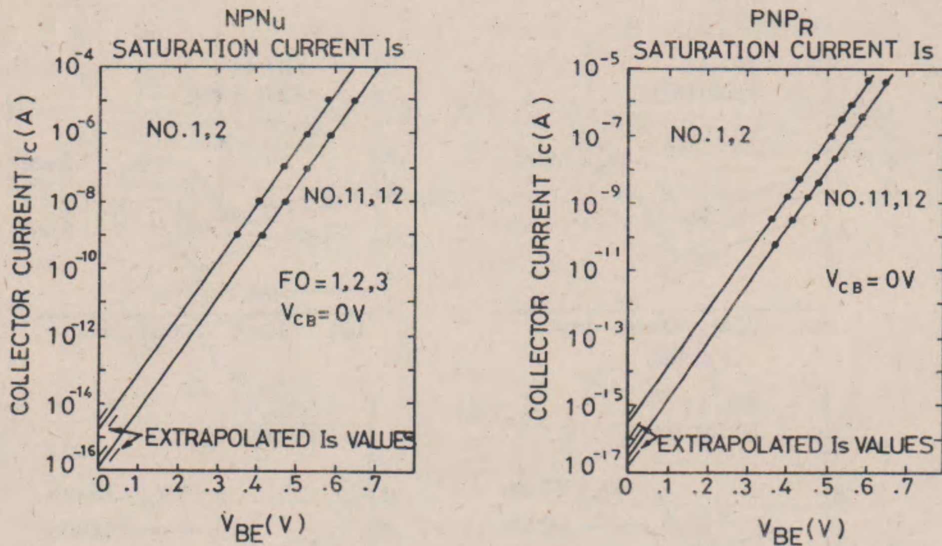

Fig.7

From the α_F, α_R versus I_C data, the following conclusions may be drawn regarding the lateral PNP transistor DC current transport ratios:

(1) Increasing impurity concentrations in the epitaxial layer results in lower α_F and α_R at a given current density. For the No. 1, 2 case, epi (No. 2) = 2 epi (No. 1) giving α_F (No. 2) = .55 and α_F (No. 1) = .4. Nearly proportional changes in RO extrinsic region efficiency are seen resulting from this.

(2) Both α_F and α_R decrease as the lateral PNP base width W_B is increased. For practical masking dimensions, Figure 4 shows 2:1 reduction of effective base width gives 50% increase in α_F. $\beta = \frac{Q_E}{Q_B} = \frac{Q_E}{W_B N_{epi}}$, so $\alpha_F = \frac{1}{1+K_2W_B}$; the solpe of the α vs. W_B curve should approach $\frac{Q_E}{N_{epi}}$ as W_B approaches zero. The data obtained suggests 5 μ with W_B masking will work; 7½ μ masking is seen to be safe.

(3) α_F is generally larger than α_R because the NPN base region is larger than the injector region supplying the gate. For Fo=1 minimum geometry gates (Figure 1) $\frac{\text{Injector-Gate Periphery}}{\text{Total Injector Periphery}} \div \frac{\text{Injector-Gate Periphery}}{\text{Total Gate Periphery}}$ =1.67; the ratios $\frac{\alpha_F}{\alpha_R}$ seen in Figure 4 are nearly equal to this (for No. 1, the ratio is 1.83). This calculation neglects bottom side injection, which should tend to be deflected by the buried layer. Also neglected is the effect of the n^+ collar on side-of-gate injection.

(4) α_F and α_R fall-off at high current (above 10 to 20 μA) because of high level injection effects and resistive voltage drops in bulk semiconductor regions. For α_R, this is a function of the placement of the base contact, "Far base" devices experience fall-off at lower current densities than "near base" devices. ("Far base" means the base contact is most distance from the injectorend of the NPN base, while "near base" means the base contact is at the end of the NPN base adjacent the injector.) This is primarily a result of resistive voltage drops in the base which cause emitter-base junction debiasing, hence greater minority carrier injection at greater distances from the injector (which acts as the collector for reverse operation).

2. Vertical NPN Transistor

In an I^2L gate the NPN transistors are operated in an inverse mode with respect to the conventional usage. In addition, multiple fanout gates share both the common-base and common-emitter regions with only the collectors processing separate diffused regions. This unconventional NPN structure yields electrical parameters considerably different from those of standard integrated circuit NPN devices.

The principal DC electrical parameters for these transistors are the upward and downward DC current gain ratios β_{eff} (or β_N) and β_d, the NPN saturation current I_S, and the Early voltage V_A. The DC current gain ratios can be measured in the commen-emitter configuration with a curve tracer (Fig. 3 c,d,e). The ratio of the collector current I_C to the base drive current I_B, with collector-emitter voltage specified (hence V_{CE}=0.5 volt), gives β_{eff}. Measurement of the collected parasitic current I_p which flows to the injector and adjacent gates when the emitter-base junction is forward biased gives β_N defined by

$$\beta_N \triangleq \frac{I_C}{I_B - I_P} \Big| \quad V_{CE} \quad \text{constant}$$

β_N is the parameter needed in the Estreich-Dutton-Wong I^2L macromodel for circuit simulation (1). β_{eff} is easier to measure β_N, and usually β_N is from 20% to 50% larger than β_{eff}, depending upon the fabrication and layout details (over a single wafer the ratio of β_{eff} to β_N is nearly constant). β_d is measured exactly as β_{eff} is measured, except the emitter and collector terminals are interchanged. For $\beta_d > 30$, there is little effect upon I^2L dynamic performance. The saturation current I_S is measured as described above for the lateral PNP transistor. The Early voltage V_A is determined from a curve tracer display of the collector current I_C versus collector-emitter voltage V_{CE} in the transistor's "normal" operating region. V_A is obtained by extrapolation of the (I_C, V_{CE}) curves for various base currents to their common voltage-axis intercept point at I_C=0.

Figure 8 and 9 show the current dependence of β_{eff} for the four process groups. Figure 9 shows a typical value of β_N at a current level of 10 μA. β_d is given at 100 μA collector current and .5V collector-emitter voltage for all groups in the inset of Figure 2. Figure 7 shows a typical curve of the I_C versus V_{BE} characteristics for devices from the four process groups.

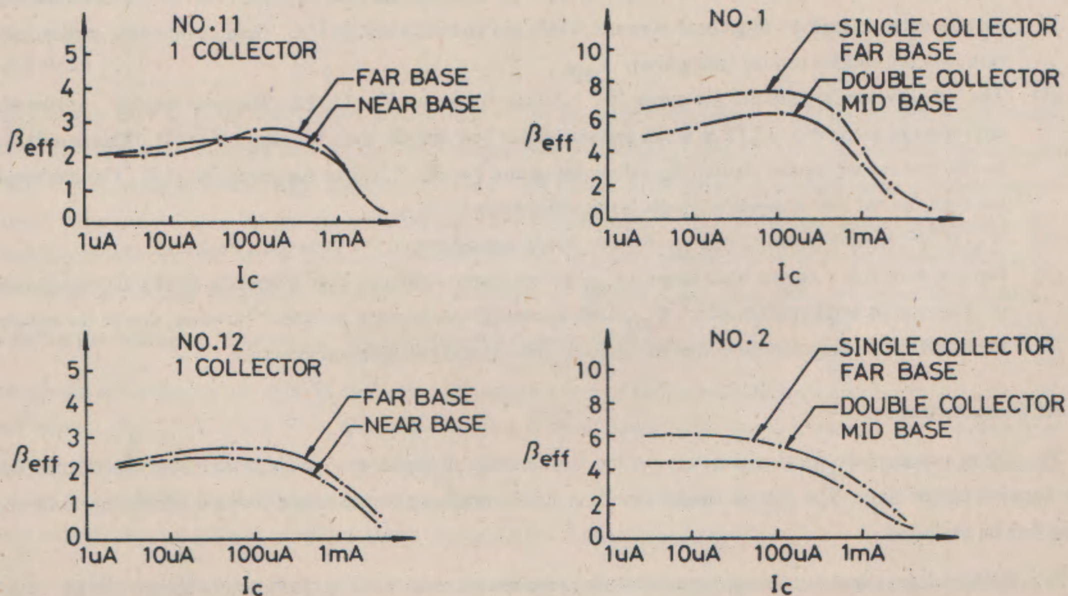

Fig.8

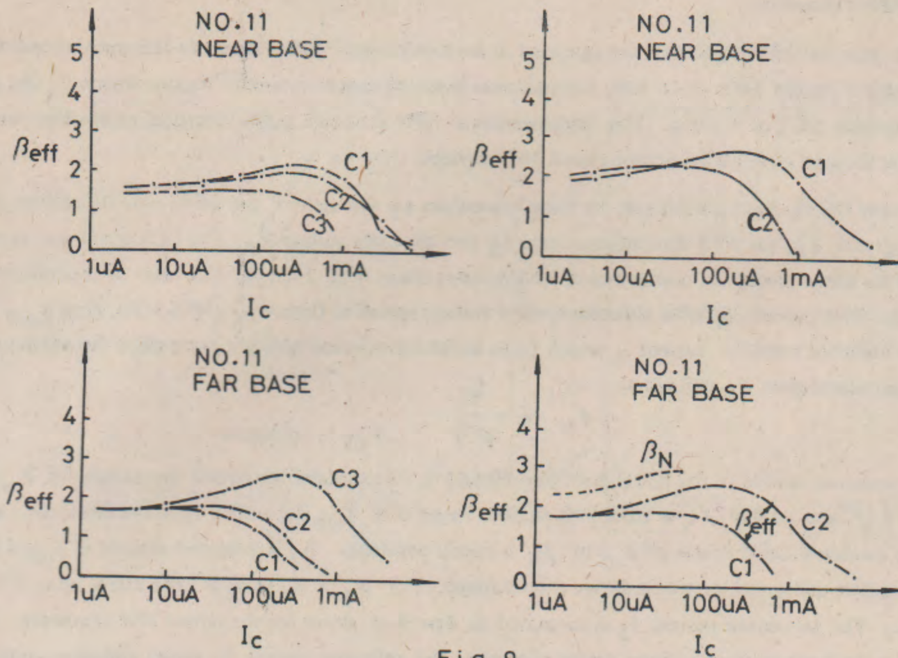

Fig.9

From the β_{eff} versus I_C data, the following conclusions may be drawn regarding the NPN transistor:

(1) Some peaking in β_{eff} can be observed for group No. 11 and No. 12. This is caused by high level injection effects resulting in conductivity modulation within the epitaxial part of the NPN emitter. Lower epitaxial impurity concentration or thicker epitaxial layer leads to stronger peaking.

(2) Collectors most distant from the base contact exhibit high-current β_{eff} fall-off (figures 8 and 9) at lower collector current densities than do collectors directly adjacent the base contact. This is due to lateral base voltage drops caused by large base currents which are characteristic in I^2L. Greater minority carrier injection into the emitter results, giving lower β_{eff}.

(3) The β_{eff} values are greater for group No. 1,2 than for group No. 11, 12. The base doping under the collectors in group No. 11,12 is much greater (wider base width) than for group No. 1,2. This is reflected in the smaller saturation current I_S values for group No. 11, 12, than for group No. 1,2. The difference between the net base dopings accounts for the difference in β_{eff}.

(4) β_N is 20% to 40% higher than β_{eff} for the devices considered in this paper (see Figure 9).

(5) Devices with larger fanout have lower β_{eff} at low current values. This is because of the decreasing ratio of collector to total emitter area. β_{eff} does not simply go inversely as fanout, however, due to the equalizing effect of the necessary gate area for the base contact and metalization clearance.

3. AC Characterization.

The AC or transient electrical parameters are the emitter-base and collector-base depletion layer capacitances and the forward transit time. The reverse transit time is typically much smaller than the forward transit time and may therefore be neglected.

The depletion layer capacitances are measured with a capacitance meter such as the Hewlett-Packard 4271A Digital LCR meter. It is important that the measurement system have adequate guarding and shielding. Accurate de-

termination of depletion layer capacitances is necessary because they control propagation delay in the I^2L extrinsic region of operation. The forward transit time τ_F is determined from the common-emitter short-circuit unity current gain frequency f_T, where

$$\tau_F = \frac{1}{2\pi f_T}$$

f_T is obtained graphically from a plot of the AC common-emitter current gain h_{fe} versus frequency, and is the frequency at which h_{fe} is unity. Gain h_{fe} is measured at an operating collector current corresponding to the maximum current gain ratio (typically 0.4 mA for the gates studied in this research and a collector-emitter voltage of 0.6 volt (single collector and injector terminal open).

4. Washed Emitters (WE).

Bipolar transistor geometries are normally limited in size by the minimum-size emitter contact hole cut. With nominal $10\mu \times 10\mu$ minimum feature size and 5μ recess inside the emitter oxide cut, the emitter has four times the area of the contact. Some microwave devices are fabricated using the emitter at minimum feature size, relying on emitter side-diffusion to allow metalization contact through the same oxide cut without base-emitter shorting (figure 1). This is implemented by "Washing out" the thin emitter-cycle oxide with HF; the etch is not allowed to continue long enough to etch through the thicker (and for P emitters, slower etching) base oxide. This is usually a yield-reducing step because it is done on shallow processes giving little side-diffusion.

In the case of I^2L, the base-collector capacitance will scale down 4:1 nominally (neglecting sidewall contritution), and the emitter-base capacitance and intrinsic-operation charge storage will scale down nominally 2:1 by use of WE. There should be an improvement in both extrinsic and intrinsic speed by about a factor of two by using this technique.

The devices from about two-thirds of the wafers were operational, the remaining ones having leaky or shorted surface n^+p junction. This may be caused by some lack of control in the 6:1 HF "wash" step. It was noticed that 103 ± 2 sec etch time (noted by etching six or eight test wafers) was required to clear the SiO_2. Perhaps 10:1 or 50:1 HF would yield more control. (A seventh mask, "WE protect" was used to protect non-WE contact areas during washing.)

III. RO Data

Unity fanout Ro's from all four process groups were tested to obtain the power-delay (PD) characteristics show in Figure 2. Previously recorded data on the No. 1 group gave a extrinsic region PD value of about .4 PJ, with an unusually flat extrinsic-intrinsic region transition. This is now known to be caused by using a buffer injector current level many times greater than the RO current per gate. Data of Figure 2 is for the buffer injector current equal to the RO injector current per gate, and is regarded as worst-case performance. Interpretation of these curves is the key to understanding processing impact on dynamic I^2L performance (fanout larger than unity are more complicated).

Adapting the relation of Kaassen [2] for extrinsic region performance, $\tau_{delay} = \frac{(C_{EB}+2C_{CB})\,V_{bias}}{2\,I_{gate}\,\alpha_F}$. This directly results by assuming the delay is dominated by charging time of the junction capacitances fed by the effective injector current ($I_{gate} \times \alpha_F$). C_{CB} is doubled because it must charge twice the logic swing. The denominator factor of two results from $\tau_{delay} \triangleq \frac{1}{2n} \quad \frac{1}{f_{RO}}$ where n is the number of stages. α_F describes the effect of current lost in the PNP. Intrinsic region minimum delay is derived by Klaassen, $\tau_{delay} = (\beta_{eff})^{1/2}/2\pi f_T$; delay increases with current gain due to increased charge storage in the saturation region.

SPICE computer simulation agrees well with the experimental data in all cases for the extrinsic region. Calculated values do not agree well with the data; this may be due to interaction of β_{eff}, α_R and $\frac{I_S(NPN)}{I_S(PNP)}$ which is beyond the

scope of this simple calculation. Calculations and data agree well for intrinsic region operation. SPICE simulation is not fully developed for this mode and was not fully investigated; No. 1 simulation was reasonably accurate, however.

Several conclusions may be drawn from this research. For intrinsic operation, the switching time dependence on $\sqrt{\beta_{eff}}/f_T$ is confirmed No. 1 and No. 11 have only 10% differing f_T, yet τ_{min} differs almost 2:1 both by calculation and experiment. This is partially explained by the β difference $(\sqrt{6}/2.5)=1.6$. Increasing delay with increasing current gain has been described by Klaassen [2] and Berger and Wiedmann [3], for the case in which β is increased more quickly than the transit time τ_t is decreased. This is so for No. 1 and No. 11. f_T varies inverselywith epitaxial resistivity for the four groups, as expected. The group No. 11 has a larger effective epitaxial doping (5×10^{16} /cm^3) than the grown epitaxial material (2.6 Ωcm) due to heavy autodoping of the thin (2.4 μ) layer. No. 11 has lower minimum delay than No. 12 due to this high effective emitter concentration, and retains the advantages of lower epitaxial doping (α_F higher) for extrinsic operation (3.5 PJ vs. 5PJ) No. 1 and No. 2 are a good example of the effective of varying only epitaxial resistivity. The more lightly doped No. 1 wafer has higher α_F, therefore lower extrinsic PD, but has lower f_T, hence slower intrinsic operation. This extrinsic-intrinsic tradeoff usually holds; exceptions are No. 11 and No. 12 as described above. No. 11 is characteristic of some thin epitaxy-low voltage industrial digital processes.

Our extrinsic region PD and intrinsic region τ_{min} are poorer than most reported I^2L because: (1) 10 μ features and 5 μ overlap masking rules were used. Industry typically uses 7 ½ μ /5 μ or 5 μ /2½ μ . This directly affects junction capacitances and charge storage. (2) Deeper n^+ isolation, V-groove, isoplanar or other isolation techniques were not employed. This increases charge storage by side-of-gate injection.

IV. Flip Flop Characterization

Investigation of flip flop circuits on a test mask is desirable because RO performance alone is not adequate to fully describe I^2L circuit performance. RO's almost always have sequentially placed gates, which may affect performance due to lateral injection [1]. In addition, RO's do not yield information concerning gate drive capability between gates of different fan-out. A second reason for looking at flip flops is that these building blocks are ubiquitous in system design; once a basic topology is developed it will be repeated as a cell without further concern.

Schematics for the six-gate (after SN 7474) is shown in Figure 10. The six-gate (6G) version has been drawn in different circuit configurations, and turns-out to be the same design. 6G for all process gorups worked well at about 100 $\mu\cdot$W total power from DC to over a megahertz. By including resistor R of the order of 100K Ω to 5MΩ, 6 G worked down to about 1 μW at kilohertz frequencies.

R
EXTERNAL CLOCK
V+
OUTPUT

SIX GATE D FLIP FLOP

Fig.10

This (R) is explained by realization that gate # 1 (FO=1) must sink gate # 2 (FO=3). Because the gates were laid out with all collectors adjacent to the injector bar, the injector-gate periphery, hence current, scales with FO. Gate # 1 has about 45 μ injector periphery and gate # 2 has 90 μ, therefore the current gain requirement of gate # 1 is $\beta_u = 2$. Figure 9 shows that at low current the current gain drops below two, explaining the circuit failure. Resistor R eliminated this problem because it bled off enough gate # 2 current to allow it to be turned off by gate # 1 at low current levels. This problem is not nearly as apparent on No. 1 and 2 as No. 11 and 12, because their β 's are higher even at low currents (they too fall-off at currents lower than given in Figure 9).

Maximum frequency of the flip flops (1-2 MH_z) is limited by the unbuffered external driving circuit capacitance. This will be corrected before subsequent processing runs. Figure 2 shows τ_{min} (FO=1) for No. 11 is about 20ns; at six propagation delays per clock cycle, maximum toggle frequency should approach 6-8 MH_z (Figure 11).

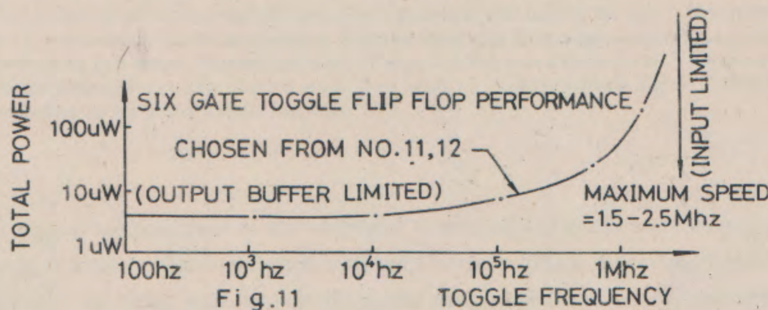

Fig.11

V. Conclusion

The purpose of this project is two-fold. Presentation of SBP I^2L processing and mask design considerations is the immediate result. This information will be of value both in conjection with data from another SBP I^2L run and eventually in judging performance of special process optimized I^2L. Other data is obtainable from the No. 11 and 12 wafers; an FO=2 RO is available for PD comparison with FO=1 RO. Also, separately selectable ground contacts are available near the RO's , 6G. An experiment to study effects of increased ground resistance (common emitter degeneration) using different ground resistances will be performed.

SBP I^2L has been shown to yield about 1.5 to 5PJ extrinsic efficiency and 80 ns to 20 ns intrinsic minimum propagation time. This performance is obtained using 10 μ minimum feature size and 5 μ overlaps (10 μ lateral PNP W_B). There are two recommendations for improvement via mask design: (1) use 7½ μ or 5 μ lateral PNP W_B to improve extrinsic performance by increasing α_F (throw away less current). (2) Use washed emitters to decrease gate size and collector-base junction size. This should give significant improvement in both extrinsic and intrinsic performance.

It is now appreciated that β_d should be high for good SBP I^2L performance. This gives suitable β_{eff} to insure drive capability between gates of different fan-out. Increasing β_{eff} also was seen to generally reduce τ_t faster than the degrading effect going as β_{eff} ½. Normal high- β processing is recommended for SBP I^2L.

Processing improvement alternatives to optimize I^2L performance while retaining SBP compatibility are:

(1) Insert a deep n^+ collar instead of the emitter n^+ (shallow) collar. Estimates of shallow collar efficiency in preventing side-of-gate injection are about 20-30% [4]. The deep collar should improve τ_{min} by about a factor of 2. An extra mask would be required for a $POCL_3$ deposition before the end of the isolation drive-in.

(2) Re-think the inverse-operation structure of NPN integrated devices. Simultaneous out-diffusion of pre-epitaxy deposited As and B into the epitaxial layer to give low emitter charge storage (no intervening

epitaxy) and a field-aid base is recommended. Low epitaxial layer concentration for normal SBP processing and high efficiency I^2L lateral NPN's would be retained. This change would be implemented with deep n^+ collar, V-groove, or other isolation techniques to prevent side injection.

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