—— Recent Publications by Faculties of NCTU

Sunil R. Das, Zen Chen and A. Bhattacharyya (Delhi College of Engineering, India)

Fault detection in sequential machines with increased fault coverage

Electronics Letters, 14, 28-29 (1978)

This letter develops an approach for fault detection and checking sequence design of sequential machines based on the principle of machine modification through augmentation of extra input and extra outputs, taking into consideration the case where faults occurring in a machine may cause an increase in its number of states.

Sunil R. Das and Ching-Lai Sheng

Strong connectivity in symmetric graphs and generation of maximal minimally strongly connected subgraphs

Information Sciences: An International Journal, 14, (1978)

In nonsymmetric graphs strong connectivity is an important concept. In this paper, extending the concept of strong connectivity of nonsymmetric graphs to the case of symmetric graphs, the idea of minimally strongly connected (MSC) and maximal minimally strongly connected (MMSC) subgraphs in a symmetric graph is introduced, and theoretical results are developed that pertain to certain useful properties of these subgraphs. A computer-oriented algorithm is also proposed for finding the MMSC subgraphs from a given symmetric graph, that seems efficient and simple, and tends to reduce computation in generating the subgraphs.

Sunil R. Das and A. Bhattacharyya (Delhi College of Engineering, India)

On the design of failure detection experiments in sequential machines based on terminal measurements

Submitted to IEEE Transactions on Instrumentation and Measurement

On modifying a given sequential machine through augmentation of extra inputs and extra outputs, efficient techniques are developed in the present paper for its fault diagnosis and for the design of checking sequences, taking into consideration the case where faults may cause an increase in the number of states of the machine. Improved bounds on the lengths of checking sequences are also established.

Sunil R. Das, Zen Chen and Ching-Lai Sheng

An approach to microprogram optimization through bit dimension reduction in a given control store specification

Accepted for presentation at the 5th National Systems Conference, Punjab Agricultural University, Ludhiana, India, September 4-6, (1978)

The application of microprogramming in present day computers is very rapidly increasing, and evidence indicates that microprogramming will play a major role in the next generation of computer systems. Microprogram optimization is one way to increase efficiency, and optimization can be crucial in some applications. Optimization refers to a reduction or minimization of execution time of microprograms, or of the control store size, BXW, where W represents the word dimension of the control store which is the number of words of control store required or used for a certain application, and B represents the bit dimension which is the number of bits per word of control store. The various optimization strategies can be broadly classified under four categories: bit dimension reduction, word dimension reduction, state reduction, and heuristic reduction. An analysis and comparison of the above techniques reveal that though microprogram optimization is an extremely important aspect, it is unfortunate that the efforts, probably with only a few exceptions, represent strategies which are either infeasible or undesirable in a practical environment. Much of the efforts on optimization has been devoted to obtaining the absolute minimal solutions rather than "good engineering solutions". Whether the reduction is being performed with respect to the bit dimension, the word dimension, or the number of states, the optimum solution is obtained by techniques that use exhaustive enumeration. These techniques require a great deal of effort, and there is no guarantee that any significant reduction can ultimately be realized. It is thus doubtful that an optimum solution can be justified even if the microcode produced is frequently executed. The use of heuristics can decrease this overhead to some extent. The heuristic reduction techniques appear to be more useful in the sense that, though they do not guarantee optimality of solutions, they can provide some reduction with little efforts. Thus, for the majority of the techniques, much further work remains to be done before any practical applications can be foreseen.

Given a particular ROM specification, and word dimension W, control memory can be reduced by reducing the bit dimension B, at the expense of flexibility. This problem of bit dimension reduction of control memory was first considered by Schwartz who proposed the following model of a ROM. The ROM is an array of storage elements consisting of W words or microinstructions of B bits each, where each word specifies one or more elementary operations or microoperations of the control part which can be executed in parallel. Since the sequencing of ROM words is of no concern, it was assumed that all B bits are used for specifying microoperations. Schwartz, although admitting that the problem is

that of minimizing B, has been unable to provide a scheme achieving this result, and has instead given an exhaustive search a algorithm for finding a partition of the subcommand set into the minimal number of groups. The problem was later reformulated by Grasselli and Montanari in the framework of switching theory, reducing the main minimization problem to a set covering problem of the prime implicant type. Starting with the same basic formulation as of Grasslli and Montanari, Das et al. subsequently developed an approach that solves a number of small cover tables rather than a single big one, and arrives at a solution with less computation in general. The present paper investigates the problem of bit dimension reduction in a control memory specification based on the switching theory formulation of Das et al., and develops a simplified methodology for a "good engineering reduction", or, if necessary, to arrive at a minimal solution.

Sunil R. Das, Ching-Lai Sheng and Zen Chen

An algorithm for finding all maximal complete subgraphs and an estimate of the order of computational complexity

Submitted for publication to Computers and Electrical Engineering

This paper develops an algorithm for finding all maximal complete subgraphs or cliques of an undirected graph. The algorithm is simple, and is based on a refinement of the technique of successive splitting described by Paull and Unger in the determination of maximal compatibles of states in the context of minimization of incomplete sequential machines. The proposed algorithm tends to reduce computation in generating the subgraphs for problems most generally encountered, particularly in relation to the applicability in sequential switching theory.

Sunil R. Das, Ching-Lai Sheng, Zen Chen and J. H. Tzeng

Transition matrices in the measurement and control of synchronous sequential machines

submitted to Information Sciences: An International Journal

This paper develops a matrix approach to the solution of the measurement and control problems in synchronous sequential machines. The control problem in sequential machines is concerned about finding input sequences that take a given machine from a known initial state to a predesignated terminal state. There may be many different measurement problems of interest in sequential machines. An important measurement problem is the identification of the unknown initial state of the machine, called the initial state identification problem or diagnosing problem; whereas, another important measurement problem is relating to the identification of the terminal state of the machine, known as the terminal state identification problem or homing problem, of which the special case is the synchronizing problem. These measurement problems may be solved by applying predetermined input sequences to the machine and noting the resulting output sequences. The conventional approach to the solution of these measurement and control problems is to make use of the information contained in the transition table of the machine in conjunction with its response tree, which is basically an exhaustive tree search process. In the present paper, instead of using the transition table and the corresponding response tree, we use only the transition matrix representation of the machine and its higher-order forms to solve the aforementioned problems. The suggested approach is very systematic and completely algorithmic, and thus lends itself to easy computer implementation.

Tan F. Lei, Chung L. Lee and Chun Y. Chang

Specific contract resistance of the Ni/Au-Ge/nGaP system

Solid-State Electronics, 21, 385-391, (1978)

This work studies the specific contact resistance for Ni/Au-Ge/nGaP system at the rectifying regime, i.e. for which the heat-treatment temperature is below 400°C and the I-V characteristics exhibit a rectifying behavior. The specific contact resistance is first computed by using the generalized majority carrier transport theory derived by Chang and Sze. The computed theoretical results are then used to interpret the experimental data which are obtained by measuring the specific contact resistance, at zero bias, as a function of the temperature for as-deposited and heat-treated Ni/Au-Ge/nGaP Schottky diodes. Au/nGaP Schottky diodes are also fabricated to verify the theoretical results. It is found that the barrier height for the Ni/Au-Ge/nGaP system rises from the as-deposited value, 1.10 ± 0.04eV, to the value of the Ni/nGaP system, 1.27 ∓ 0.02eV, as the contact is heat-treated at various temperatures up to 360°C, the eutectic point of the Au-Ge system, and drops rapidly as the contact is heat-treated above 360°C. The barrier height rise is believed to be caused by the Ni in-diffusion toward the Au-Ge/nGaP interface during the heat-treatment. The smaller temperature dependence of the specific contact resistance for Schottky diode samples heat-treated above 360°C indicates that after heat-treatment above this temperature, an n^+ layer is formed on the GaP surface. The theoretically computed results are used to fit the experimentally measured data to obtain the effective n^+ doping concentrations and barrier heights.

Ching-Cheng Teng

Design of proportional-plus-integral-plus-derivative output feedback for pole assignment

Dec. 1977 Symposium on Automatic Control/ Tsing Hua University

This paper studies the problem of pole assignment in linear time-invariant multivariable systems using proportional-plus-integral-plus-derivative output feedback. It is shown that all system poles can be assigned arbitrarily by use of the unity-rank PID feedback matrices. An example is provided to illustrate the design procedures.