A 0.18-μm CMOS CMFB DOWNCONVERSION MICROMIXER WITH DEEP *N*-WELL TECHNOLOGY FOR LO-RF AND LO-IF ISOLATION IMPROVEMENTS

C. C. Meng,[1] S. K. Hsu,[2] T. H. Wu,[1] and G. W. Huang[3]
[1] Department of Communication Engineering
National Chiao Tung University
Hsin-Chu, Taiwan, R.O.C.
[2] Department of Electrical Engineering
National Chung-Hsing University
Taichung, Taiwan, R.O.C.
[3] National Nano Device Laboratories
Hsin-Chu, Taiwan, R.O.C.

Received 28 September 2004

ABSTRACT: *CMOS deep* N-*well technology can eliminate the physical effects of NMOS transistors and reduce substrate noise and coupling in order to reach the NMOS channel. These properties result in better LO-IF and LO-RF isolations in a Gilbert micromixer. Two identical 0.18-μm CMOS downconversion micromixers (except at the RF input stage) with deep* N-*well or without deep* N-*well are fabricated in adjacent areas of the same wafer for the purpose of isolation comparison. A −37-dB LO-IF and −38-dB LO-RF isolation downconversion micromixer with 19-dB conversion gain and* $IP_{1dB} = -20$ *dBm and* $IIP_3 = -13$ *dBm when RF = 2.4 GHz and LO = 2.25 GHz is demonstrated here using 0.18-μm-deep* N-*well CMOS technology. On the other hand, a downconversion micromixer without deep* N-*well has almost identical power performance but achieves only −20-dB LO-IF isolation and −21-dB LO-RF isolation.* Microwave Opt Technol Lett 45: 168–170, 2005; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.20759

Key words: *CMOS; CMFB; mixer; deep* N-*well*

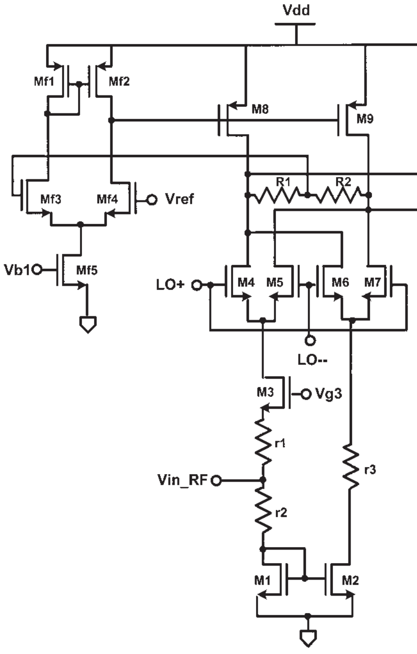

Figure 1 Schematic diagram of the CMOS CMFB downconversion micromixer

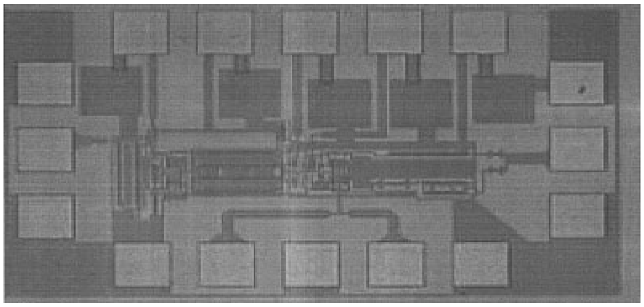

Figure 2 Photograph of the CMOS CMFB downconversion micromixer

INTRODUCTION

The micromixer proposed by Gilbert [1] has become popular for high-frequency RF mixer applications. A CMOS common-mode feedback (CMFB) downconversion micromixer is illustrated in Figure 1. A micromixer has a single-to-differential input stage constructed with M_1, M_2, M_3, and two resistors, as shown in Figure 1 [2, 3]. The common-gate-biased transistor M_3 and common-source-biased transistor M_2 should provide equal but out-of-phase transconductance gain when M_1 and M_2 are connected as a current mirror. However, the common-gate-biased transistor M_3 suffers from a physical effect in a standard *N*-well CMOS process and thus the unequal transconductance causes LO-IF isolation degradation. A deep *N*-well CMOS technology provides good contacts for NMOS transistors [4] and thus source of a NMOS transistor can be connected to the *P*-well contact to avoid physical effects and improve LO-IF isolation. A deep *N*-well can also reduce substrate noise and coupling in order to reach the NMOS channel for better LO-RF isolation. Two identical circuits are illustrated in Figure 1, except that $M_1 \sim M_3$ in deep *N*-wells or $M_1 \sim M_3$ without deep *N*-wells are fabricated in adjacent areas of the same wafer for the purpose of comparison. The rest of the NMOS transistors are all in deep *N*-wells.

CIRCUIT DESIGN

The single-to-differential stage of a Gilbert micromixer renders a high-speed response and also facilitates wideband impedance matching. The common-gate-configured transistor M_3 possesses good frequency response, while the speed of common-source-configured transistor M_2 is improved drastically by adding a low-impedance diode-connected transistor M_1 at the input of common-source-configured transistor M_2. We can set the resistance at the RF input port to be 50Ω by properly designing M_1, M_2, and M_3.

A deep submicron CMOS circuit has low operating voltage; thus, differential active PMOS loads instead of resistive loads are used here to increase the conversion gain without sacrificing the voltage-swing headroom. A resistively sensing CMFB, as illustrated in Figure 1, is needed to bias both the NMOS and PMOS current sources in saturation regions. In other words, M_{f1}–M_{f5} form a comparison amplifier and V_{ref} is set to force the drain voltages of M_8 and M_9 to be V_{ref} by adjusting the PMOS active current loads, M_8 and M_9, in order to guarantee both NMOS and PMOS current sources in the saturation regions. The common-mode sensing resistors, R_1 and R_2, lower the differential-mode gain because the joint point of R_1 and R_2 is virtually grounded but does not affect the voltage swing headroom. Thus, high IF gain can be achieved by choosing high values of resistors at the cost of reducing the IF bandwidth. A differential amplifier formed by $M_{d1} \sim M_{d3}$ serves as a differential-to-single active balun at the output and a common drain stage, M_{d4}, converts the output to the

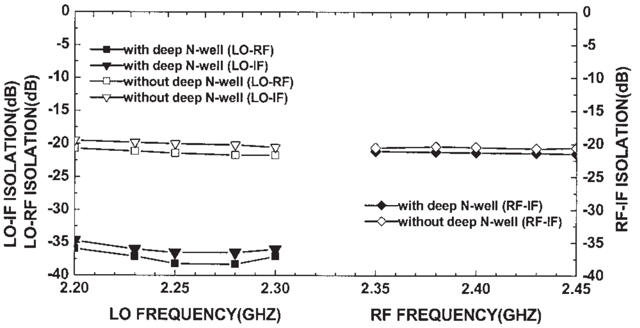

Figure 3 Measured LO-IF, LO-RF, and RF-IF isolation of the CMOS CMFB downconversion micromixer

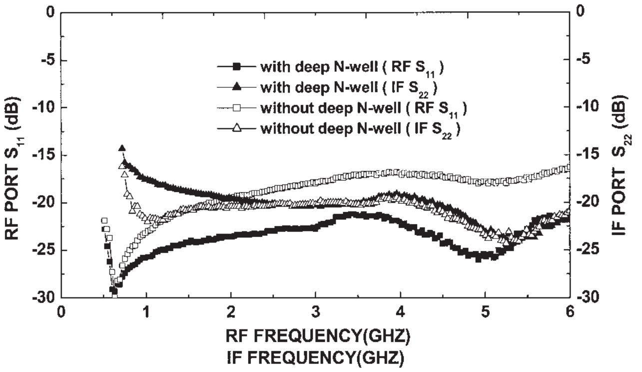

Figure 5 Measured input-return loss in RF port and output-return loss in IF port of the CMOS CMFB downconversion micromixer

low impedance level, as required by the VSWR consideration. Circuit topology with a broadband single-to-differential RF input stage and a broadband differential-to-single output IF stage can facilitate on-wafer measurements and distinguish the isolation improvement effect from the deep *N*-well CMOS technology.

EXPERIMENTAL RESULTS

Figure 2 shows a photograph of the 0.18-μm CMOS CMFB micromixer with a GSG RF input, a GSG IF output, and a GSGSG LO input for on-wafer RF measurements. An off-chip rat-race coupler can generate balanced LO signals to feed the GSGSG LO port. The rat-race coupler is centered at 2.25 GHz and can provide very balanced LO signals for the frequencies from 2.2 to 2.3 GHz. The supply voltage is 2.4 V.

The maximum conversion gain of 19 dB occurs at −5-dBm LO power when LO = 2.25 GHz and RF = 2.4 GHz. LO-IF isolation and LO-RF isolation measurement results when LO = −5 dBm are illustrated in Figure 3. Deep *N*-well has great influence on LO-IF and LO-RF isolation, as expected. −37-dB LO-IF isolation and −38-dB LO-RF isolation are achieved in downconversion micromixer with deep *N*-well, while −20-dB LO-IF isolation and −21-dB LO-RF isolation are achieved in downconversion micromixer without deep *N*-well. The RF-IF isolation-measurement results when LO = 2.25 GHz at −5 dBm are also illustrated in Figure 3 and both circuits have about −21-dB RF-IF isolation because balanced LO signals are provided by the rat-race coupler for both circuits.

The performed power measurements show that both circuits have almost identical results. Figure 4 illustrates the one-tone power measurements and both circuits have 19-dB conversion gain and $IP_{1dB} = -20$ dBm when RF = 2.4 GHz and LO = 2.25 GHz at −5 dBm. The two-tone intermodulation power-measurement results of the mixers are also illustrated in Figure 4 and $IIP_3 = -13$ dBm.

The input-return and output-return losses of both circuits are better than 15 dB for frequencies up to 6 GHz, as illustrated in Figure 5. Figure 6 illustrates the conversion gain as a function of RF frequency when LO = 2.25 GHz at −5 dBm. The conversion gain is 19 dB when IF = 150 MHz and increases up to 24 dB when IF = 50 MHz.

CONCLUSION

A high-isolation CMFB downconversion micromixer with 19-dB conversion gain and $IP_{1dB} = -20$ dBm and $IIP_3 = -13$ dBm when RF = 2.4 GHz and LO = 2.25 GHz has been demonstrated here using 0.18-μm deep *N*-well CMOS technology. Deep *N*-well technology has great influence on LO-IF and LO-RF isolation, but not on RF-IF isolation. CMOS deep *N*-well technology can eliminate the physical effects of NMOS transistors to improve LO-IF isolation. The reduction of substrate noise and coupling to reach NMOS channel improves LO-RF isolation. RF-IF isolations are the same for micromixers both with and without deep *N*-wells, as long as balanced LO signals are provided. A −37-dB LO-IF and −38-dB LO-RF isolation downconversion micromixer with 19-dB conversion gain has been demonstrated in this paper by using 0.18-μm deep *N*-well CMOS technology. On the other hand, a downconversion micromixer without deep *N*-well has an almost identical power performance but achieves only −20-dB LO-IF

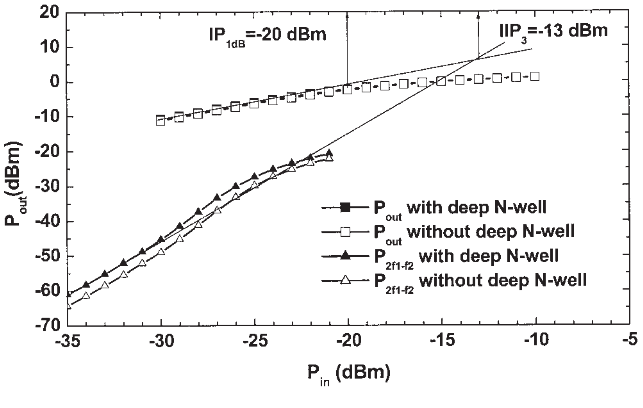

Figure 4 One-tone and two-tone power measurements of the CMOS CMFB downconversion mixer

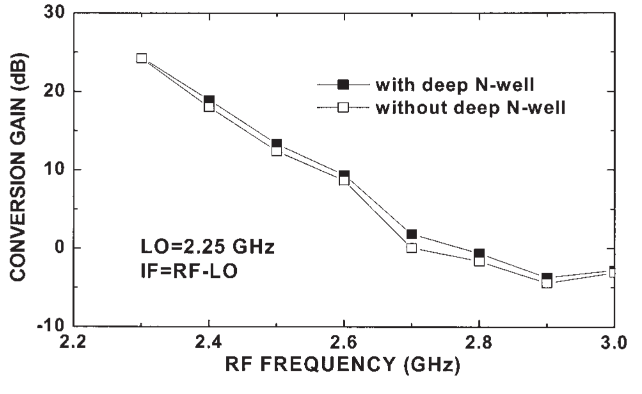

Figure 6 Measured gain response of the CMOS CMFB downconversion micromixer when LO = 2.25 GHz and −5 dBm

isolation and −21-dB LO-RF isolation, even if two kinds of mixers are fabricated in adjacent areas of the same wafer.

ACKNOWLEDGMENTS

The authors would like to thank the National Chip Implementation Center (CIC) for technical support. This work was supported by the National Science Council of Republic of China under contract nos. NSC 93-2752-E-009-003-PAE and NSC 93-2219-E-009-026, and by the Ministry of Economic Affairs under contract no. 92-EC-17-A-05-S1-020.

REFERENCES

1. B. Gilbert, The MICROMIXER: A highly linear variant of the Gilbert mixer using a bisymmetric Class-AB input stage, IEEE J Solid-State Circ 32 (1997), 1412–1423.
2. J. Durec and E. Main, A linear class AB single-ended to differential transconverter suitable for RF circuits, IEEE MTT-S Dig, San Francisco, CA, (1996), 1071–1074.
3. J. Durec, An integrated silicon bipolar receiver subsystem for 900-MHz ISM band applications, IEEE J Solid-State Circ 33 (1998), 1352–1372.
4. J.G. Su, H.M. Hsu, S.C. Wong, C.Y. Chang, T.Y. Huang, and J.Y.C. Sun, Improving the RF performance of 0.18-μm CMOS with deep n-well implantation, IEEE EDL 22 (2001), 481–483.

RF EQUIVALENT-CIRCUIT MODEL OF INTERCONNECT BENDS BASED ON *S*-PARAMETER MEASUREMENTS

Xiaomeng Shi,[1] Jianguo Ma,[1] Beng Hwee Ong,[1]
Kiat Seng Yeo,[1] Manh Anh Do,[1] and Erping Li[2]
[1] Center for Integrated Circuits & Systems
Nanyang Technological University
Nanyang Avenue, Singapore 639798
[2] Institute of High Performance Computing (IHPC)
1 Science Park Road #01-01, The Capricorn
Singapore Science Park II, Singapore 117528

Received 22 September 2004

ABSTRACT: *A modified model for RF interconnect bends on lossy substrate in CMOS technology is presented. The model parameters are extracted directly from the on-wafer S-parameter measurements. The accuracy is verified up to 20 GHz by the measurements of the test structures.* © 2005 Wiley Periodicals, Inc. Microwave Opt Technol Lett 45: 170–173, 2005; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.20760

Key words: *equivalent circuits; interconnect models; scattering parameters measurement*

1. INTRODUCTION

Nowadays, there is a tremendous interest in using conventional CMOS technology for RF and microwave applications [1]. However, the low-resistivity substrate used in the RF CMOS process causes significant high-frequency losses. Additionally, the operating frequencies already reach multi-giga Hertz. As a result, RF interconnects play an increasingly important role in RFICs [2]. To date, one of the limiting factors of RFIC designs is the absence of accurate interconnect models [3]. In the literature, most studies have focused on simple structures such as straight lines, double-paralleled lines, and so forth [4–7]. Interconnects with bends, very often used in real designs, are seldom reported.

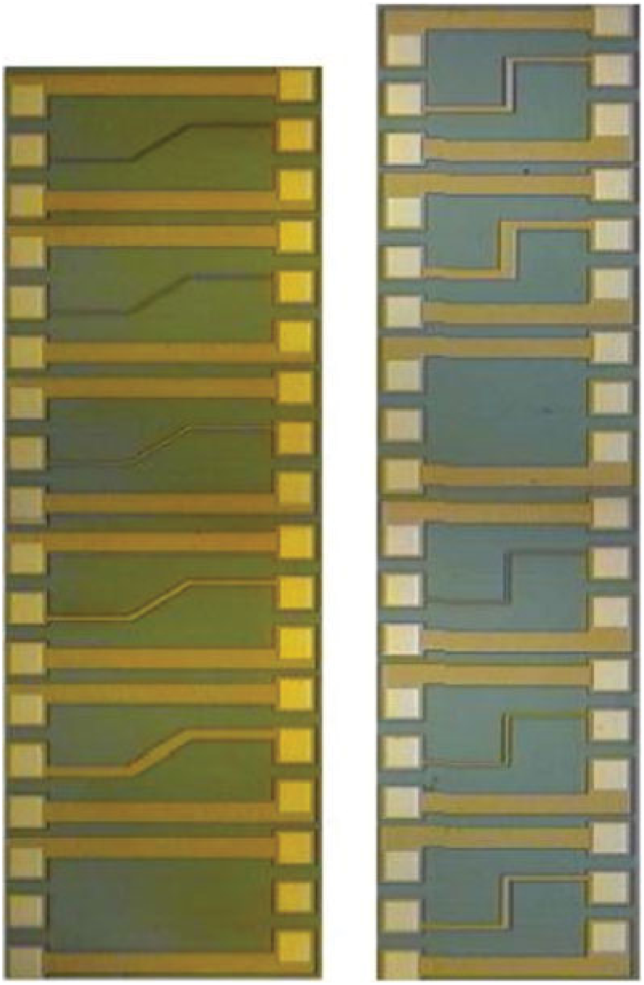

Figure 1 Test structures of the fabricated interconnect bends. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com.]

In this paper, interconnects with both 90° and 45° bends are studied. As illustrated in Figure 1, test structures with different dimensions were designed and fabricated on the top metal layer, employing the 0.18-μm RF CMOS process by Chartered Semiconductor Manufacture Ltd. (CSM). The *S*-parameters of these structures were measured up to 20 GHz and used for the characterization [8].

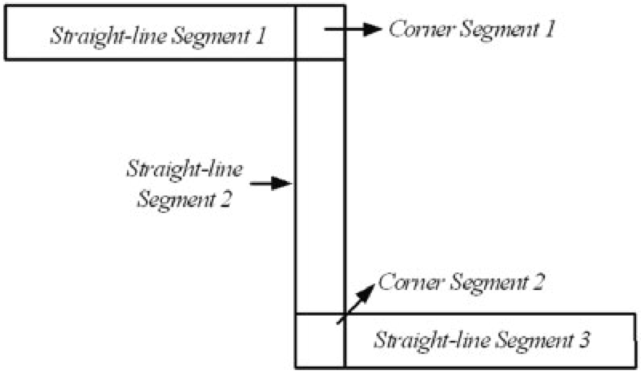

Figure 2 Structure of interconnect bends