High-Performance Poly-Si TFTs Fabricated by Implant-to-Silicide Technique

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***Abstract*—High-performance poly-Si thin-film transistors (TFTs) with fully silicided source/drain (FSD) and ultrashort shallow extension (SDE) fabricated by implant-to-silicide (ITS) technique are proposed for the first time. Using the FSD structure, the S/D parasitic resistance can be suppressed effectively. Using the ITS technique, an ultrashort and defect-free SDE can also be formed quickly at about 600 °C. Therefore, the FSD poly-Si TFTs exhibits better current-voltage characteristics than those of conventional TFTs. It should be noted that the on/off current ratios of FSD poly-Si TFT ($W/L = 1/4\mu$m) is over 3.3×10^7, and the field-effective mobility of that device is about 141.6 (cm^2/Vs). Moreover, the superior short-channel characteristics of FSD poly-Si TFTs are also observed. It is therefore believed that the proposed FSD poly-Si TFT is a very promising TFT device.**

***Index Terms*—Implant-to-silicide (ITS), silicide source/drain (S/D), thin-film transistor (TFT).**

I. Introduction

POLYCRYSTALLINE silicon thin-film transistors (poly-Si TFTs) were attractive for many potential applications including the active matrix liquid crystal display (AMLCD) [1], [2]. In order to integrate peripheral driving circuits on the same glass substrate, the device with high on/off current ratio (I_{on}/I_{off}) by a simple and low-temperature process should be developed. Conventionally, long-term post-ion implantation annealing treatments which was used to activate dopants and remove damage defects was usually carried out using furnace annealing around 600 °C for as long as several tens of hours after the source/drain (S/D) implantation [3]. The prolonged process time of implant annealing caused low throughput in the fabrication of conventional poly-Si TFTs (CN TFTs). Thus, it suffered from a substantial trade-off between performance and throughput.

On the other hand, to reduce parasitic S/D resistance (R_p), various techniques such as raised S/D, SiGe raised S/D, and Tungsten-clad S/D poly-Si TFTs were proposed to suppress the large parasitic resistance [4]–[6]. Silicide poly-Si TFTs were also suggested recently [7]. Nevertheless, in the salicide TFTs, in order to activate the dopant and remove implanted damage defect in poly-Si, the long-term post-ion implantation annealing treatments could not be neglected. Furthermore, the complex process and the quite shallow silicide S/D structure were needed to maintain S/D junction intact [8].

In this letter, to reduce the R_p of CN TFTs while promote the throughput, we introduce a novel fully silicided S/D poly-Si TFTs (FSD TFTs) with ultrashort S/D extension (SDE) structure by simple, low-temperature ITS technique for the first time [9]. Because of the implant-to-silicide (ITS) technique, different to the process of salicide TFTs, the dopants can be implanted into the silicide region without damage the poly-Si region, and then, activated and diffused out quickly from silicide to the interface of silicide/poly-Si at about 600 °C by rapid thermal annealing (RTA). Therefore, the activation thermal budget for FSD TFTs is less than that for the CN and salicide TFTs. Furthermore, the excellent short channel characteristics are also achieved by the ultra shallow SDE structure. Therefore, high performance novel FSD TFTs with simple, quick, and low temperature process are fabricated and demonstrated in this letter first.

II. Device Fabrication

Fig. 1 shows the key fabrication steps for the proposed FSD TFT structure. Briefly, the fabrication begins by depositing an amorphous Si (α-Si) layer (45 nm) at 550 °C using low-pressure chemical vapor deposition (LPCVD) on 6 in. Si wafers capped with a thermal oxide layer (1 μm). The deposited α-Si layer was then recrystallized by solid phase crystallization (SPC) process at 600 °C for 24 h in N_2 ambient. After patterning the active region, a 45–nm CVD gate oxide and a α-Si layer (100 nm) were deposited. The α-Si layer was then patterned to form the gate electrode layer as shown in Fig. 1(a). Next, a 100-nm CVD oxide layer was deposited and anisotropically etched to form a sidewall spacer abutting the poly-Si gate, as shown in Fig. 1(b). Afterwards, a self-aligned silicidation treatment was performed to form the fully silicided S/D. Thus was accomplished by depositing a thin Ni layer (22 nm), followed by a RTA (500 °C, 40 s) step. At the same time, Ni-silicide was formed on poly-Si gate simultaneously. After the silicidation process, a wet etching step in a H_2SO_4–H_2O_2 (3:1) solution was then used to remove the unreacted Ni layer as shown in Fig. 1(c). Next, an ITS process was employed to form SDE. Phosphorus ions were implanted to silicide at 30 KeV to a dose of 5×10^{15} cm^{-2} for n-channel FSD TFTs. Dopants were then diffused out of silicide to form an ultrashort SDE at the channel-S/D interface by a low-temperature RTA process at temperature of 600 °C for 30 s in N_2 ambient. Because of the low solid-state solubility of phosphorous

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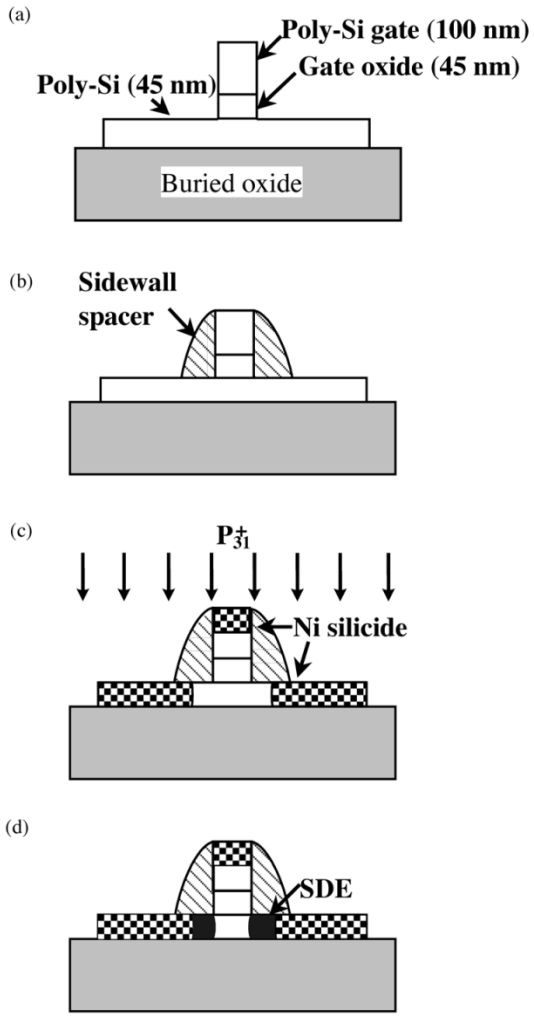
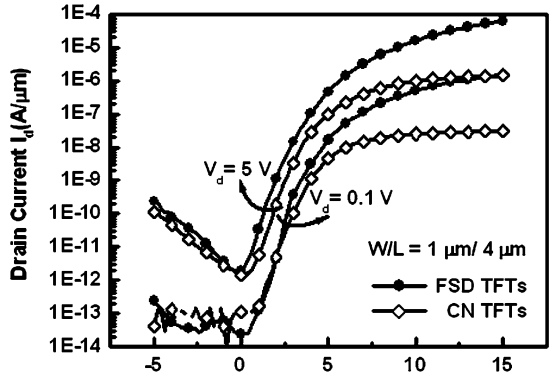


Fig. 1. Main process flow of the FSD TFTs.

atoms in Ni silicide, they diffused out and piled up at the Si/silicide interface to form an ultrashort SDE as shown in Fig. 1(d). Since the ion implantation process does not damage Si layer directly, the junction would be free of crystalline defects and low junction leakage current could be expected [10]. Finally, typical inter layer dielectric deposition, contact hole patterning, and Al metallization completed the fabrication process. A plasma treatment at 350 °C in NH_3 for 30 min was performed before measurements. For comparison, CN TFTs implanted after gate patterning; then, activated at temperatures of 600 °C for 24 h without silicidation and ITS process steps were also fabricated.

III. Results and Discussions

Fig. 2(a) depicts the typical transfer characteristics for FSD and CN TFTs at drain voltages (V_d) of 0.1 and 5 V. The nominal channel length (L) and channel width (W) are 4 and 1 μm, respectively. The measured as well as extracted key devices parameters, including threshold voltage $(V_{\rm th})$, subthreshold swing (S.S.), field-effect mobility $(\mu_{\rm FE})$, leakage current ($I_{\rm off}$ at $V_d = 5$ V), and on/off current ratio ($I_{\rm on}$ $I_{\rm off}$ at $V_d = 5$ V) are summarized in Fig. 2(b). Obvious improvement in devices characteristics is obtained for FSD TFTs instead of CN TFTs; as shown in Fig. 2(b), $V_{\rm th}$ decreased from 4 to 3.4 V, SS decreased from



(b)

Parameters	CN	FSD
Threshold voltages, V_{th} (V)	4	3.4
Subthreshold swing, S.S. (V/dec)	0.6	0.45
Field-effect mobility, μ_{FE}(cm^2/V.s)	3.2	141.5
Leakage current, I_{off} (pA)	1.45	1.84
On/off current ratio, I_{on}/I_{off}	9.9×10^5	3.3×10^7

Fig. 2. Comparisons of (a) transfer characteristics and (b) device characteristics for FSD and CN poly-Si TFTs with $L = 4$ μm and $W = 1$ μm.

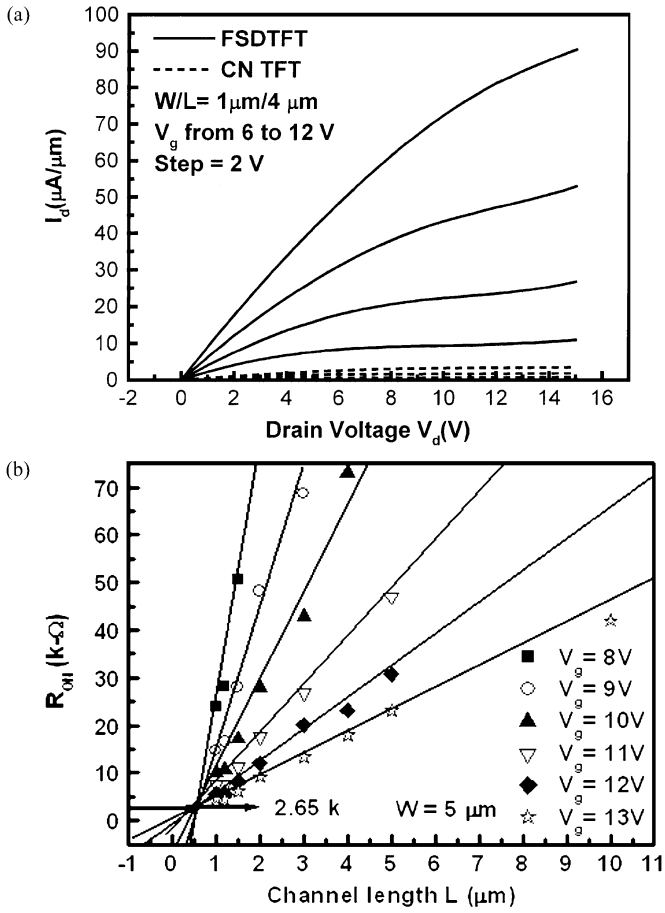


Fig. 3. (a) Output characteristics of FSD and CN TFTs with $L = 4$ μm and $W = 1$ μm. The circle and triangle are for the FSD and CN TFTs, respectively. (b) The width-normalized ON resistance $(R_{\rm ON})$ of FSD TFTs as a function of channel length. The channel width is fixed at 5 μm while the channel length is varied from 10 to 1 μm.

0.6 to 0.45 V/dec, $\mu_{\rm FE}$ increased from 3.2 to 141.5 cm^2/Vs, and $I_{\rm on}/I_{\rm off}$ increased from 9.9×10^5 to 3.3×10^7. Since the

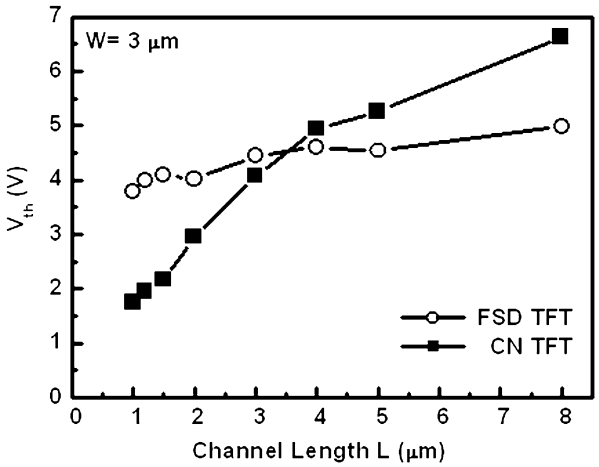


Fig. 4. Threshold voltage ($V_{\rm th}$) of FSD and CN TFTs with channel length (L) varying from 8 to 1 μm, the channel width (W) is kept at 3 μm.

ion implantation process does not damage the poly-Si layer directly, the junction would be free of crystalline defects; therefore, the $I_{\rm off}$ of FSD TFTs is almost identical with that of CN ones. Fig. 3(a) shows the typical output characteristics (I_d-V_d) at several different gate voltages for the FSD and CN TFTs. The $W/L = 1\ \mu$m$/4\ \mu$m FSD TFTs exhibits a larger driving current than CN ones, especially under high gate bias. This is because for large gate bias, the channel resistance becomes smaller; hence the dominant resistance is due to the R_p [11]. The R_p of FSD TFTs, in the linear region, is also extracted by plotting width-normalized on state resistance ($R_{\rm ON}$) versus gate length (L), as shown in Fig. 3(b), [12]. All the width-normalized $R_{\rm ON}$-L curves merge at $L = 0.45\ \mu$m and have a residual value of a gate voltage-independent R_p of 2.65 kΩ. The R_p of CN TFTs is also extracted by the same method and is about 20 kΩ, which is about 13 times larger than that of FSD TFTs.

To examine the short-channel effect of the FSD TFTs, the threshold voltages ($V_{\rm th}$) rolloff of FSD and CN TFTs are compared in Fig. 4. The $V_{\rm th}$ is determined by the constant drain current ($I_{\rm d} = 1$ nA/μm, at $V_d = 0.1$ V) method. Apparently, $V_{\rm th}$ rolloff of FSD TFTs is effectively released than that of CN devices. The plausible reason is that the diffusion length of SDE of FSD TFTs can be effectively suppressed by the low temperature ITS process; therefore, the effective channel length could be controlled appropriately.

IV. Conclusion

We have proposed a novel high-performance poly-Si TFT with ultralow parasitic resistance fully silicide S/D and ultrashort SDE by a simple, low-temperature ITS process. The experimental results show that the proposed devices not only depict improved turn-on characteristics by successfully reducing the R_p but also maintain the low off-state leakage current by SDE region. Superior short channel characteristics are also observed, which may be explained by the ultrashallow SDE of FSD TFTs. Therefore, the proposed FSD TFT is ideally suitable for implementing high-density and high-performance driver circuits on the glass panel for AMLCD applications.

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