Minimized Transient and Steady-State Cross Regulation in 55-nm CMOS Single-Inductor Dual-Output (SIDO) Step-Down DC-DC Converter

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***Abstract*—A single-inductor dual-output (SIDO) step-down DC-DC converter with continuous conduction mode (CCM) operation is proposed to achieve an area-efficient power management module. The low-voltage energy distribution controller (LV-EDC) can simultaneously guarantee good voltage regulation and low output voltage ripple. With the proposed dual-mode energy delivery methodology, cross regulation in steady-state output voltage ripple, which is rarely discussed, and cross regulation in load transient response are both effectively reduced. In addition, the energy mode transition operation helps obtain the appropriate energy operation mode using the energy delivery paths for dual outputs. Moreover, within the allowable output voltage ripple, the automatic energy bypass (AEB) mechanism can reduce the number of energy delivery paths, thereby ensuring voltage regulation and further enhancing efficiency. The test chip, fabricated in 55-nm CMOS, occupies 1.44 mm^2 and achieves 91% peak efficiency, low output voltage ripple, and excellent load transient response for a high-efficiency system-on-a-chip (SoC) integration.**

***Index Terms*—Cross regulation, energy bypass mechanism, energy delivery path, load transient response, output voltage ripple, power conversion efficiency, single-inductor dual-output (SIDO) converter.**

I. Introduction

SINGLE-INDUCTOR dual-output (SIDO) converter [1]–[14] can be used to power the different function blocks to achieve the battery-operated system-on-a-chip (SoC) integration. With the use of a single off-chip inductor, the SIDO converter can allocate energy to dual outputs and provide two independent supply voltages. As a result, the print-circuit-board (PCB) area can be effectively reduced since the conventional power management modules [15]–[18] require two inductors to generate dual outputs. Low output voltage ripple, minimized cross regulation, and high power conversion efficiency are essential design issues for a SIDO converter. Fig. 1 shows the proposed SIDO step-down converter in SoC integration. The embedded power switches in the SIDO converter can deliver energy from $V_{\rm IN}$, typically the battery output, to both off-chip capacitors C_{OA} and C_{OB} through an off-chip inductor. Thus, the converter generates two output voltages, V_{OA} and V_{OB}, to supply the analog and the digital parts, respectively. However, cross regulation can diminish the quality of the two supply voltages.

The typical cross regulation problem in the SIDO converter is illustrated in Fig. 2. Cross regulation may occur both in transient and steady-state periods because of one-inductor utilization. That is, in case of a load current step at I_{OA}, for example, the output voltage of V_{OA} derives a voltage drop. However, unintended voltage variation also occurs at V_{OB}, which maintains a constant load current, I_{OB}. This occurrence is called the transient cross regulation resulted from the energy delivery scheme during the load transient response. This transient cross regulation may cause abnormal operation in the circuits supplied by V_{OB} and must be minimized. Steady-state cross regulation is clearly observed when the two outputs have a large load difference. When one of the two outputs operates at light loads while the other has to provide a large load current, the light-load output would be overcharged if no suitable energy delivery scheme is in place. Moreover, with the discontinuous inductor current received at both outputs, the induced output voltage ripple increases due to the existence of equivalent series resistance (ESR) on output capacitor. The functions of some noise-sensitive circuits can be seriously affected. Therefore, cross regulation must be minimized to achieve the advanced low-voltage high-performance SoC applications.

The comparator-controlled output technique is mostly used in multi-output structure to obtain adequate energy without considering a complex energy delivery scheme [1], [2]. Nevertheless, this approach suffers from large output voltage ripple and the insufficient regulation performance. The discontinuous conduction mode (DCM) operation [3], [4] serves as an effective method for separating the energy correlation between dual outputs. It prevents energy from accumulating in the inductor, but exhibits poor transient performance. In addition, the priority of the energy delivery paths will ensure the voltage regulation on only one specific output [5], [15], which carries out the load restriction of the dual outputs. The control method of pseudo-continuous conduction mode (PCCM) combines the operation of both the continuous conduction mode (CCM) and DCM [6], [7]. However, it results in large power dissipation because of

Manuscript received February 17, 2011; revised May 10, 2011; accepted July 20, 2011. Date of publication September 12, 2011; date of current version October 26, 2011. This paper was approved by Guest Editor Muneo Fukaishi. This work was supported by the National Science Council, Taiwan, under Grant NSC 100-2220-E-009-050 and Grant NSC 100-2220-E-009-055.

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Digital Object Identifier 10.1109/JSSC.2011.2164019

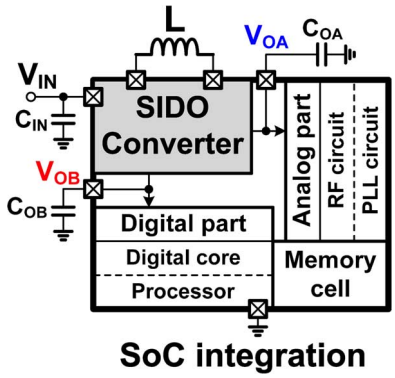

Fig. 1. Brief illustration of the proposed SIDO step-down converter in SoC integration.

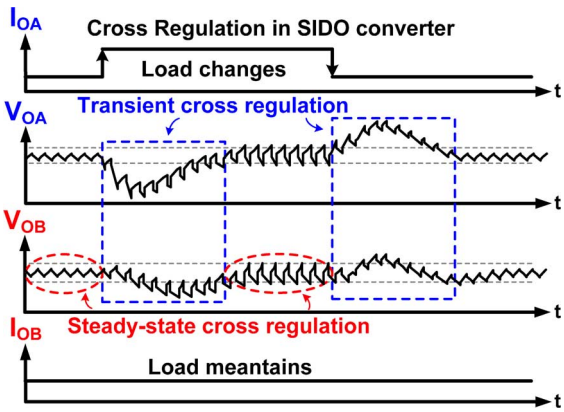

Fig. 2. Cross regulation in both transient and steady-state of the SIDO converter.

existing freewheel stage and high induction current level. Additionally, cross regulation can be minimized with the use of an extra flying capacitor [8], although cost increases. To achieve regulated output voltages and minimize cross regulation, the arrangement of the energy delivery paths is a popular design consideration in SIDO converters [9]–[14]. Unfortunately, this method would restrict the voltage levels or the loading priorities at the outputs. These are determined by the design of the power stage and the order of the energy delivery paths. Therefore, minimized cross regulation in both transient and steady-state must be simultaneously achieved with maintaining good voltage regulation and high power conversion efficiency. The proposed low-voltage energy distribution controller (LV-EDC) with the current-programmed control can ensure the voltage regulations and yield a stable response in both transient and steady-state. The dual-mode energy delivery methodology, with both the energy mode transition operation and the automatic energy bypass (AEB) mechanism, is implemented to minimize cross regulation and further enhance the efficiency of the proposed SIDO converter.

This paper is organized as follows. The proposed SIDO converter structure with the LV-EDC is depicted in Section II. The proposed dual-mode energy delivery methodology is illustrated in Section III. Detailed circuit implementations of the LV-EDC are described in Section IV. Experimental results are shown in Section V. Finally, a conclusion is made in Section VI.

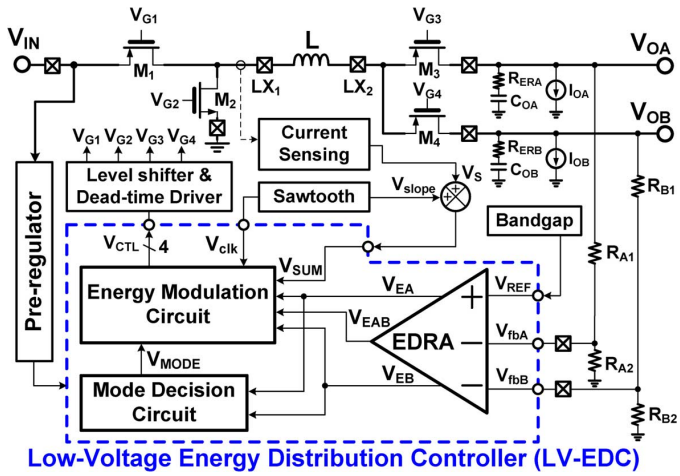

Fig. 3. The proposed step-down SIDO converter with LV-EDC.

II. Proposed SIDO Converter With the LV-EDC

The proposed SIDO converter with the LV-EDC is shown in Fig. 3. Power stage is composed of four power switches, $M_1 - M_4$, an inductor, and capacitors for delivering energy from $V_{\rm IN}$ to dual outputs, V_{OA} and V_{OB}, through the specific energy path combinations. The power switches, which are implemented by the thick oxide devices in 55-nm CMOS technology, can tolerate the voltage range of battery-powered input. The voltage dividers are carried out by R_{A1}, R_{A2}, R_{B1}, and R_{B2} to feed output voltage information to the LV-EDC for monitoring output load conditions. The current sensing circuit can derive inductor current information by detecting the voltage variations of switching node LX_1. To achieve a robust current-programmed control, the slope compensation signal $V_{\rm slope}$ and the current sensing signal V_S create the summing signal $V_{\rm SUM}$ to avoid subharmonic oscillation [16].

The LV-EDC can operate under 1-V low voltage with the use of 55-nm core devices to achieve power saving and small silicon area. The energy distribution regulation amplifier (EDRA), which is used to reflect the output load conditions, generates the error signals V_{EA} and V_{EB} for V_{OA} and V_{OB}, respectively. Voltage V_{EAB} generated by the summation of V_{EA} and V_{EB} [12] represents the overall energy demand of dual outputs and, in addition, can indicate the peak inductor current level. The intersections of $V_{\rm SUM}$ with V_{EA}, V_{EB}, as well as V_{EAB}, can achieve energy modulation with the current-programmed control. Consequently, low output voltage ripple and good transient response can be guaranteed because the dual outputs can both obtain energy in each pulse-width-modulation (PWM) switching cycle. The mode decision circuit in the LV-EDC helps determine energy operation modes through the signal, $V_{\rm MODE}$, in accordance with load conditions. It minimizes both transient and steady-state cross regulations. Additionally, the energy modulation circuit produces a 4-bit control signal, $V_{\rm CTL}$, and achieves PWM operation within one switching period, T_S. Furthermore, the level shifter and dead-time driver can enhance the driving capability of power switches and prevent the shoot-through current between the power switches of $M_1 - M_2$ and $M_3 - M_4$.

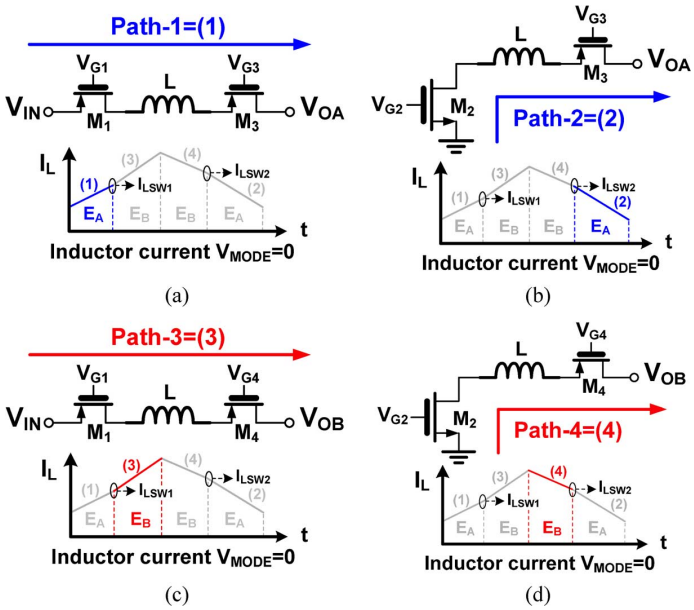

Fig. 4. Four distinct energy delivery paths at power stage in the proposed SIDO converter.

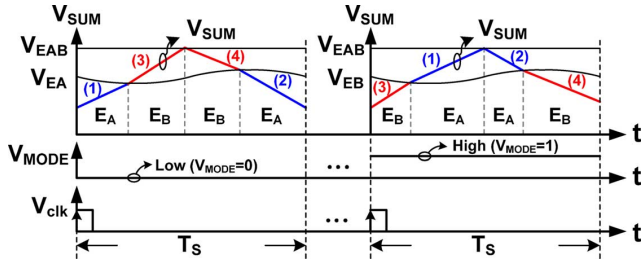

Fig. 5. Illustration of the dual-mode energy delivery methodology.

III. Dual-Mode Energy Delivery Methodology

Fig. 4 shows the four distinct energy delivery paths in the power stage of the proposed SIDO converter. With an input voltage $V_{\rm IN}$ of 3.3 V and nominal output voltages, V_{OA} and V_{OB}, of 1.8 V and 1.2 V, respectively, the dual step-down operation is derived. Path-1 and path-3 are regarded as the inductor charging paths with positive slopes shown in Fig. 4(a) and (c) to deliver energy for V_{OA} and V_{OB}, respectively. Meanwhile, path-2 and path-4 are considered as the inductor discharging paths with negative slopes shown in Fig. 4(b) and (d) to transfer energy for V_{OA} and V_{OB}, respectively. When these four energy delivery paths are combined, energy distribution for dual output can be achieved with CCM operation.

According to the characteristics of CCM operation, the final state of the inductor current level is equal to the initial state in one switching period at steady-state. However, the inductor current waveform shown in Fig. 4 is the specific one combination of the energy delivery paths in steady-state, which is controlled by mode decision signal $V_{\rm MODE}$. The $V_{\rm MODE}$ signal determines two distant methodologies to achieve the operation in the proposed SIDO converter. As a result, to minimize both transient and steady-state cross regulations induced by the output load steps and the large load difference between the dual outputs, respectively, the proposed dual-mode energy delivery methodology can appropriately arrange the energy delivery paths and the inductor current level. Consequently, the transient cross regulation can be improved by rapidly adjusting the inductor current when the load transient response occurs, and the steady-state cross regulation can be simultaneously minimized with the output voltage ripple in the proposed SIDO converter.

Fig. 5 illustrates the proposed dual-mode energy delivery methodology controlled by $V_{\rm MODE}$. If the energy delivered to the output of V_{OA} is smaller than that of V_{OB}, $V_{\rm MODE}$ will be set to low. The energy delivery paths follow the order of path-1, path-3, path-4, and path-2. Thus, energy is delivered to V_{OA} at the beginning of every PWM switching cycle after the trigger by system clock $V_{\rm clk}$. On the other hand, $V_{\rm MODE}$ is set to high when the output of V_{OA} has a larger energy request than that of V_{OB}. Therefore, the energy delivery paths are achieved with the order of path-3, path-1, path-2, path-4 in sequence, and commence when the energy deliver to V_{OB} synchronized with $V_{\rm clk}$. In addition, the switches among the four energy delivery paths are decided by the intersections of summing signal $V_{\rm SUM}$ with V_{EAB}, V_{EA}, and $V_{\rm EB}$. Here, the intersection of V_{EAB} and $V_{\rm SUM}$ determines the peak inductor current. The stored energy in the inductor can be optimized compared to the prior arts [6] because V_{EAB} is the summation of V_{EA} and $V_{\rm EB}$ that represents the exact energy requirement of the dual outputs. Utilizing the superposition theorem in SIDO converter with the current-programmed control is similar to the combination of the two separated single-output buck converters. Additionally, V_{EA} determines the transition points from path-1 to path-3 and path-4 to path-2 when $V_{\rm MODE} = 0$. $\rm E_A$ indicates the provision of the energy for V_{OA}, and is delivered at the period that has a lower inductor current value. $\rm E_B$ indicates the energy provision for V_{OB}, and is located at the period containing the peak inductor current. Moreover, the energy transition points from path-3 to path-1 and path-2 to path-4 are decided by error signal $V_{\rm EB}$ when $V_{\rm MODE} = 1$. $\rm E_B$ is derived at the period with lower inductor current value, whereas $\rm E_A$ is obtained near the peak inductor current. That is, either of the energy operation modes can achieve the energy delivery scheme with the current-programmed control through the determination of $V_{\rm MODE}$.

Fig. 6 shows the LV-EDC control scheme in detail. The EDRA contains the two individual error amplifiers (EA) that can respond output load conditions and generate error signals V_{EA} and $V_{\rm EB}$. In the proposed work, the error amplifier is designed using the low-voltage multistage structure presented in [17] to guarantee high system loop gain for ensuring good output voltage regulation. The energy modulation circuit is composed of three individual comparators and the energy path logic. Fig. 6(a) shows the exact control scheme when the signal $V_{\rm MODE}$ is set to low. With the selection of ordered energy delivery path 1-3-4-2 depicted in Fig. 5, V_{EAB} and V_{EA} are compared with $V_{\rm SUM}$ through the comparators, $\rm comp_1$ and $\rm comp_2$. Subsequently, output signals $V_{\rm CAB}$ and $V_{\rm CA}$ are sent to the energy path logic to determine control signals for turning the power switches on or off. In addition, V_{EAB} and $V_{\rm EB}$ are compared with $V_{\rm SUM}$ through, $\rm comp_1$ and $\rm comp_3$ shown in Fig. 6(b) to generate the ordered energy delivery path 3-1-2-4, which is derived when the $V_{\rm MODE}$ is set to high. To realize the

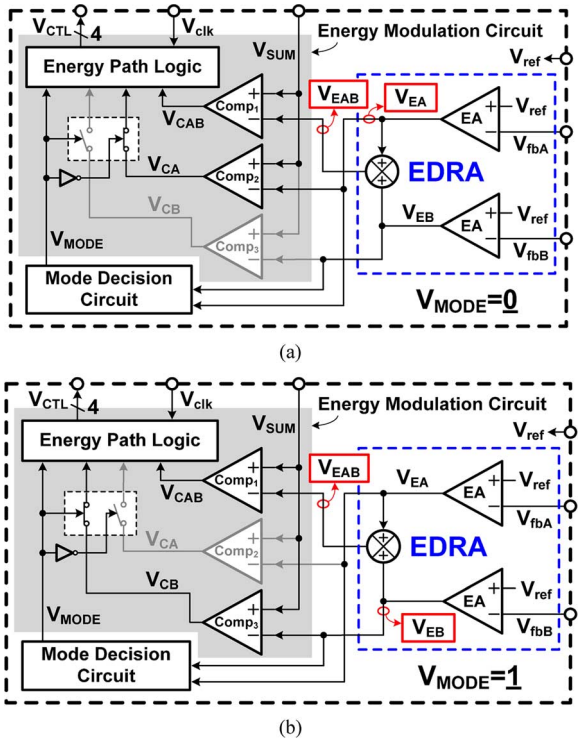

Fig. 6. Control scheme of the LV-EDC circuit. (a) The operation of $V_{\rm MODE} = 0$. (a) The operation of $V_{\rm MODE} = 1$.

energy delivery paths, the energy path logic can determine the 4-bit control signal, $V_{\rm CTL}$, with the synchronization of $V_{\rm clk}$ for achieving the energy delivery methodology.

Moreover, to further enhance both transient and steady-state cross regulations, the energy delivery paths must be optimized in accordance with the output load conditions. That is, the energy operation mode and the energy delivery paths must be adjusted accordingly to obtain suitable energy delivery scheme for dual outputs.

A. Energy Mode Transition Operation

Output voltage ripples Δv_{oA} and Δv_{oB} in the proposed SIDO converter are illustrated, respectively, as

$$\Delta v_{oA} \cong \frac{V_{OA}}{C_{OA}R_{LA}} T_{\rm on\_M4} + R_{ERA} I_{LSW} \tag{1}$$

$$\Delta v_{oB} \cong \frac{V_{OB}}{C_{OB}R_{LB}} T_{\rm on\_M3} + R_{ERB} I_{LSW} \tag{2}$$

where

$$I_{LSW} = \max\{I_{LSW1}, I_{LSW2}\}. \tag{3}$$

R_{LA} and R_{LB} are the equivalent load resistances at V_{OA} and V_{OB}, respectively. $T_{\rm on\_M3}$ and $T_{\rm on\_M4}$ indicate the turned-on periods of the power switches, M_3 and M_4, respectively. R_{ERA} and R_{ERB} are the ESRs on output capacitors C_{OA} and C_{OB} respectively. From the equations shown in (1) and (2), the first term in both (1) and (2) contain the output voltage values, load conditions, and output capacitor values. These factors are all limited by design specifications. As depicted in (3), I_{LSW} is the maximum value between the currents of I_{LSW1} and I_{LSW2} depicted in Fig. 4. I_{LSW} represents the exact inductor current value at the energy path transition point, where $V_{\rm SUM}$ and V_{EA} or $V_{\rm SUM}$ and V_{EB} intersect in different energy operation modes. In addition, the power switches M_3 and M_4 are used to allocate energy for the dual outputs, both of which, however, cannot receive energy simultaneously owing to the SIDO methodology. Thus, the discontinuous inductor current is certainly derived at both outputs, and thereby the output voltage ripple is affected by the ESR and the current I_{LSW}. As shown in (1) and (2), the lower output voltage ripples are generated through the reduction of the I_{LSW} value. In other words, given the material-dependent value of ESR, minimizing the current I_{LSW} can helps reduce the output voltage ripples, as well as the steady-state cross regulation. That is, although the first terms in both (1) and (2) cannot be alleviated due to the design specifications, the energy mode transition operation can help get lower I_{LSW} to further reduce the output voltage ripple.

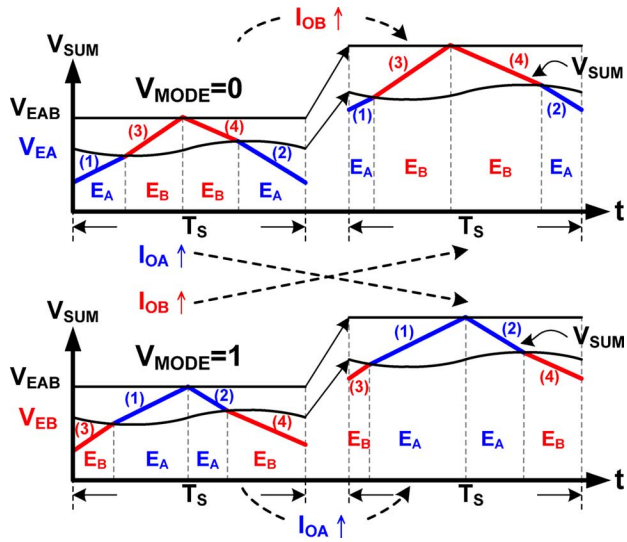

Fig. 7. Energy mode transition operation during the load transient response.

The superposition theorem can achieve the operation in proposed SIDO converter without the need of freewheel stage, and can reduce the inductor current level to obtain smaller I_{LSW} as well as output voltage ripples. However, when a large load difference occurs between the dual outputs, the output voltage ripple may increase because of the increase in I_{LSW}. For example, if I_{OA} is considerably larger than I_{OB} and the $V_{\rm MODE}$ is set to low, the area $\rm E_A$ shown in Fig. 5 would occupy most of the energy transition period in one switching cycle. That is, I_{LSW} and the output voltage ripple will increase. This phenomenon, which is considered as the steady-state cross regulation, is resulted from the unchanged energy delivery scheme that the $V_{\rm MODE}$ is set to low. This energy operation mode cannot operate well in such as the load condition. Therefore, the combination and duration of the energy delivery paths must be adjusted according to the output load conditions.

The energy mode transient operation of the proposed SIDO converter is shown in Fig. 7. Assuming that $V_{\rm MODE}$ is initially set to low, the increase in I_{OB} leads to the increase in the inductor current with the extension of energy delivery period for V_{OB} to acquire more power. The energy delivery mode must be maintained because of the remained loading of V_{OA}. Thus, the energy path transition point is set to the lower side of the

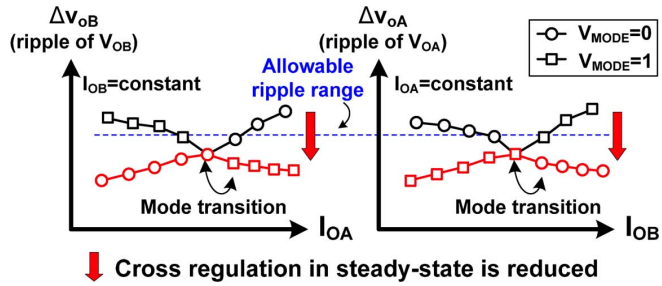

Fig. 8. Illustrations of steady-state cross regulation with output voltage ripple.

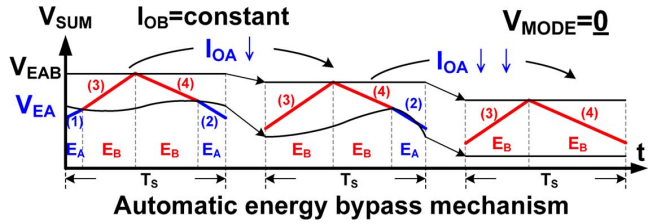

Fig. 9. Operation of the AEB mechanism with $V_{\rm MODE} = 0$.

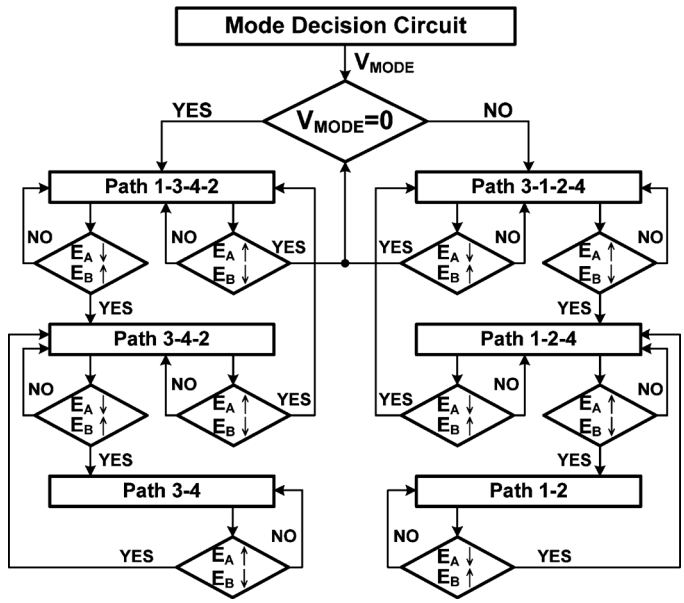

Fig. 10. Flow chart of both energy mode transition operation and AEB mechanism.

inductor current to prevent V_{OA} from being overcharged, so as to minimize the steady-state cross regulation. Conversely, once I_{OA} considerably increases, the energy operation mode changes from $V_{\rm MODE} = 0$ to $V_{\rm MODE} = 1$ to achieve a better energy delivery scheme. That is, the inductor delivers energy to the light-load output during the period with a lower inductor current, but transfers energy to the heavy-load output within the duration of the peak inductor current. A similar operation is achieved when $V_{\rm MODE}$ is set to high at the beginning of load transient response. As a result, the energy mode transition operation ensures the receipt of energy within the periods of higher and lower inductor current levels for heavy-load and light-load outputs, respectively. The operation can also help avoid overcharging during the load transient period. The voltage regulations of the dual outputs can be assured with the reduction of output voltage ripples, as well as transient and steady-state cross regulations in the proposed SIDO converter.

The steady-state cross regulation with output voltage ripple is shown in Fig. 8. As explained in Fig. 7, the energy path transition points of the two outputs, which are determined by V_{EA} when $V_{\rm MODE} = 0$ or V_{EB} when $V_{\rm MODE} = 1$, are set to the lower inductor current level. If I_{OA} increases, but I_{OB} is kept constant, $V_{\rm MODE}$ would be set from low to high, and the output voltage ripple is properly suppressed through the energy mode transient operation. Therefore, the output voltage ripples can be generated within an allowable ripple range. This result indicates that the required energy for V_{OA} is delivered from the period with a low inductor current level to the period with a high inductor current level as I_{OA} increases. Similarly, $V_{\rm MODE}$ signal would be set from high to low when I_{OB} continuously increases, but I_{OA} is maintained. Hence, the output ripple of V_{OA} can also be generated within an allowable ripple range in the steady-state operation.

On the other hand, the transient cross regulation is also enhanced through both the current-programmed energy delivery methodology and the energy mode transition operation. Output load variations can rapidly respond to the error signals for achieving the inductor current modulation owing to the current-programmed scheme. In addition, the energy mode transition operation activates when one output derives a load step. If the load in one output changes from light-load to heavy-load, the energy will provide to the relative light-load output at the beginning of each switching cycle for minimizing transient cross regulation before delivering to the heavy-load one. Thus, the light-load output with no load variation would not have large voltage drop during the load transient period because it derives a constant energy supply during the load transient period. As a result, energy is properly distributed during the load transient period to minimize the transient cross regulation. That also means the energy delivery methodology in the proposed SIDO converter is flexible, which can be automatically adjusted according to different output load current conditions.

B. Automatic Energy Bypass (AEB) Mechanism

To further enhance power conversion efficiency and ensure voltage regulation in steady-state, the AEB mechanism is used to reduce the number of energy delivery paths for lowering both the switching loss and conduction loss at the power stage, without sacrificing output voltage regulation. That is, when one output has a decreasing load condition, the existing energy delivery paths would be bypassed if the load continuously decreases. Fig. 9 shows that with $V_{\rm MODE} = 0$, the energy delivery paths 1-3-4-2 are automatically bypassed because of the PWM operation with a constant switching frequency. When I_{OA} decreases but I_{OB} remains constant, the decease in I_{OA} reduces the load dependent error signal V_{EA} owing to the characteristics of current-programmed control. As a result, path-1 is bypassed first to reduce the duration of energy delivery for V_{OA}. The maintained three energy delivery paths can ensure voltage regulation that the light-load output is not overcharged in steady-state, and the output voltage ripple is still maintained

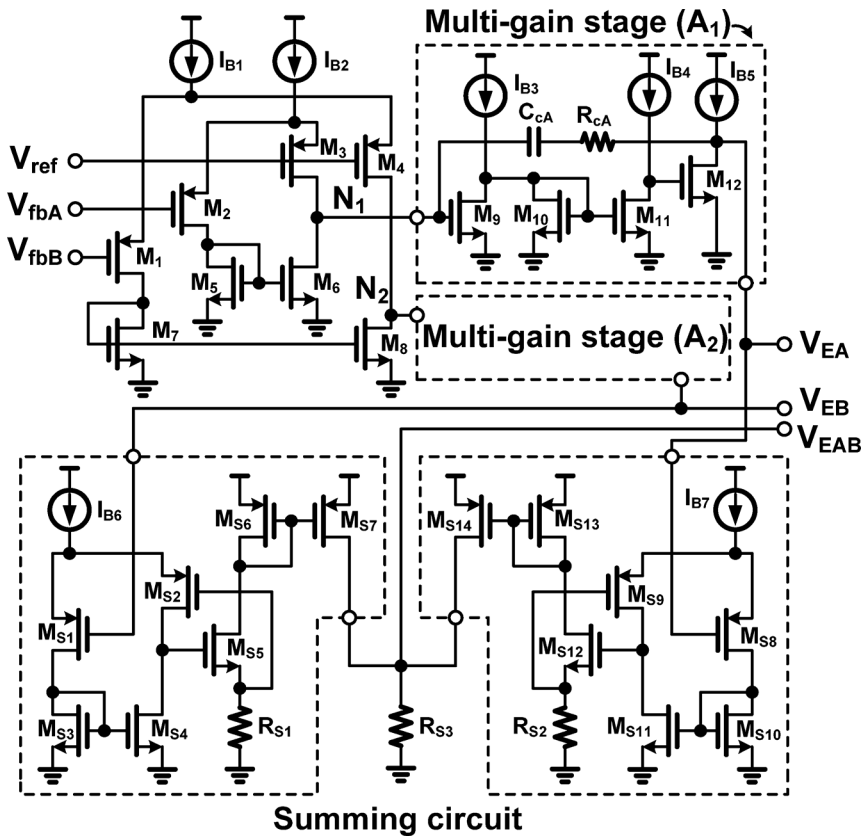

Fig. 11. Schematic of the EDRA circuit.

within an allowable range. Furthermore, when I_{OA} continuously decreases, that is, to the ultra light-load or no-load conditions, the energy delivery paths for V_{OA} are excluded. This indicates that the SIDO converter can achieve the single step-down operation for that specific heavy-load output when the large load difference between the two outputs is derived. Consequently, the high inductor current level resulted from the heavy-load output does not cause overcharge at the ultra light-load output because of the AEB mechanism. A similar operation is also activated when $V_{\rm MODE} = 1$ with the continuous decrease in I_{OB}.

Particularly, the AEB mechanism is achieved with the implementation of energy mode transition operation in the proposed SIDO converter because the energy mode transition operation can set the light-load output to obtain the energy during the period of the lower inductor current level. The flow chart for both energy mode transition operation and AEB mechanism is shown in Fig. 10. With these proposed control schemes, the applications become flexible since there is no specific load restriction between the two outputs. Moreover, both transient and steady-state cross regulations are alleviated since the problem of overcharge is effectively removed.

IV. Circuit Implementation

A. Energy Distribution Regulation Amplifier (EDRA)

The schematic of EDRA implemented by 55-nm core devices is shown in Fig. 11. The supply voltage can be scaled down to 1 V for achieving the low-voltage operation in the LV-EDC circuit. The EDRA is composed of two multi-gain stage amplifiers, A_1 and A_2, which act as the compensation-embedded multistage amplifiers [17] to achieve high system loop gain and on-chip compensation. The EDRA outputs error signals, V_{EA} and V_{EB}, to indicate the load conditions of the dual outputs, and thereby accomplishing the proposed dual-mode energy delivery methodology. In addition, applying the superposition theorem to the energy delivery scheme, the behavior of the proposed SIDO converter is similar to that of the conventional current-programmed buck converter [17], [18], as well as the utilization of the system compensation scheme. Two load-dependent system poles derived at each output node of the proposed SIDO converter. Thus, each of the multi-gain stage amplifiers generates the compensation pole-zero pairs to ensure system stability. The small on-chip compensation capacitor C_{cA} can be amplified through multi-gain stage A_1 to produce a low-frequency compensation pole ω_{pA} as described in

$$\omega_{pA} = \frac{1}{C_{cA} A_1 r_{o,N1}} \tag{4}$$

to stabilize the control loop of V_{OA}. $r_{o,N1}$ represents the output resistance derived at node N_1. Similarly, compensation pole ω_{pB} generated in the control loop of V_{OB} can be described as

$$\omega_{pB} = \frac{1}{C_{cB} A_2 r_{o,N2}} \tag{5}$$

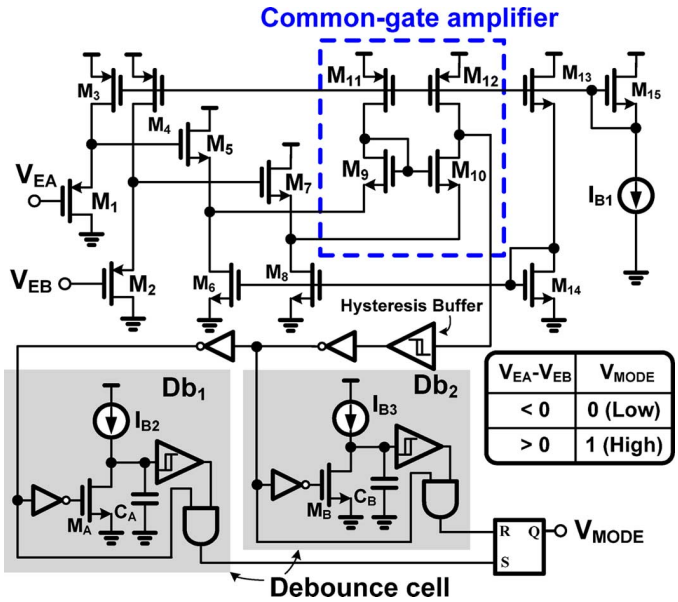

Fig. 12. Mode detection circuit.

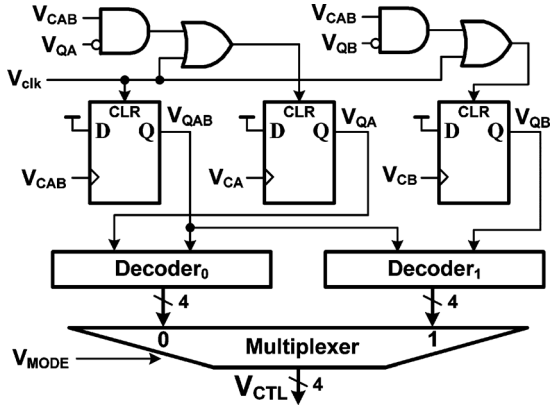

Fig. 13. Energy path decision logic.

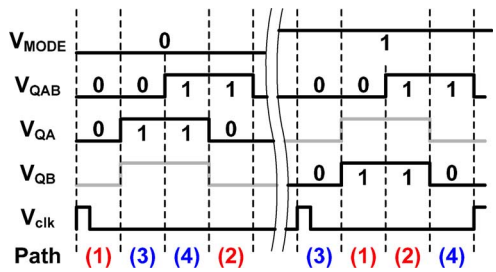

Fig. 14. Time diagram of the energy path decision logic.

with the on-chip compensation capacitor C_{cB} in the multi-gain stage A_2. Conversely, the compensation zero ω_{zA} shown as

$$\omega_{zA} \cong \frac{1}{C_{cA}R_{cA}} \tag{6}$$

is determined by the product of C_{cA} and the compensation resistance R_{cA} in the control loop of V_{OA} to cancel the effect of the system pole derived at output node V_{OA}. Similarly, compensation zero ω_{zB} in the control loop of V_{OB} can be described as

$$\omega_{zB} \cong \frac{1}{C_{cB}R_{cB}} \tag{7}$$

with C_{cB} and the compensation resistance R_{cB}.

Moreover, the summing circuit is used to generate peak current control signal V_{EAB} through the combination of both the error signals for the dual-mode energy delivery methodology. The error signals are converted to the currents by resistors R_{S1} and R_{S2} to obtain V_{EAB} across the resistor R_{S3}. As a result, good load regulation performance and correct energy delivery scheme can be guaranteed with the EDRA in the proposed SIDO converter.

B. Mode Decision Circuit

Error signals, V_{EA} and V_{EB}, contain the information of output loading owing to the current-programmed control. Fig. 12 shows the proposed mode detection circuit which appropriately decides the energy operation mode for the dual-mode energy delivery methodology. The mode detection circuit is composed of the level-shift structures, a common-gate amplifier, and two debounce cells. Transistors, $M_1 - M_4$, are used in the shift-up structures, whereas transistors $M_5 - M_8$ act as the shift-down operations. In addition, the common-gate amplifier responds faster than that does in the conventional operation amplifier, without consuming a large amount of power. The hysteresis buffer and debounce cells, Db_1 and Db_2, which delay the mode decision signal, are derived from the amplifier's output to guarantee a smooth and stable energy mode transition operation. The operations of the mode decision circuit are summarized in the attached table shown in Fig. 12. The mode decision circuit determines the energy operation mode according to the output load conditions.

In addition, the cascade level-shift structure is implemented to cope with the wide-range error signals for achieving correct operation. Because of the low-voltage operation in the LV-EDC circuit, the error signal is produced with a low voltage value, especially at the light-load conditions, owing to the current-programmed scheme. The implementation of the conventional comparator structure would suffer from the large signal delay that the compared results for mode decision and the energy mode transition operation will be deteriorated in the proposed SIDO converter. Moreover, the input of the common-gate amplifier cannot directly connect to both V_{EA} and V_{EB} because the additional bias current can affect the voltage level of the error signals, which might cause abnormal operations.

C. Energy Path Logic

Fig. 13 shows the energy path logic in the energy modulation circuit. To achieve the dual-mode energy delivery methodology, 4-bit signal V_{CTL} is produced as the control signal for power switches. V_{CA}, V_{CB}, and V_{CAB} derived from the outputs of the comparators in the energy modulation circuit depicted in Fig. 6 can be used to determine the energy path transition point. $Decoder_0$ and $\mathrm{Decoder}_1$ are used to generate the corresponding energy delivery paths of $V_{\mathrm{MODE}} = 0$ and $V_{\mathrm{MODE}} = 1$, respectively. Finally, the output signal of multiplexer, V_{CTL}, is

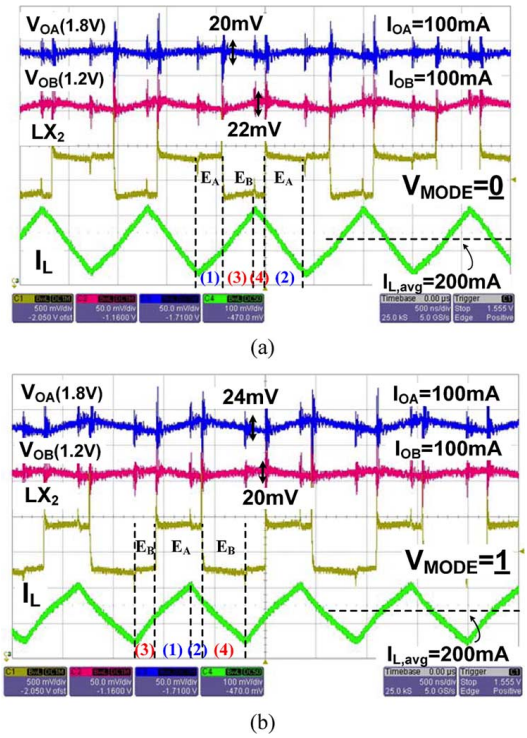

Fig. 15. Measured steady-state operation with both $I_{OA} = 100$ mA and $I_{OB} = 100$ mA when V_{IN} is 3.3 V. (a) $V_{\rm MODE} = 0$ with path 1-3-4-2. (b) $V_{\rm MODE} = 1$ with path 3-1-2-4.

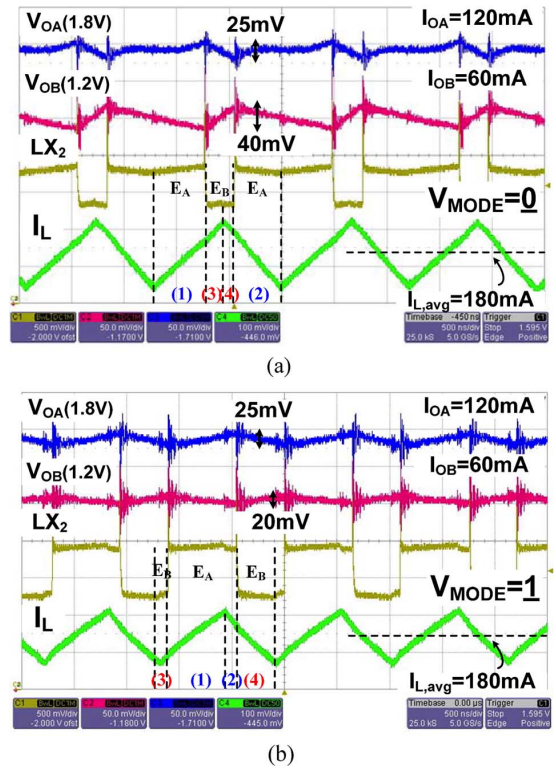

Fig. 16. Measured steady-state operation with both $I_{OA} = 120$ mA and $I_{OB} = 60$ mA when V_{IN} is 3.3 V. (a) $V_{\rm MODE} = 0$ with path 1-3-4-2. (b) $V_{\rm MODE} = 1$ with path 3-1-2-4.

selected through the $V_{\rm MODE}$ signal to realize the dual-mode energy delivery methodology. The timing diagram of the energy path logic is shown in Fig. 14.

V. Experimental Results

The proposed SIDO converter with the LV-EDC was fabricated in 55-nm CMOS technology. The nominal output voltages of V_{OA} and V_{OB} are 1.8 V and 1.2 V, respectively. Fig. 15 shows the measured steady-state operation with load currents of 100 mA at the two outputs, I_{OA} and I_{OB}. Fig. 15(a) demonstrates the ordered energy delivery paths with path 1-3-4-2 in sequence when $V_{\rm MODE}$ is set to low. The average inductor current is 200 mA, which is equal to the summation of the two output loads. The output voltage ripples are derived with 20 mV and 22 mV at V_{OA} and V_{OB}, respectively. Fig. 15(b) shows the energy delivery scheme with path 3-1-2-4 when $V_{\rm MODE}$ is set to high. The output voltage ripples are kept within 24 mV and 20 mV, respectively. That is, the energy delivery scheme can be achieved with either of the two energy operation modes when no large load difference exists between the dual outputs. Fig. 16 shows the measured waveforms with I_{OA} and I_{OB} of 120 mA and 60 mA, respectively. Fig. 16(a) shows the measured result with forcing $V_{\rm MODE}$ to low. The light-load output V_{OB} is obtained energy within the period containing the peak inductor current. Thus, the voltage ripples of V_{OA} and V_{OB} are 25 mV and 40 mV, respectively, indicating that the light-load output suffers from the steady-state cross regulation due to the incorrect utilization of the energy operation mode. Fortunately, with the operation of mode decision circuit shown in Fig. 16(b), the voltage ripple of V_{OB} is reduced to 20 mV, while

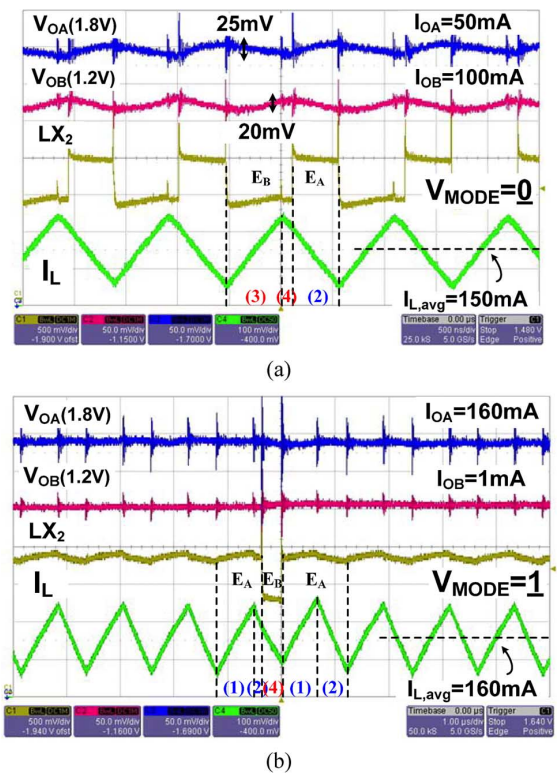

Fig. 17. Measured AEB mechanism under different load conditions when V_{IN} is 3.3 V. (a) $I_{OA} = 50$ mA and $I_{OB} = 100$ mA with $V_{\rm MODE} = 0$. (b) $I_{OA} = 160$ mA and $I_{OB} = 1$ mA with $V_{\rm MODE} = 1$.

the voltage ripple of V_{OA} is retained at 25 mV when $V_{\rm MODE}$ is changed to high. This result demonstrates the suppression of the

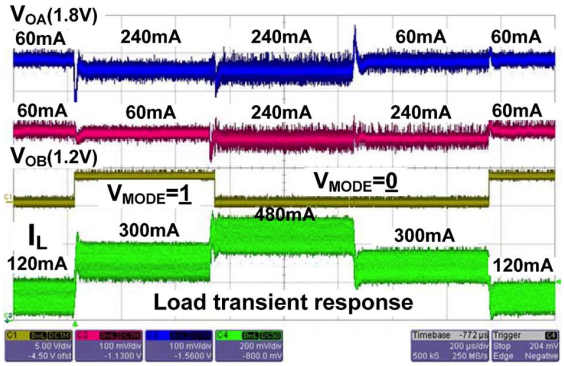

Fig. 18. Measured load transient response with energy mode transition operation.

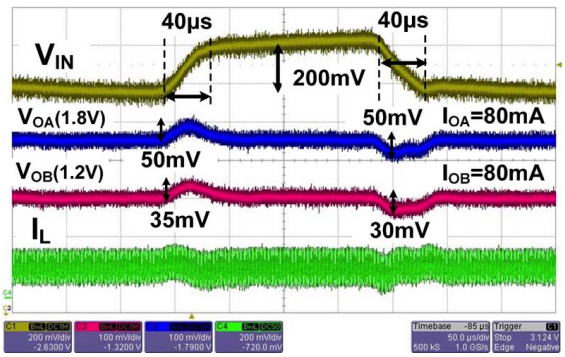

Fig. 19. Measured line transient response of a 0.2 V voltage step at V_{IN} with $I_{OA} = 80$ mA and $I_{OB} = 80$ mA.

steady-state cross regulation in the proposed SIDO converter. Fig. 17 shows the measured AEB mechanism. When $V_{\rm MODE}$ is set to low, the decrease in I_{OA} activates the AEB mechanism to bypass the energy delivery path to enhance efficiency and ensure voltage regulation. As shown in Fig. 17(a), the energy path is reduced to path 3-4-2 in one PWM switching cycle when I_{OA} and I_{OB} are 50 mA and 100 mA, respectively. Therefore, the switching loss can be reduced while voltage regulation is still guaranteed. Moreover, Fig. 17(b) shows the ultra light-load condition of V_{OB}. Through the proposed AEB mechanism, the SIDO converter can operate the single step-down operation for V_{OA} unless V_{OB} requires energy replenishment. As a result, no minimum loading restriction occurs at each output in the proposed SIDO converter.

Fig. 18 shows the measured load transient response. The load currents are initially set to 60 mA for each output at $V_{\rm MODE} = 0$. When I_{OA} is suddenly changed from 60 mA to 240 mA, the energy operation mode is changed to obtain a better energy delivery scheme, which realizes the energy delivery period of V_{OA} including the peak inductor current. Subsequently, when I_{OB} increases from 60 mA to 240 mA and I_{OA} is maintained at 240 mA, the energy operation mode is once again changed through the energy mode transient operation. Therefore, both transient and steady-state cross regulations can be minimized. The largest voltage variation is near 100 mV and the voltage recovery time is shorter than 30 μs. Particularly, the final state of the measured load transient response is identical to that in the initial state. That is, the final state derives the 60 mA load at each

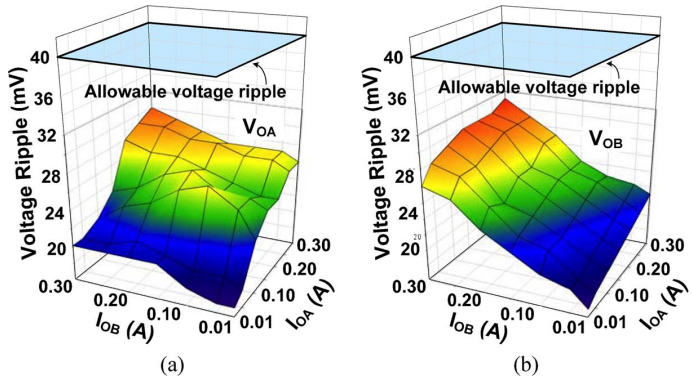

Fig. 20. Measured output voltage ripple. (a) Output ripple of V_{OA}. (b) Output ripple of V_{OB}.

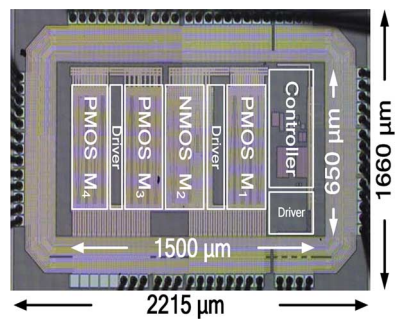

Fig. 21. Chip micrograph of the proposed SIDO converter.

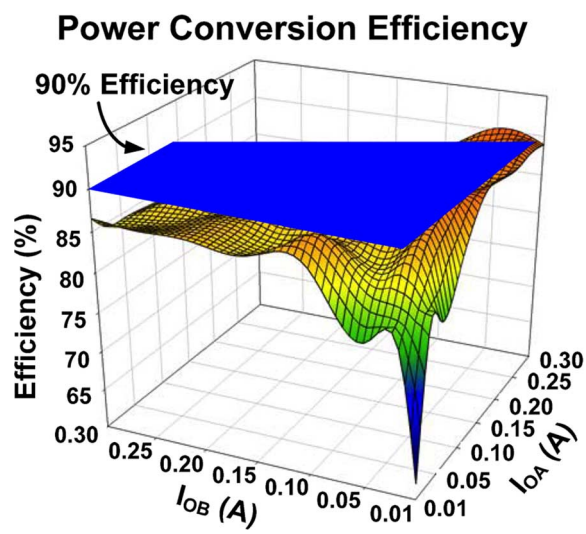

Fig. 22. Measured power conversion efficiency with $V_{IN} = 3.3$ V, $V_{OA} = 1.8$ V, and $V_{OB} = 1.2$ V.

output, but operates with the distinct energy operation mode compared to initial state. This result is caused by the hysteresis buffer in the mode decision circuit. Nevertheless, either of the energy operation modes can be utilized when the two output loads are closed as demonstrated in Fig. 16. Fig. 19 shows the measured line transient response. When V_{IN} has a voltage step of 200 mV within 40 μs, the dual output voltages derive the induced voltage variations, which are smaller than 50 mV.

Fig. 20 shows the measured output voltage ripple. Through the energy mode transition operation and the AEB mechanism,

TABLE I
DESIGN SPECIFICATIONS OF THE PROPOSED SIDO CONVERTER

Technology	55 nm CMOS process	
Input voltage	2.7 V – 3.6 V	
Inductor / DCR	4.7 μH / 200 mΩ	
Switching frequency	1 MHz	
Chip side	1500 μm × 650 μm (excluding pads)	
Outputs (nominal)	V_{OA} = 1.8 V	V_{OB} = 1.2 V
Output capacitor / ESR	4.7 μF / 30 mΩ	4.7 μF / 30 mΩ
Transient cross regulation (Load transient response)	60 mA ➔ 240 mA 240 mA ➔ 60 mA	13 mV 8 mV
	21 mV 9 mV	60 mA ➔ 240 mA 240 mA ➔ 60 mA
Steady-state cross regulation (Steady-state ripple)	w/i energy mode transition operation	
	25 mV / 120 mA	20 mV / 60 mA
	w/o energy mode transition operation	
	25 mV / 120 mA	40 mV / 60 mA
Efficiency	Max. 91 % (I_{oA}=300 mA, I_{oB}=50 mA)	

TABLE II
COMPARISONS OF OTHER SIDO (SIMO) METHODOLOGIES

	This work	JSSC 2007 [1]	CICC 2009 [5]	PE 2010 [8]	JSSC 2009 [11]
Technology	55 nm CMOS	0.5 μm BiCMOS	0.35 μm CMOS	0.25 μm CMOS	0.25 μm CMOS
Supply voltage	2.7 – 3.6 V	2.5 – 4.5 V	1.8 – 2.4 V	2.7 – 5 V	1.8 – 2.2 V
Switching frequency	1 MHz	700 kHz	1.25 MHz	1.3 MHz	660 kHz
Type	SIDO	SIMO	SIDO	SIDO	SIMO
Outputs	1.8 V / 1.2 V	5 – 12 / -9.5 V	3 – 3.6 V	1.2 V / 1.8 V	1.25 – 2.25 V
Inductor	4.7 μH	10 μH	1 μH	4.7 μH	10 μH
Output capacitor	4.7 μF	4.7 μF	4.7 μF	47 μF	33 μF
Total load current	600 mA	110 mA	600 mA	600 mA	N/A
Transient voltage drop / settling time	100 mV / 30 μs (ΔI_{load}=0.18A)	100 mV / N/A (ΔI_{load}=0.03A)	500 mV / 100 μs (ΔI_{load}=0.2A)	50 mV / 10 μs (ΔI_{load}=0.27A)	N/A
Transient cross regulation (ΔV/V)	< 2.5 %	< 1 %	< 5 %	< 2.7%	< 0.35 %
Steady-state cross regulation (Ripple)	< 30 mV	< 160 mV	< 160 mV	< 40 mV	< 22 mV
Peak efficiency	91 %	81 %	87.8 %	87 %	93 %
Active area	0.975 mm^2	8.7 mm^2	2.21 mm^2	5.29 mm^2	3.78 mm^2

the steady-state output voltage ripple can be suppressed under the allowable value. Fig. 21 shows the chip micrograph with an active core area of 0.975 mm^2. Majority of the occupied silicon area is accounted for the implementation of embedded power switches. The LV-EDC circuit has a small active area owing to the utilization of core devices in the 55-nm CMOS technology. Fig. 22 shows the power conversion efficiency. The LV-EDC circuit with a 1-V operation consumes 60 μA for achieving the correct operation. Most of the power consumption is derived from the conduction loss and switching loss in the four main power switches. The efficiency is higher than 80 % at medium and heavy loads, and reaches a peak value of 91% because of the AEB mechanism. As a result, the proposed high efficiency and wide-load range SIDO converter can be a good candidate for the power management module in SoC applications. The detailed design specifications are listed in Table I. The comparisons of other SIDO (SIMO) methodologies are shown in Table II.

VI. CONCLUSION

The proposed SIDO converter with LV-EDC circuit can minimize cross regulation in both transient and steady-state. The dual-mode energy delivery methodology can regulate the output voltages and keep the output voltage ripple within an allowable ripple range. The energy mode transient operation can exchange the energy operation mode to obtain the optimal energy delivery scheme in accordance with different output load conditions. Moreover, the AEB mechanism can bypass the energy delivery paths to ensure voltage regulations, and reduce switching loss for further enhancing efficiency. The test chip occupies an active area of 0.975 mm^2 through the fabrication of 55-nm CMOS technology. Experimental results show the correct operation of the SIDO converter under different energy operation modes, and reach 91% peak efficiency with the allowable output voltage ripple for SoC integration.

ACKNOWLEDGMENT

The authors wish to thank Energy Pass Incorporation for their help.

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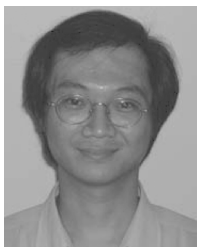

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