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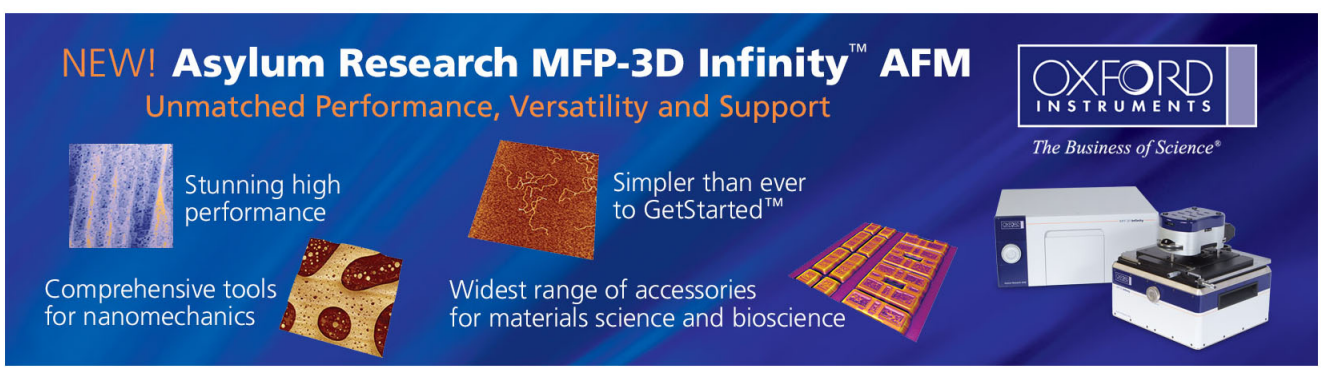

Effect of graded-temperature arsenic prelayer on quality of GaAs on Ge/Si substrates by metalorganic vapor phase epitaxy

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The growth of GaAs epitaxy on Ge/Si substrates with an arsenic prelayer grown with graded temperature ramped from 300 to 420 °C is investigated. It is demonstrated that the graded-temperature arsenic prelayer grown on a Ge/Si substrate annealed at 650 °C not only improves the surface morphology (roughness: 1.1 nm) but also reduces the anti-phase domains' (APDs) density in GaAs epitaxy (dislocation density: $\sim 2 \times 10^7\,cm^{-2}$). Moreover, the unwanted interdiffusion between Ge and GaAs epitaxy is suppressed by using the graded-temperature arsenic prelayer due to the low energy of the Ge-As bond and the use of a low V/III ratio of 20. © *2011 American Institute of Physics*. [doi:10.1063/1.3656737]

Currently, the installation of InGaP/InGaAs/Ge multi-junction solar cells is limited by the relatively high cost of III-V solar cells as compared to silicon-based solar cells.[1] Therefore, the integration of the GaAs/Ge/SiGe heterostructure on Si substrates as an alternative template for low cost and high conversion efficiency III-V based solar cells has attracted much attention.[2,3] However, many growth challenges exist in the GaAs/Ge heterostructure, including anti-phase domains (APDs), misfit dislocations, and the interdiffusion of the Ga, As, and Ge atoms. APD formation in the GaAs/Ge heterostructure can be suppressed by adjusting growth conditions such as the growth temperature, the substrate misorientation angles, and the Ge film annealing process.[4–6] In general, the abovementioned methods induce atomic surface steps on the Ge layer. The formation of surface steps can boost the single-domain GaAs-A growth, in which the first atomic layer on the surface of Ge layer is arsenic (As) atoms, and promote the self-annihilation of APDs during GaAs/Ge heterostructure growth. Besides, Luo *et al.*[6] also pointed out that anti-phase boundaries (APBs) in the GaAs/Ge heterostructure were the routes for Ge diffusion into the GaAs layer. They demonstrated that termination of APD formation led to reduction in the interdiffusion in the GaAs/Ge heterostructure.

In order to decrease the interdiffusion probability of As and Ge atoms, a low-temperature epitaxial technique and various interfacial layers such as AlAs, Ga, and As (Refs. 7 and 8) were used for the GaAs/Ge heterostructure growth. However, the low-temperature growth of GaAs on the Ge layer led to the formation of GaAs-B domain, which generated APDs in the GaAs layer, and As-antisite defects on the terraces.[5,9] Although a thin AlAs prelayer grown between GaAs and Ge epitaxy suppressed the interdiffusion of Ge atoms, diffusion of Al atoms into the GaAs epitaxy was observed at higher growth temperatures (>540 °C).[7] In contrast, the growth of the Ga prelayer between Ge and GaAs epitaxy decreased the As and Ge interdiffusion as compared to the growth of As prelayer,[8] but the APD formation in GaAs/Ge system was difficult to avoid. Therefore, the development of an advanced technique that can suppress the unwanted interdiffusion while maintaining the lower APD formation in the GaAs/Ge system is necessary for the development of low-cost and high-efficiency III-V optoelectronic devices on Si substrate.

In this paper, we present the use of an As prelayer grown using graded-temperature technique for the suppression of APD formation. This layer is also found to improve the surface morphology and reduce the interdiffusion during the GaAs/Ge/Si heterostructure growth. All samples in this study were grown by a low-pressure metal organic chemical vapor deposition (MOCVD, EMCORE D180) using trimethylgallium (TMG) and arsine (AsH_3) as the source materials. The substrates used were the Ge epitaxy on Si (001) substrate with 4° off misorientation toward the [110] direction. A detailed description of the growth of Ge epitaxy on Si substrate can be found elsewhere.[10] The As prelayer was deposited onto the Ge epitaxy while the substrate temperature was ramped from 300 to 420 °C. Then, GaAs layers with different V/III ratios (11–75) were grown on the As/Ge/Si heterostructure by a low-temperature epitaxial technique (450 °C). The Ge/Si substrate was annealed at 650 °C to generate atomic surface steps before the GaAs/As epitaxial growth.[4] The surface morphology of the GaAs/Ge/Si heterostructure with graded-temperature As prelayer was examined using atomic force microscopy (AFM). The threading dislocation density and crystalline quality of the grown sample were estimated using transmission electron microscopy (TEM) and high resolution x-ray diffraction (HRXRD), respectively. Finally, the interdiffusion of Ga, Ge, and As atoms in the samples was determined by secondary ion mass spectrometry (SIMS).

Figure 1 illustrates the AFM images of the GaAs/As epitaxy grown on the Ge/Si heterostructure. The root mean square (RMS) roughness of the samples was about 7.0, 2.3,

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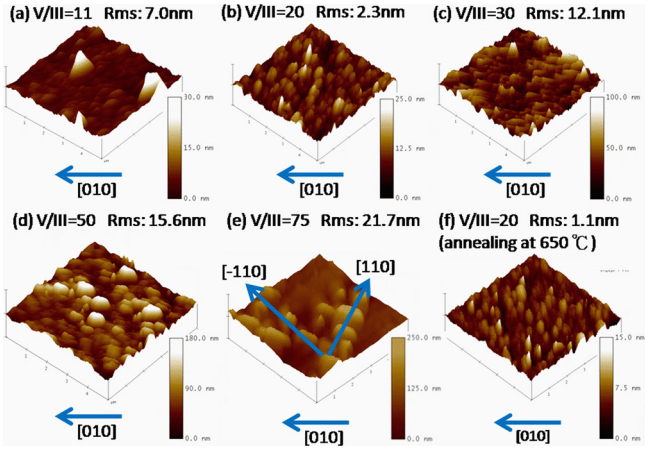

FIG. 1. (Color online) AFM images (5 μm × 5 μm) of GaAs layer with different V/III ratios grown on a Ge/Si substrate using a graded-temperature As prelayer: (a) V/III: 11, (b) V/III: 20, (c) V/III: 30, (d) V/III: 50, (e) V/III: 75, and (f) V/III: 20 and annealed at 650 °C.

12.1, 15.6, and 21.7 nm for the GaAs layers grown with V/III ratios of 11, 20, 30, 50, and 75, respectively. A large variation in the surface roughness with hill-and-valley structures was observed for the samples grown with inappropriate V/III ratios. At the low V/III ratio of 11 (i.e., lower As flow), the possibility of Ga atoms being incorporated into GaAs epitaxy exceeds that of As atoms, leading to poor surface morphology and APD formation.[11,12] For V/III ratios larger than 30, the surface morphology becomes rougher because of the different growth rates at different growth orientations.[13] The growth rate of GaAs epitaxy in the [110] direction is faster than that in the [−110] direction for higher V/III ratios and at lower growth temperature.[13,14] It is known that a high V/III ratio is required for the growth of the GaAs/Ge/(Si) heterostructure without any interfacial layer.[11,15] The results shown in Figs. 1(a)–1(e) indicate that the graded-temperature As prelayer sufficiently improves the surface morphology of GaAs epitaxy grown on Ge/Si substrate at a low V/III ratio of 20, even at a growth temperature of 450 °C. Controlling the surface structure is another efficient way to suppress APD formation prior to the GaAs/As growth.[4] It is demonstrated that the smallest RMS roughness of 1.1 nm was achieved for the samples grown using the graded-temperature As prelayer with substrate annealing process at 650 °C, as shown in Fig. 1(f).

Figure 2 illustrates the cross-sectional TEM images of the GaAs epitaxy (V/III: 20) grown on the Ge/Si heterostructure using a graded-temperature As prelayer. It can be seen that many APDs were formed in the GaAs layer on the unannealed Ge/Si substrate (threading dislocation density: $\sim 1 \times 10^8\,\mathrm{cm}^{-2}$), as shown in Fig. 2(a). For the substrate annealed at 650 °C, an APD-free GaAs epitaxy with lower dislocation density ($\sim 2 \times 10^7\,\mathrm{cm}^{-2}$) was obtained (Fig. 2(b)). These results suggest that, following the short annealing process at high temperature, surface transition may occur on the Ge surface that generates many extra atomic surface steps[4] to provide better As coverage. In the selective-area diffraction pattern diffracted from the GaAs/As interface area, only the GaAs diffraction spots exist along [110] zone axis as shown in Fig. 2(b). This observation suggests that the

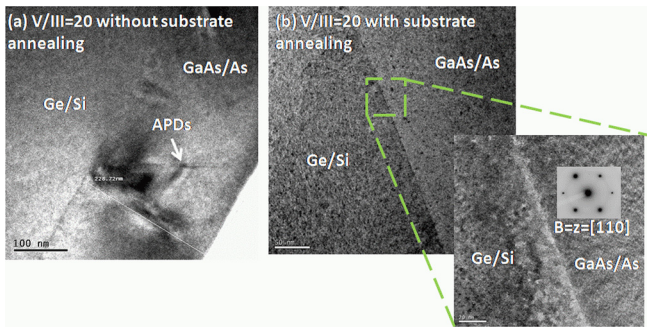

FIG. 2. (Color online) TEM cross-sectional micrograph of GaAs/As/Ge/Si heterostructure grown at a V/III ratio of 20. (a) Unannealed Ge/Si substrate and (b) Ge/Si substrate annealed at 650 °C.

graded-temperature arsenic prelayer enhances the As concentration on the Ge surface, which can be verified by Figs. 4(a) and 4(e), and does not generate different crystal structure in the GaAs/As epitaxy. This implies that As coverage formed on the Ge/Si substrate did not change the structural configuration of GaAs/Ge epitaxy. The As prelayer grown on the Ge/Si substrate annealed at 650 °C modifies the surface morphology of the GaAs epitaxy and reduces the APD formation.

Figure 3 illustrates the HRXRD results of the GaAs/As epitaxy on both the unannealed Ge/Si substrate and the Ge/Si substrate annealed at 650 °C. In regard to the change of GaAs Bragg angle (∼45 arc sec) for these two samples, we speculated that carbon incorporation may have played a role in the GaAs epitaxy with low V/III ratios. The lattice contraction is attributed to the incorporation of substitutional carbon during the growth of the III-V materials, as discussed in a recent study.[16] The HRXRD and SIMS results show that the substrate annealing process effectively reduced carbon incorporation into the GaAs epitaxy, as shown in Figs. 3 and 4(f). Furthermore, full width at half maximum (FWHM) value of the GaAs peak decreased from 402 to 250 arc sec, which confirms that annealing step improves the GaAs crystal quality.

Figure 4 illustrates the SIMS depth profiles of Ge, As, and Ga atoms in the GaAs epitaxy grown on the Ge/Si heterostructure using the graded-temperature As prelayer. It is found that the interdiffusion of Ge into GaAs was suppressed for all the samples. Because the energy of the As-Ge bond (35.8 kcal/mol) is much lower than that of the Ga-Ge bond (46.7 kcal/mol),[17] the Ge atoms segregate at the As prelayer before the deposition of the GaAs layer at low growth temperature. On the other hand, this implies that the As atoms can diffuse into the Ge layer easily and react with the Ge atoms. The incorporation probability of As atoms in the GaAs/Ge system could be described by Barnett *et al.*[18] and shown in Eq. (1).

$$J^{net} = \alpha^{In} + d\theta_s/dt, \tag{1}$$

The incorporation rate $\alpha^{In} = N \cdot GT$, where N and GT are the As concentration and growth rate in the film, respectively. The net flux $J^{net} = J^{sup} - J^{des}$, where J^{sup} represents the supplying flux of AsH_3 and J^{des} is the total desorption flux. The As surface coverage, $d\theta_s/dt$, is zero at steady state. For V/III ratios larger than 20 (i.e., larger As flux), the larger J^{net}

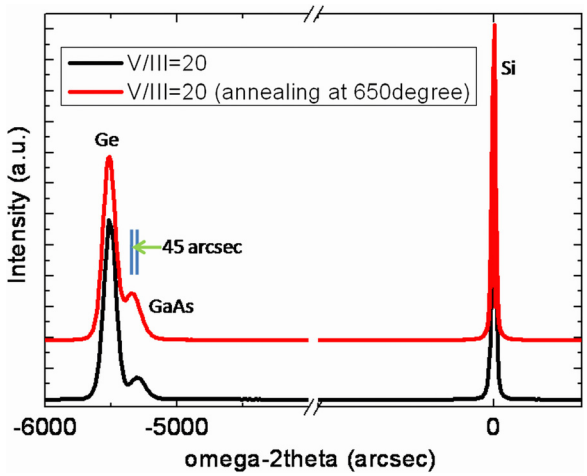

FIG. 3. (Color online) HRXRD rocking curves of the GaAs/As/Ge/Si heterostructure grown at a V/III ratio of 20. (a) Unannealed Ge/Si substrate and (b) Ge/Si substrate annealed at 650 °C.

resulted in significant As interdiffusion as shown in Figs. 4(a)–4(d). For GaAs epitaxy with a V/III ratio of 20 and the graded-temperature As prelayer on the Ge/Si heterostructure annealed at 650 °C, virtually no As interdiffusion was observed as shown in Fig. 4(e). As judged from the SIMS and TEM results, the As prelayer grown using graded-temperature technique is also an excellent candidate for suppressing interdiffusion of the Ga, As, and Ge atoms.

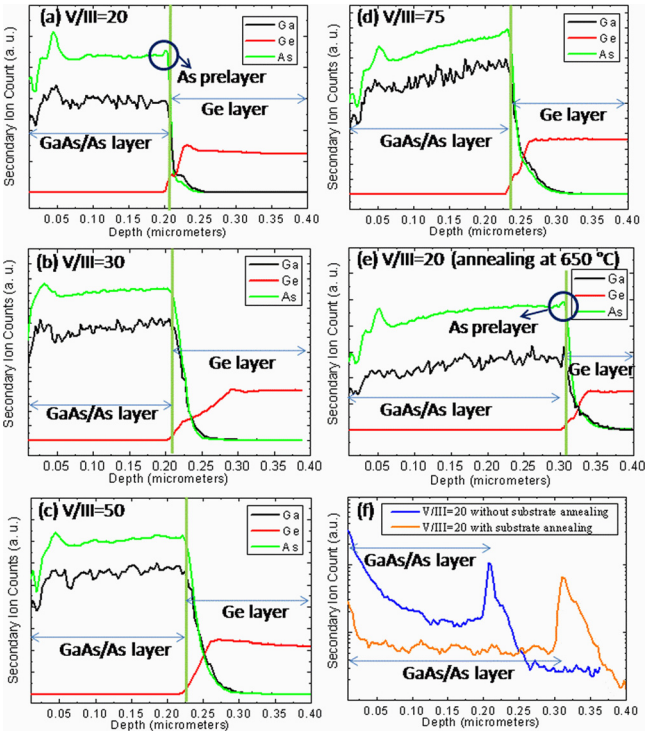

FIG. 4. (Color online) SIMS profiles for GaAs epitaxy grown at different V/III ratios on a Ge/Si substrate with a graded-temperature As prelayer (a) V/III: 20, (b) V/III: 30, (c) V/III: 50, (d) V/III: 75, (e) V/III: 20 and annealed at 650 °C, and (f) SIMS profile of carbon for the GaAs/As epitaxy grown on both the unannealed Ge/Si substrate and the Ge/Si substrate annealed at 650 °C.

In summary, we have demonstrated that the As prelayer grown using graded-temperature technique on the Ge/Si substrate annealed at 650 °C effectively improves the surface morphology of GaAs epitaxy (roughness: 1.1 nm) and avoids the need for high V/III ratios, unlike in traditional growth techniques.[11,15] The thin GaAs epitaxy grown on the Ge/Si substrate also contains lower APD density ($\sim 2 \times 10^7\ cm^{-2}$) and lower carbon incorporation when the graded-temperature As prelayer and substrate annealing process were adopted. These results suggest that the generation of atomic steps on the Ge surface promotes As deposition at lower growth temperature and boosts single-domain GaAs-A growth during the heterostructure growth of GaAs/As/Ge/Si. Furthermore, we also demonstrate that the interdiffusion of Ge and As atoms in the GaAs/Ge/Si heterostructure can be effectively suppressed by the graded-temperature As prelayer because of the difference in energies between As-Ge and Ga-Ge bonds and low As flux. These excellent results suggest that the graded-temperature As prelayer grown on Ge/Si substrate has great potential for use in the growth of III-V nanoelectronic devices and optoelectronic devices on the Si substrate.

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