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Formation and composition of titanium oxinitride nanocrystals synthesized via nitridizing titanium oxide for nonvolatile memory applications

Li-Wei Feng [a,b], Chun-Yen Chang [a,b], Ting-Chang Chang [c,d,*], Chun-Hao Tu [a,b], Pai-Syuan Wang [a,b], Chao-Cheng Lin [e], Min-Chen Chen [c], Hui-Chun Huang [f], Der-Shin Gan [f], New-Jin Ho [f], Shih-Ching Chen [c], Shih-Cheng Chen [g,h]

[a] Department of Electronics Engineering, National Chiao Tung University, Hsinchu, 300, Taiwan, ROC
[b] Institute of Electronics, National Chiao Tung University, Hsinchu, 300, Taiwan, ROC
[c] Department of Physics, National Sun Yat-Sen University, Kaohsiung, 804, Taiwan, ROC
[d] Center for Nanoscience & Nanotechnology, National Sun Yat-Sen University, Kaohsiung, 804, Taiwan, ROC
[e] Green Energy and Environment Research Laboratories, Industrial Technology Research Institute, Hsinchu, 310, Taiwan, ROC
[f] Institute of Materials Science and Engineering, National Sun Yat-Sen University, Kaohsiung, 804, Taiwan, ROC
[g] Department of Electrical Engineering, National Tsing Hua University, Hsinchu, 310, Taiwan, ROC
[h] Institute of Electronic Engineering, National Tsing Hua University, Hsinchu, 310, Taiwan, ROC

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ABSTRACT

Formation and composition analyses of titanium oxinitride nanocrystals (NCs) fabricated via treating a magnetron co-sputtered thin film of titanium and silicon dioxide with a rapid thermal annealing in nitrogen ambient were demonstrated for nonvolatile memory applications. Phase separation characteristics with different annealing conditions were examined by transmission electron microscopy and chemical bonding characteristics were confirmed by X-ray photon emission spectra. It was observed that a blanket layer composed mainly of titanium oxide was still present as annealing temperature was increased to 700 °C, associated with the thermodynamically stable phase of titanium oxide. Furthermore, a higher thermal treatment of 900 °C induced formation of a well-separated NC structure and caused simultaneously partial nitridation of the titanium oxide, thereby forming titanium oxinitride NCs. A significant capacitance–voltage hysteresis in threshold voltage shift at 1 V was easily achieved under a small sweeping voltage range of +2 V/−2 V, and a memory window retention of 2.2 V was obtained after 10^7 s by extrapolation under a 1 s initial-program/erase condition of +5 V/−5 V, respectively.

1. Introduction

In the past few years, portable electronic devices have significantly impacted consumer electronics markets. Because of the low working voltage and non-volatility, flash memory based on a floating-gate structure has been widely employed [1]. However, one problematic area for floating-gate structures is the limited potential for continued scaling of the device structure. Therefore, in recent years, nanocrystal (NC) nonvolatile memory (NVM) devices with discrete charge trapping centers have been extensively studied and discussed for use with different materials, such as metal NCs, semiconductor NCs [2–5] and even high-κ dielectric NCs [6–8], due to their ability to achieve high program/erase speed, low programming voltage, low-power performance and excellent retention and disturb characteristics [9–11]. Among these materials, titanium nitride (TiN) [12,13] and titanium oxide (TiO_2) [14] NCs have received increasing attention for NVM applications due to their advantages of high electrical conductivity (TiN)/high dielectric constant (TiO_2), larger memory window, easy fabrication, low cost, good heat stability, and especially excellent compatibility with complementary metal-oxide-semiconductor processes. Therefore, in this study, titanium oxinitride (TiN_xO_y) NCs were investigated for application in NVM because TiN_xO_y materials can act as a conductor (TiN) or an insulator (TiO_2) by virtue of a tunable N/O ratio. There have been many preparation methods for a TiN_xO_y film reported, such as a reactive sputtering of Ti in an oxygen/nitrogen atmosphere, oxidative annealing of TiN [15], or metalorganic chemical vapor deposition [16,17]. In this study, another simple technique to synthesize TiN_xO_y in NCs structures was also proposed via treatment of a magnetron co-sputtered thin film of titanium (Ti) and silicon dioxide (SiO_2) with a rapid thermal annealing in nitrogen (N_2) ambient.

* Corresponding author at: Department of Physics, National Sun Yat-Sen University, Kaohsiung, 804, Taiwan, ROC.
E-mail address: tcchang@mail.phys.nsysu.edu.tw (T.-C. Chang).

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2. Experiment

A ~6-nm-thick tunnel oxide measured by transmission electron microscopy (TEM) observation was thermally grown by a dry oxidation process at 875 °C after the standard Radio Corporation of America (RCA) clean process [SPM: H_2SO_4 (sulfuric acid) + H_2O_2 (hydrogen peroxide), SC1: NH_4OH (ammonium hydroxide) + H_2O_2 + H_2O, SC2: HCl (hydrochloride) + H_2O_2 + H_2O, and HF dip] of a p-type silicon (100) wafer [18]. Next, a ~15-nm-thick Ti-based charge trapping layer was deposited by RF and DC magnetron co-sputtering with SiO_2 and Ti targets, respectively. The sputtering chamber was initially evacuated to a base pressure of 2.1×10^{-4} Pa and the working pressure was maintained at 0.61 Pa in argon ambient at room temperature. The RF power of the SiO_2 target was fixed at 100 W while the DC power of the Ti target was fixed at 50 W. Then, annealing treatments with different temperature conditions varying up to 900 °C were performed for 1 min in N_2 (6 N purity) ambient at a pressure of 3×10^{3} Pa. A base-pressured evacuation of about 5×10^{-4} Pa was also performed before the annealing process and the surroundings during rising and lowering of annealing temperature were filled with N_2 ambient. Subsequently, a blocking oxide of 40 nm thickness was deposited by a plasma enhanced chemical vapor deposition system at 300 °C. Finally, a 500-nm-thick aluminum (Al) gate electrode was deposited by thermal evaporation and patterned by a shadow mask with a pad radius of 0.4 mm to form a capacitor structure for electrical measurement. The schematic diagram of device structure is shown in the inset of Fig. 1a. TEM and X-ray photon emission spectra (XPS) were adopted for the microstructure analysis and chemical material analysis of the NCs, respectively. Note that the XPS analyses were carried out using a Microlab 350 with a monochromatized Al Kα X-rays source (1486.6 eV; 300 W) with XPS data adopted from the annealed samples before capping the blocking oxide. Cross-sectioned TEM samples were prepared using the focused ion beam system (FIB, SEIKO SMI3050SE; ion beam operating at 30 kV and 200–7000 pA) lift-out method and analyzed by a Philips Tecnai-20 System operating at an accelerating voltage of 200 kV. The sample thickness was about 80 nm. In addition, electrical characteristic measurements, including the capacitance–voltage (C–V) hystereses and retention characteristics, were performed by a HP4284 Precision LCR Meter with high frequency of 1 MHz.

3. Results and discussion

To observe the phase separation after the different annealing conditions, TEM image analyses were performed. Fig. 1 shows the cross-sectional TEM images of the Ti/SiO_2 co-sputtered samples with annealing temperatures of (a) 500 °C, (b) 700 °C, and (c) 900 °C in N_2 ambient for 1 min. In Fig. 1a, a continuous trapping layer structure was still observed after an annealing treatment of 500 °C. However, when the annealing temperature was increased to 700 °C, the trapping layer was observed to segregate partially and incompletely, as shown in Fig. 1b. Furthermore, after the 900 °C annealing treatment, observation of clear NC dot structures was visually confirmed, shown in Fig. 1c, where an NC density of ~6.2×10^{10} cm^{-2} could be roughly estimated. The NCs were most probably surrounded by SiO_2 as the brighter contrast with the NCs confirms, which corresponds to the XPS results discussed later. In addition, on the basis of the strong variations in contrast of the Ti-contained region between TEM images in Fig. 1, it would be reasonable to suspect a substantial migration of Ti out of the TiO_2 layer. Further, an expansion of the NC size to ~20 nm in diameter was also observed, which could be due to the severe thermal diffusion of the trapping layer after undergoing such a high annealing temperature treatment. The migration of Ti into the substrate is less than out-diffusion. This suggests that the migration of larger Ti atoms into the Si substrate would severely damage the tunneling oxide quality and then severely degrade the retention characteristic, which is unobserved in our results. Moreover, we also analyze the NCs by Fourier transformation with Gatan tool from the TEM sample, which detected the TiO, Z = [011] as shown in the inset of Fig. 1c.

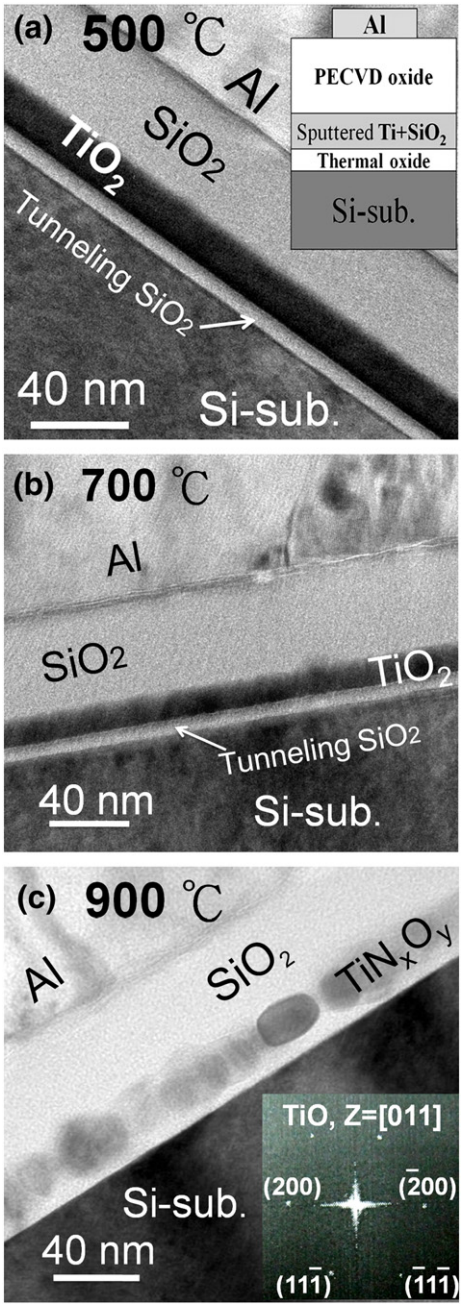

Fig. 1. Cross-sectional TEM images of the Ti/SiO_2 co-sputtered samples with annealing temperatures of (a) 500 °C, (b) 700 °C, and (c) 900 °C in N_2 ambient for 1 min. A schematic diagram of device structure is shown in the inset of a. The inset of c shows the NCs by Fourier transformation with Gatan tool.

Fig. 2 shows comparisons of XPS for O-1s, N-1s, and Ti-2p for the Ti/SiO_2 co-sputtered samples with annealing temperatures of 500 °C, 700 °C, and 900 °C in N_2 ambient. Energy calibration, necessary because of charging effects, was performed using the adventitious carbon C-1s peak at 284.7 eV. In O-1s spectrum, the main peak signal for Ti–O binding at 530 eV was observed in the 500 °C-annealed sample [19]. The Ti atom is easily oxidized since TiO_2 is a thermodynamically stable phase, and hence, the trace O_2 existing in the co-sputtering process or the absorbed O_2 on the wafer surface during wafer transportation (air exposure) is enough to cause the

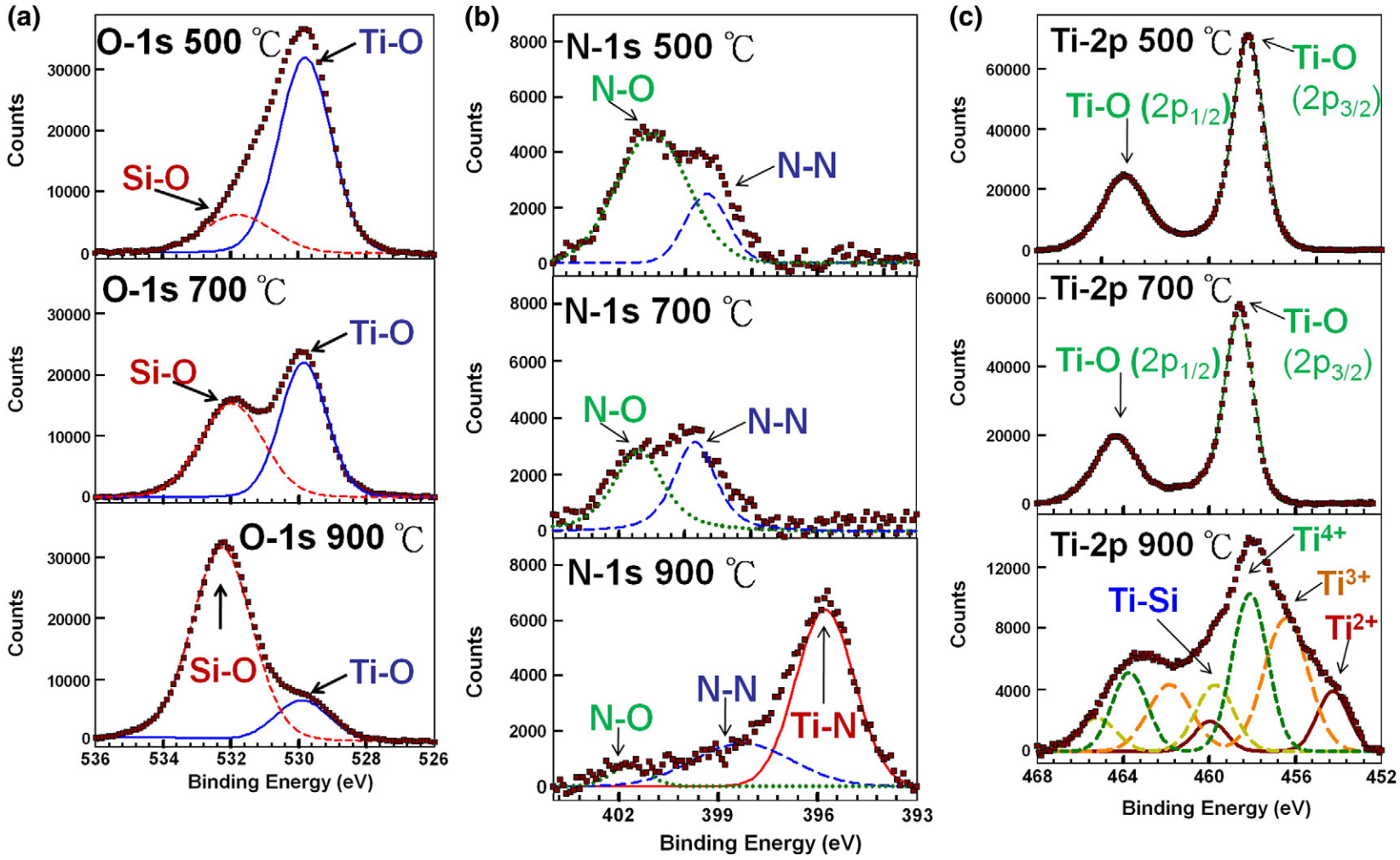

Fig. 2. Comparisons of XPS for O-1s, N-1s, and Ti-2p on the Ti/SiO_2 co-sputtered samples with annealing temperatures of 500 °C, 700 °C, and 900 °C in N_2 ambient.

formation of Ti–O bonding during the rapid annealing process [20,21]. As the annealing temperature was increased to 700 °C, the peak signal was observed at 532.6 eV, referencing Si–O binding, and was obviously enhanced while the intensity of the Ti–O peak decreased relatively [22]. Furthermore, after the 900 °C-annealing treatment, the Si–O peak began to dominate rather than the Ti–O bond. The increase of Si–O bonds and the decrease of Ti–O bonds with an increase in annealing temperature are associated with the formation of silicon dioxide around the NCs, inferred from the TEM results, as well as the partial replacement of Ti–O bonds by Ti–N bonds. In the N-1s spectrum, observations of peak signals around 400 eV and 402 eV in the samples with the 500 °C and 700 °C annealing temperatures, respectively, were representative of molecularly chemisorbed γ-N_2, caused from a small amount of N_2 molecules incorporated into the TiO_2 lattice [23]. As the annealing temperature was increased to 900 °C, a peak signal at 397 eV is clearly observed, contributed from the formation of atomic β-N [23]. Moreover, the occurrence of a positive shift of +1 V in binding energy when compared to normal Ti–N bond (396 eV) confirms the formation of titanium oxinitride bindings due to the existence of higher electronegative oxygen atoms. According to reference [22], TiN dissolution and TiO_x formation are thermodynamically favored; however, observations of these abnormal binding formations in our experiment are presumably driven by the excess of N_2 in this co-sputtered charge trapping layer. It is also mentioned that silicon nitride might also be composed while such a high temperature annealing condition is treated on the sample, but the influence of SiN could be ignored here according to the unobvious observation of Si–N peak in the N-1s spectrum, compared to the Ti–N peak. In the Ti-2p spectrum, two detectable principal peaks close to 464 and 458 eV in the samples with the 500 °C and 700 °C annealing temperatures, respectively, are representative of Ti^{4+}-$2p_{1/2}$ and Ti^{4+}-$2p_{3/2}$, contributed from titanium dioxide bonds [24]. Detection of these bonds also corresponds to the results of the O-1s spectrum due to the existence of the thermodynamically stable phase of TiO_2. However, a significant broadening of the Ti-2p lines on the lower binding energy side occurs in the sample with the 900 °C annealing temperature due to the formations of Ti^{3+} and Ti^{2+} bindings [25] as well as the Ti–Si binding at 459 eV [26]. The observation of Ti^{3+} and Ti^{2+} peaks also confirms the occurrence of nitridizing TiO_2.

Fig. 3 shows C–V characteristics of different gate voltage sweeping regions on the Ti/SiO_2 co-sputtered samples with annealing treatments of (a) 500 °C, (b) 700 °C, and (c) 900 °C. As shown in Fig. 3a, no threshold voltage shifts occurs for the 500 °C sample. Moreover, the C–V curve shifts along the negative voltage axis, which is associated with the existence of positive fixed charge in the TiO_2 layer. This suggests, therefore, that a blanket TiO_2 layer exhibits no programmable/erasable charge trapping centers for NVM applications. As the annealing temperature was increased to 700 °C (Fig. 3b), small threshold voltage shifts occur due to partial and incomplete segregation in the trapping layer. Furthermore, after the 900 °C-annealing condition, outstanding threshold voltage shifts of ~2 V, ~5 V, and ~8 V are exhibited, increasing with an increase in the gate voltage sweeping regions of 3/−3 V, 5/−5 V, and 7/−7 V, respectively. A threshold voltage shift of 1 V is easily achieved under a small sweeping voltage range of 2 V/−2 V. Explicit observation of the threshold voltage shift is mainly due to the formation of well-separated NC structures instead of

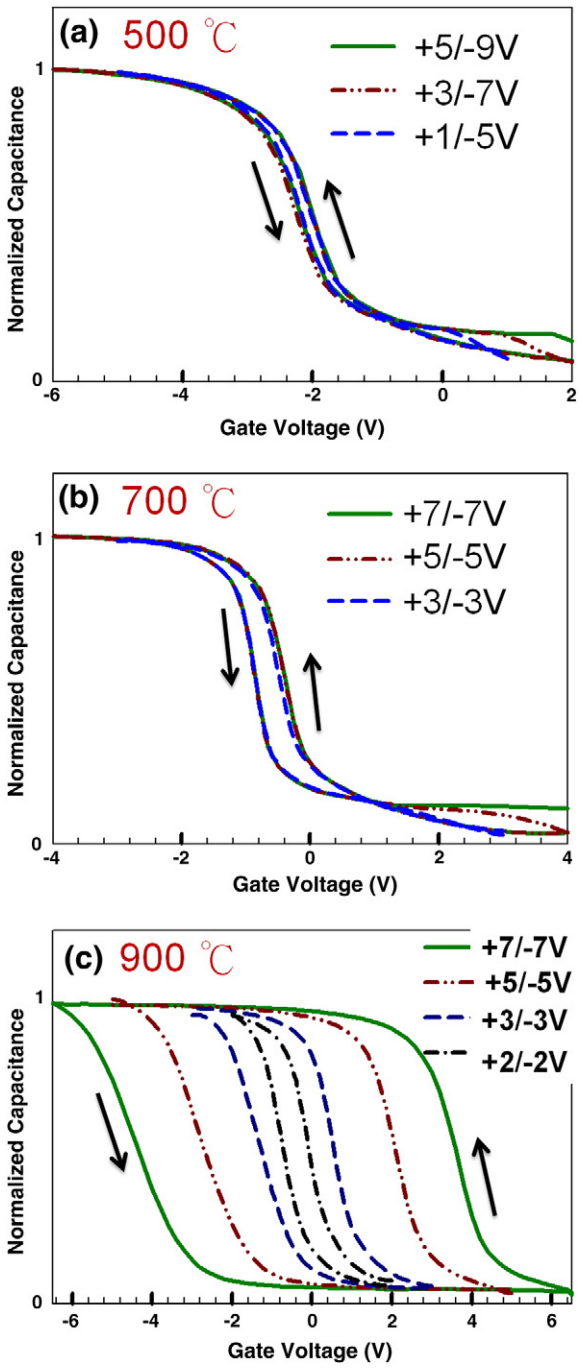

Fig. 3. C–V characteristics of different gate voltage sweeping regions on the Ti/SiO_2 co-sputtered samples with annealing treatments of (a) 500 °C, (b) 700 °C, and (c) 900 °C. The arrows indicate voltage sweeping directions.

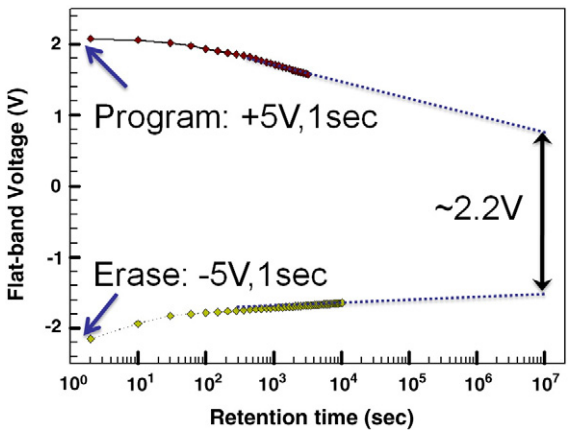

Fig. 4. Charge loss characteristic of the TiN_xO_y NC capacitor with the annealing treatment of 900 °C.

a continuous trapping layer structure, which would result in a stored carrier charge possessing lateral leak. This indicates that the TiN_xO_y NCs provide excellent characteristics for acting as charge storage centers for NVM applications, especially their potential for low power operation device applications. In addition, observation of the counterclockwise hysteresis loops of the C–V curves indicates the phenomenon of substrate injection of carriers through the tunneling oxide, which is preferable to gate injection through the blocking oxide.

Fig. 4 shows the charge loss characteristic of the TiN_xO_y NC capacitor with the annealing treatment of 900 °C. After an initial-program/erase bias condition of 5 V/−5 V for 1 s, the threshold voltage shift still remains about 2.2 V after 10^7 s by extrapolation, indicating excellent charge storage characteristic of TiN_xO_y NCs for NVM applications.

4. Conclusion

This study investigates material analyses and the formation of TiN_xO_y NCs fabricated by co-sputtering titanium and silicon dioxide targets with different annealing conditions in N_2 ambient. A 900 °C-annealing treatment induced a well-separated NC structure and nitridation of the titanium oxide to form the TiN_xO_y NCs, which provide high electrical performance for NVM applications. A significant C–V hysteresis of threshold voltage shift in 1 V is observed under the low operating voltage of +2 V/−2 V voltage sweeping. The retention characteristics were also tested to be robust.

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