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Design of a CMOS phase to digital transducer for optical incremental sensors☆

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ABSTRACT

In this paper, a CMOS phase to digital transducer for optical incremental sensors is newly proposed. The proposed chip can easily produce phase shifts of signals by using a resistor chain. A set of calibration circuits for optical incremental sensors is also designed in the proposed chip. Another innovation is that the outputs of the proposed chip are directly digitized; they could be easily sent over a wide range of transmission media, such as PSN, radio, optical, IR, ultrasonic, etc. Besides, it does not also need a ROM component or a fast counter as used in the structures of ADC-based and PLL-based interpolations. Based upon the device parameters of 0.5 μm 2P2M CMOS technology with 5 V power supply, all the functions and performance of the proposed CMOS phase to digital transducer for optical incremental sensors are successfully tested and proven through measurements. The area of the proposed chip including ESD I/O pads is 2010 × 1502 μm^2. The interpolation factor is 5, 10, and 40. The proposed chip is suitable for optical incremental sensors.

1. Introduction

The developments of precise measurement and positioning devices [1,2] have been used on the process, testing equipment of electronic and semiconductor industry. Smaller line width and more precise needs are required into nano-meter scale. Thus, the techniques of improving the accuracy and resolution on precise measurements are strongly required.

Except for the laser interferometer, the main positioning and displacement devices are linear encoders, which have the characteristics of lower cost. Among linear encoders, optical encoders are popular in modern electronic and semiconductor industry due to its characteristic of high-accuracy. Optical encoders, which consist of optical sensors and circuits, employ the light passing through the grating. Thus, the encoders generate periodic quadrature signals. The phases of these quadrature signals are relative to the movement of the grating. However, the accuracy is still restricted by optical properties and mechanical assembly. In order to improve the accuracy and resolution of optical encoders, a technique of interpolation is developed [3–10]. It improves the resolution of optical encoders by doing the subdivision of the phases. Previous method [3,4] utilizes a phase-locked loop (PLL) to achieve the interpolation. However, these achievements should design an oscillator to synthesize frequency. The design of a high-frequency PLL, which is with precision locked frequency and good linearity of an oscillator, is rather difficult. Another method [5–8], which uses an analog-to-digital converter (ADC), is used to perform the interpolation. However, this scheme needs a ROM component to perform the function of look-up table. The technology and ROM size will be another considerable issue. Besides, this scheme may need a higher system clock. For example, previous work [6] requires a clock frequency of 30 MHz. Hence, a technique, which is based on comparator-based interpolation [9,10], is proposed. However, Stephens et al. [9] and Rieder et al. [10] need to use 4 and 3 sine signals to generate signals with different phases. The processing circuits are complicated. Another issue of the interpolation error should also be discussed. The phase delay and frequency jitter of PLL produce the interpolation error of PLL-based interpolation. This error is basically related to the circuit structure of PLL. The interpolation error of ADC-based interpolation is caused by the resolution, response time, and accuracy of ADC. Although the interpolation error can be reduced by using a high resolution ADC, the response time also increases. Besides, the accuracy is related to the circuit structure of ADC. For example, nonlinear effect of ADC is a problem on the ADC-based interpolation. The interpolation error of comparator-based interpolation comes from the finite DC gain and response time of comparator. The interpolation error can be reduced by increasing the finite DC gain and speeding up the transient response of a comparator. Compared with ADC-based and PLL-based interpolations, the interpolation error of comparator-based interpolation is easily reduced by designing on the circuit

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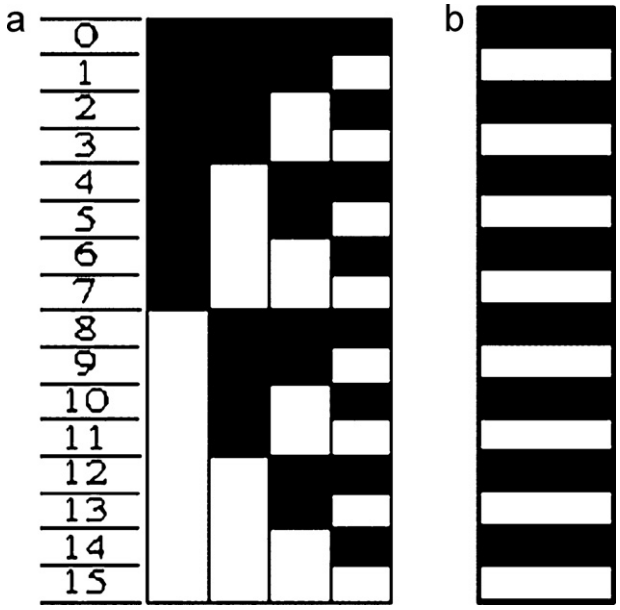

Fig. 1. (a) Optical absolute sensors and (b) optical incremental sensors.

structure of a uniform comparator. Different to previous works, an improved method [11] of comparator-based interpolation is proposed. The proposed chip can easily produce phase shifts of signals by using a resistor chain. A set of calibration circuits for optical incremental sensors is also designed in the proposed chip. Another innovation is that the outputs of the proposed chip are directly digitized; they could be easily sent over a wide range of transmission media, such as PSN, radio, optical, IR, ultrasonic, etc. Besides, it does not also need a ROM component or a fast counter as used in the structures of ADC-based and PLL-based interpolations. Relative to this work, a digital-to-phase converter is discussed in [12,13]. However, they are mainly researched on high-speed PLL or delay-locked loop (DLL). In this work, we propose an improved method and openly demonstrate how to implement a phase to digital transducer for optical incremental sensors. Readers can understand whole design techniques from this work, and this is the main contribution of this work.

In this paper, a CMOS phase to digital transducer for optical incremental sensors is newly proposed and designed in CMOS 0.5 μm 2P2M process with 5 V power supply. The area of the proposed chip including ESD I/O pads is $2010 \times 1502\ \mu m^2$. The power consumption is 50 mW. The proposed chip is suitable for optical incremental sensors.

In Section 2, the overview of optical incremental sensors is addressed. Section 3 discusses system architecture and simulation results. Section 4 demonstrates the measurements. Finally, conclusions and future works are described.

2. The overview of optical incremental sensors

Optical sensors used in the optical encoders can be distinguished into two types as shown in Fig. 1. One is optical absolute sensors and the other is optical incremental sensors. The difference between them is in the arrangements of optical grating. The distance of optical grating of incremental type is designed in equal space. The output signals are periodic signals. However, the arrangements of absolute type are totally different. The output signals just correspond to its absolute position. The design of optical grating of incremental type is easier than that of absolute type. In this paper, the incremental type is chosen and its corresponding circuit is proposed. However, due to congenital features of incremental type,

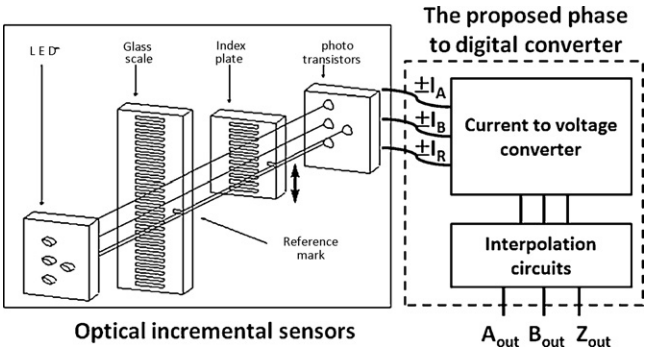

Fig. 2. Optical incremental sensors and the proposed phase to digital transducer.

measurement errors will be always accumulated. Thus, optical incremental sensors need to perform the extra calibration to eliminate the accumulated errors. The calibration method is to add a design of reference mask. As shown in Fig. 2, when a glass scale and an index plate have a relative movement, the lighting intensity of photo transistors will be changed. The output signals can be viewed as waves which are similar to sine signals as shown in Fig. 3. The output currents of optical incremental sensors are I_A, I_B, and I_R. I_A and I_B are the main input sources of the proposed chip. I_R is the current used to calibrate the accumulated errors. The period of I_A and I_B is equal to the width of an optical grating. To calculate the numbers of the period is to obtain the distance of the movement.

The resolution of optical increment sensors is limited by the width of an optical grating. If the resolution needs to increase, the width of an optical grating must also be shortened. However, the technique to make the width be less than 1 μm is rather difficult. Besides, the effects of diffraction and noise will be serious problems. This work proposes an improved method to do the subdivision of the phases. By using the proposed method, resolution can be increased without changing the width of an optical grating. The specification of the optical incremental sensor can be captured from [14]. In Section 4, the optical incremental sensor will be applied and experimented on the proposed phase to digital transducer. In the following sections, all the discussions of system architecture, simulation, and measurement results will be discussed.

3. System architecture and simulation results

The proposed CMOS phase to digital transducer for optical incremental sensors includes a current to voltage converter and interpolation circuits. The interpolation circuits as shown in Fig. 4 implement a resistor chain, comparators, and the digital processing circuits. The signals of V_A, V_{A-}, Z_{in}, and V_B are connected to the outputs of the current to voltage converter. The signals of A_{out}, B_{out}, are the digitized outputs. The output signal of Z_{out} is used to calibrate the accumulated errors of optical incremental sensors. The signal of A_{com} is the common-mode voltage. The current of I_{ref} is the bias current of comparators. The signals of Sel_0 and Sel_1 can decide the interpolation factor of 5 or 10. The signal of En is an enable signal, which can turn on or off the chip.

Fig. 5 shows the basic principle of the proposed phase-shift method. A resistor chain is built to implement the phase-shift method. The pulse signal of V_D is the output of a comparator and the signal of V_s is a phase-shift signal with phase ϕ. The phase difference of V_A and V_B is 90°. According to the superposition theorem, the voltage of V_s can be obtained as

$$V_s = \frac{R_2}{R_1+R_2}\sin(\theta) + \frac{R_1}{R_1+R_2}\cos(\theta) = \frac{\sqrt{(R_1^2+R_2^2)}}{R_1+R_2} \times \sin(\theta+\phi) \quad (1)$$

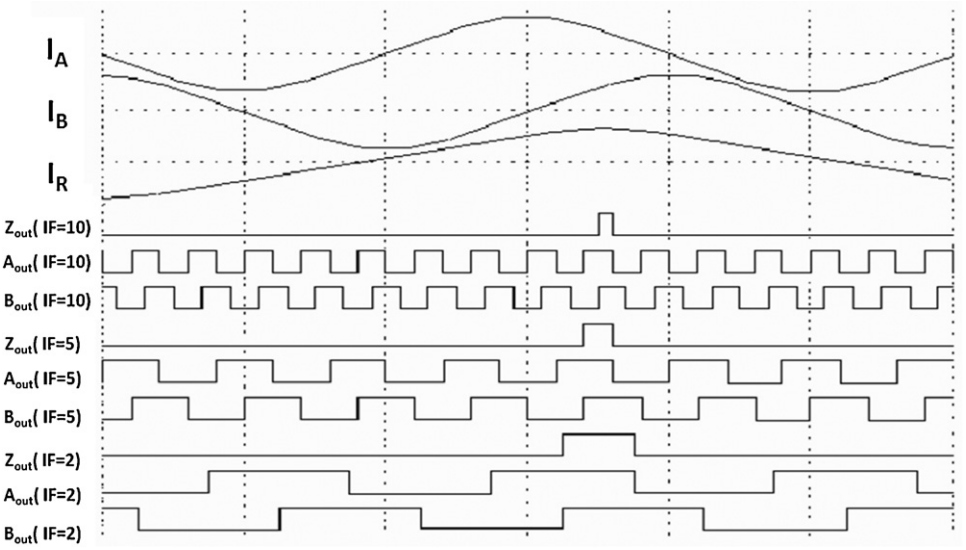

Fig. 3. I_A, I_B, and I_R are the output currents of optical incremental sensors. A_{out}, B_{out}, Z_{out} are the outputs of the proposed phase to digital transducer. The number of *IF* is the interpolation factor.

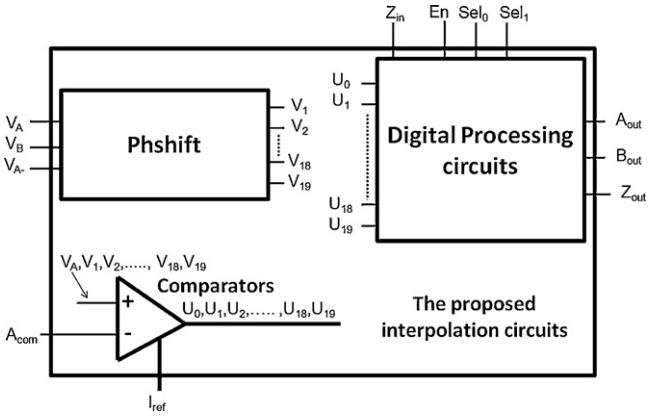

Fig. 4. The circuit diagram of the proposed interpolation circuits.

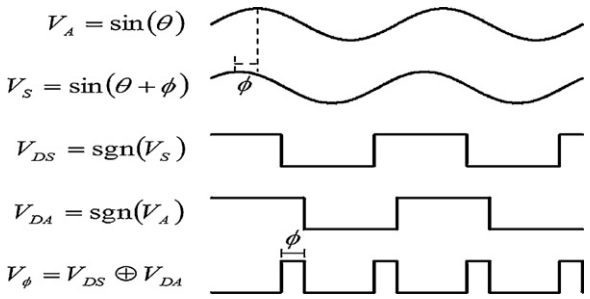

Fig. 6. The waveform of V_ϕ.

and

$$\cot\phi = \frac{R_2}{R_1} \tag{2}$$

where ϕ is the shift phase. By (2), when the ratio of R_1 and R_2 is chosen, the ϕ is attained. In Fig. 6, the signal of V_ϕ is acquired by using a XOR logic gate. That means that the V_ϕ is generated from the XOR logic function of V_{DS} and V_{DA}. The function of interpolation is implied in the signal of V_ϕ. Similarly, the proposed method can be extended into the interpolation factor of N as shown in Fig. 7. The phase difference of $\Delta\phi$ within each resistor is a fixed phase of ϕ. By following (1) and (2), each resistor R_M within a resistor chain

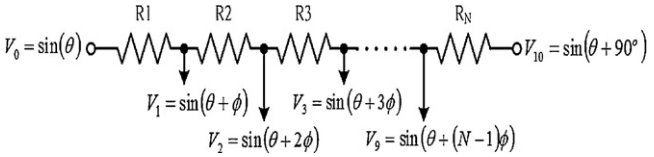

Fig. 7. The divisions of phases with the interpolation factor N. In this example, N is 10.

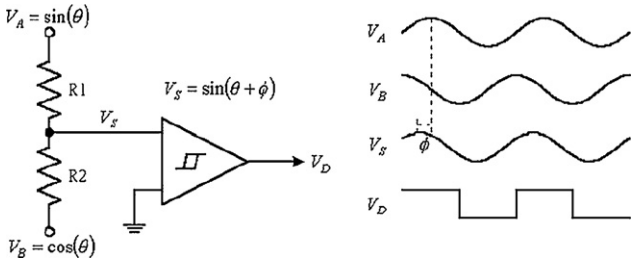

Fig. 5. The basic principle of the proposed phase-shift method.

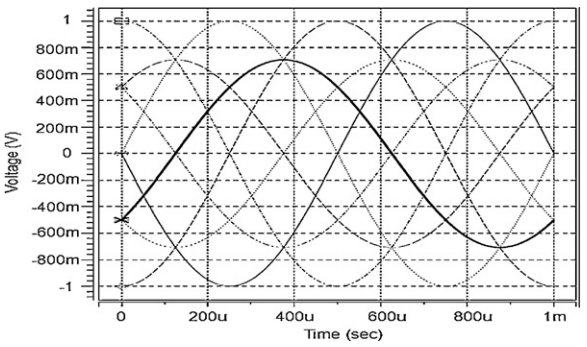

Fig. 8. SPICE simulations of the proposed phase-shift method. The interpolation factor is 8.

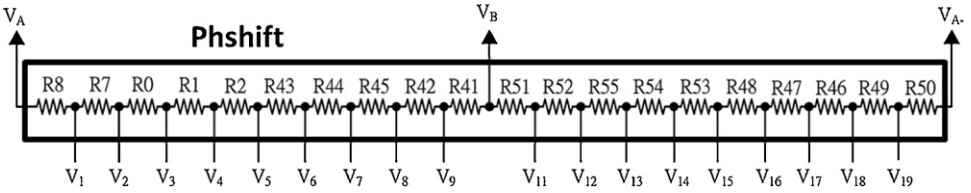

Fig. 9. The circuit diagram of phase shift shown in Fig. 4.

is derived as

$$R_M = R_{total} \times \left[\frac{1}{1+\cot[(M/N)\times 90^\circ]} - \sum_{i=1}^{M-1} \frac{1}{1+\cot[(i/N)\times 90^\circ]} \right] \quad (3)$$

where M represents the assigned number of each resistor, and R_{total} is the total resistance of a resistor chain. By (1)–(3), the phases can be easily divided by a resistor chain. For example, if N is 10 and R_{total} is 1 MΩ, 10 resistors of R_1 to R_{10} are 137 kΩ, 109 kΩ, 92 kΩ, 83 kΩ, 79 kΩ, 79 kΩ, 83 kΩ, 92 kΩ, 109 kΩ, and 137 kΩ, respectively. As shown in Fig. 8, eight phases within a resistor chain are successfully shifted.

In circuit implementation, Fig. 9 shows the circuit diagram of phase shift shown in Fig. 4. The signals of V_1 to V_{19} with different phases are generated and connected to the inputs of comparators. Fig. 10 demonstrates the circuit diagram of digital processing circuits shown in Fig. 4. The signals of U_0 to U_{19} are the output signals of comparators. They are used to perform digital processing procedures through the circuits of interpolation A and B, and the circuit of zais A and B. The circuit diagram of interpolation A and B is displayed in Fig. 11. The output signals of A_{out}, B_{out} can be attained by performing XOR logic gate. The circuit diagram of zais A and B is built by a 3-input AND logic gate. In the design of comparators, noise is always a considerable problem. In order to decrease erroneous judgements, comparators need to have a hysteresis voltage. The circuit is displayed in Fig. 12, and the hysteresis is derived as

$$V_{SPH} = Vin_+ - Vin_- = \frac{Iss}{gm} \times \frac{(\beta_B/\beta_A)-1}{(\beta_B/\beta_A)+1} \quad \text{for } \beta_B \geq \beta_A \quad (4)$$

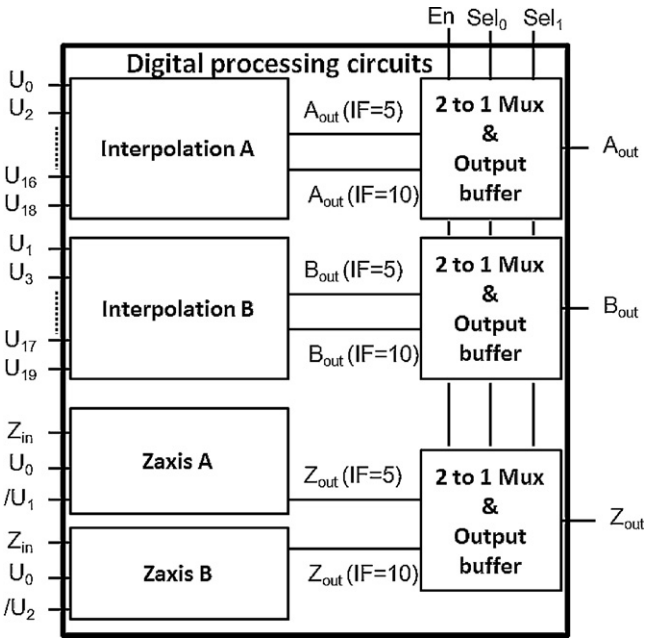

Fig. 10. The circuit diagram of digital processing circuits shown in Fig. 4.

and

$$V_{SPL} = -V_{SPH},\ \beta_B = \beta_6 = \beta_7,\ \beta_A = \beta_5 = \beta_8 \quad (5)$$

where gm is the transconductance of the MOSFET, the parameter of β is defined as $\mu_n C_{ox} W/L$, and V_{SPL} and V_{SPH} are half of hystere-

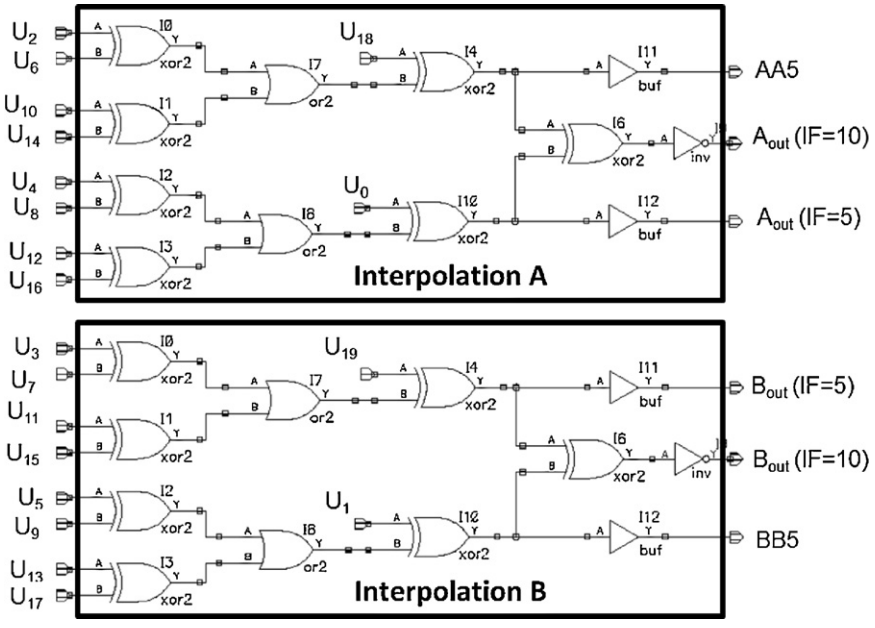

Fig. 11. The circuit diagram of interpolation A and B shown in Fig. 10.

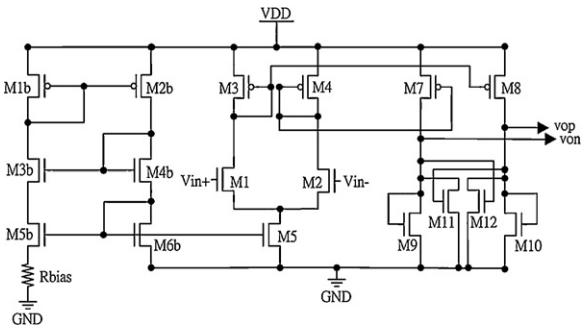

Fig. 12. Circuit schematic of the comparator.

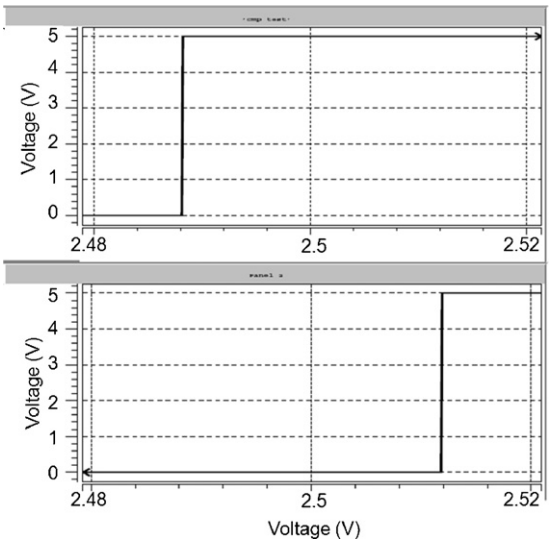

Fig. 13. SPICE simulations of the hysteresis of the comparator.

Table 1
The specification of the comparators.

V_{offset}	10 mV
$V_{hysteresis}$	24 mV
DC gain	5000
Delay time	50 ns
VDD	5 V
I_{DD}	0.5 mA

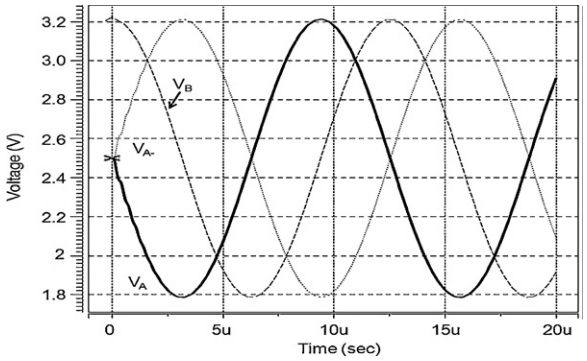

Fig. 15. SPICE simulations of the current to voltage converter.

sis voltage. After simulations, the hysteresis is 24 mV as shown in Fig. 13. The design specifications of comparators are listed in Table 1. Fig. 14 demonstrates the circuit schematic of the current to voltage converter connected to optical incremental sensors. The currents generated by sensors are $I_{\pm A}$, $I_{\pm B}$, and $I_{\pm R}$. Converted by the current to voltage converter, each corresponding voltages of V_A, V_{A-}, and V_B, are obtained as shown in Fig. 15.

Finally, the whole circuits are built and simulated. The output signals of A_{out}, B_{out}, and Z_{out} under the interpolation factor of 10 and 5 are demonstrated in Figs. 16 and 17, respectively. As demonstrated, these outputs are successfully attained. The test of integral nonlinearity (INL) and differential nonlinearity (DNL) are verified in

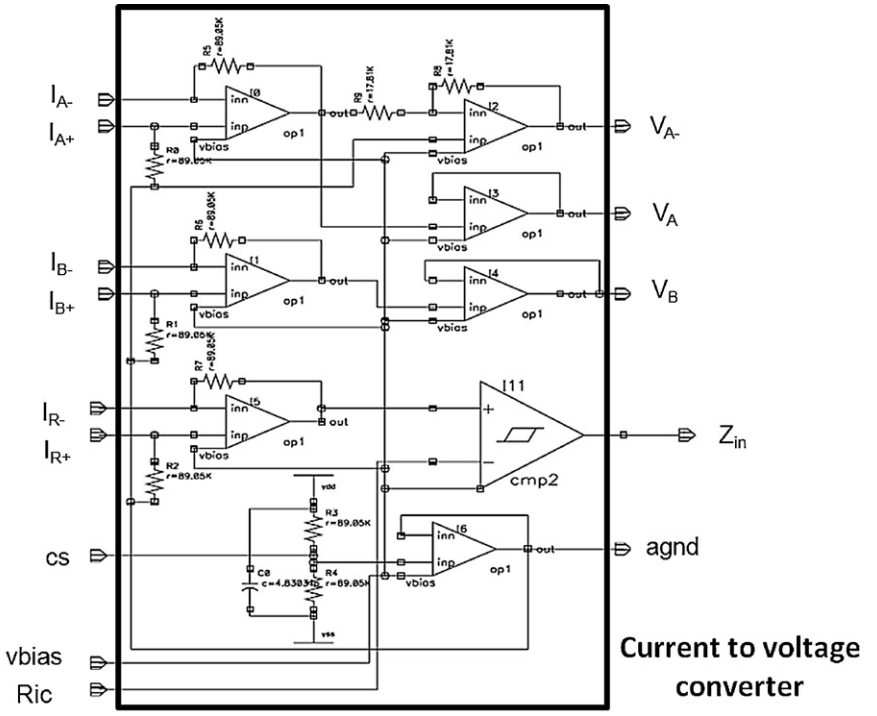

Fig. 14. Circuit schematic of the current to voltage converter connected to optical incremental sensors.

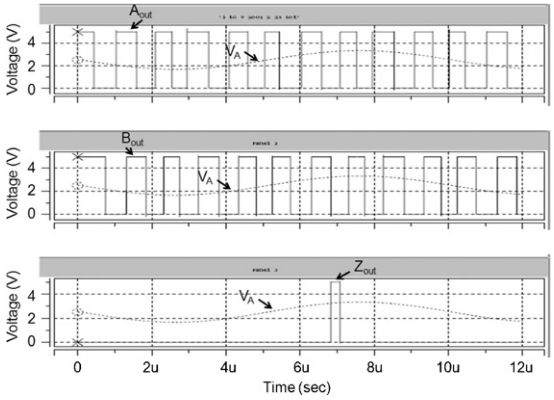

Fig. 16. SPICE simulations of A_{out}, B_{out}, and Z_{out} under the interpolation factor of 10.

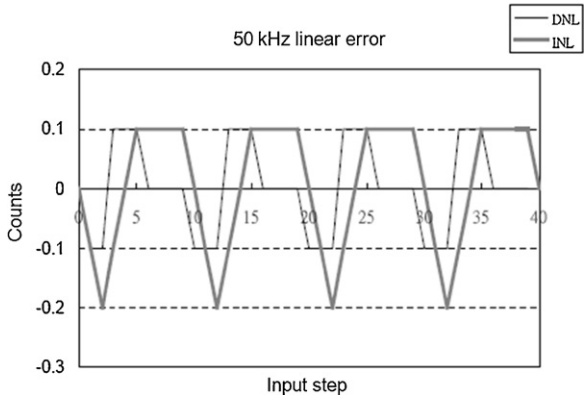

Fig. 18. The INL and DNL.

Fig. 18. Both of them are all less than 1 count, and indicate that the proposed chip has a good linearity. Although the interpolation factor can just be chosen 5 or 10, the outputs under the interpolation factor of 40 can be easily obtained by performing the XOR logic function of A_{out} ($IF = 10$) and B_{out} ($IF = 10$). However, it is optional for user choice. All the functions and performance of the proposed phase to digital transducer for optical incremental sensors are successfully tested and proven through SPICE simulations.

4. Measurement results

Fig. 19 demonstrates the microphotograph of the proposed CMOS phase to digital transducer for optical incremental sensors. In this work, the CMOS 0.5 μm 2P2M process with 5 V power supply is chosen due to its lower cost to fabricate this chip. The chip area including ESD I/O pads is $2010 \times 1502\ \mu m^2$. The power consumption is 50 mW. The measurement setup is built as shown in Fig. 20. A logic analyzer is to generate digital codes from two sine signals that have the phase difference of 90°. Undoubtedly, these two codes also have the phase difference of 90°. The currents of $\pm I_A$ and $\pm I_B$ are obtained from a digital to analog converter (DAC) and voltage to current converters marked as v2i. The current of $\pm I_R$ can be easily generated by a signal generator. Fig. 21 demonstrates

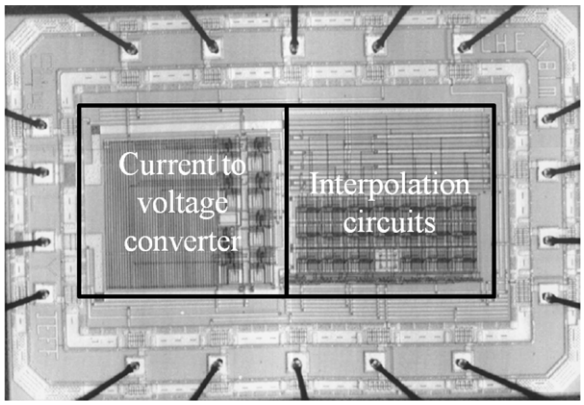

Fig. 19. The microphotograph of the proposed CMOS phase to digital transducer for optical incremental sensors is $2010 \times 1502\ \mu m^2$ including ESD I/O pads.

the measurement results under the interpolation factor of 5 and 10, respectively. The signal frequency is 50 kHz. As shown, the output signals are successfully proven. The test of the INL and DNL is displayed in Fig. 22. The INL is less than 0.8 count and DNL is less than 0.5 count. Although the value is slightly increased, it is still

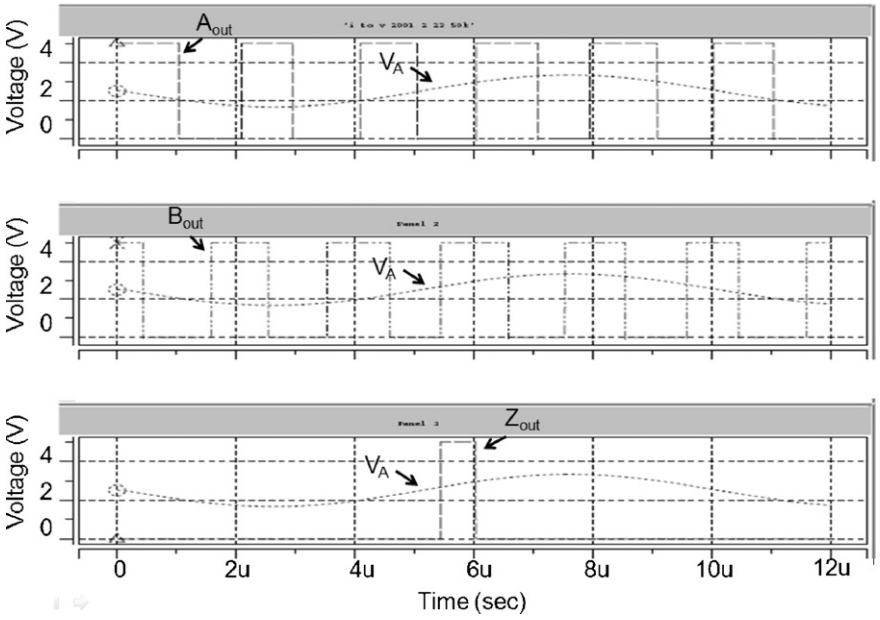

Fig. 17. SPICE simulations of A_{out}, B_{out}, and Z_{out} under the interpolation factor of 5.

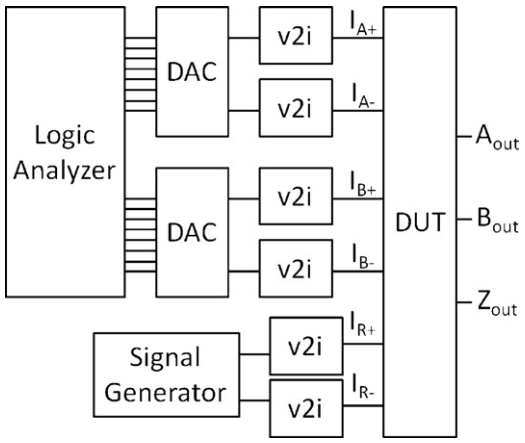

Fig. 20. The measurement setup.

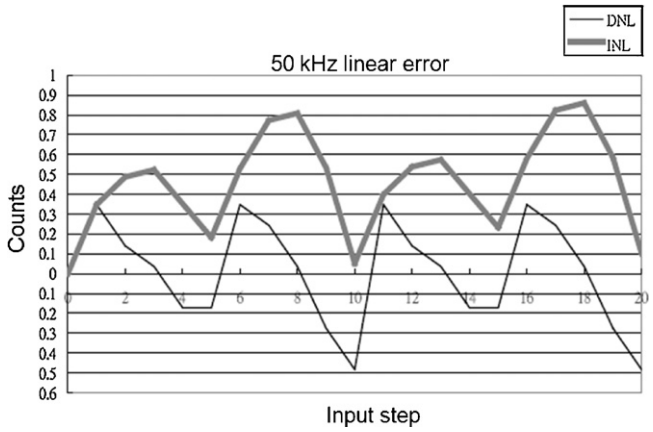

Fig. 22. The INL and DNL of the measurement results under the interpolation factor of 10. The signal frequency is 50 kHz.

Table 2
Summary on the characteristics of the proposed CMOS phase to digital transducer for optical incremental sensors.

Technology	0.5 μm CMOS 2P2M
Power supply	5 V
Interpolation factor	5, 10, 40 (optional)
Signal amplitude	±0.2 to ±0.8 V
Signal bandwidth	50 kHz
Sampling frequency	Do not need
Power consumption	50 mW
Physical layout of the proposed chip	2010 × 1502 μm^2
Application field	Optical incremental sensors

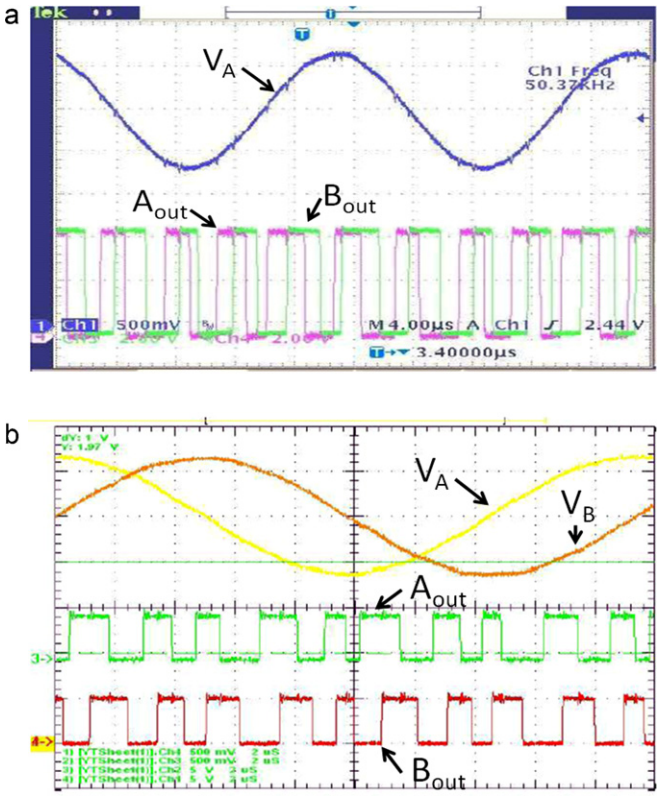

Fig. 21. The measurement results under the interpolation factor of (a) 5 and (b) 10. The signal frequency is 50 kHz.

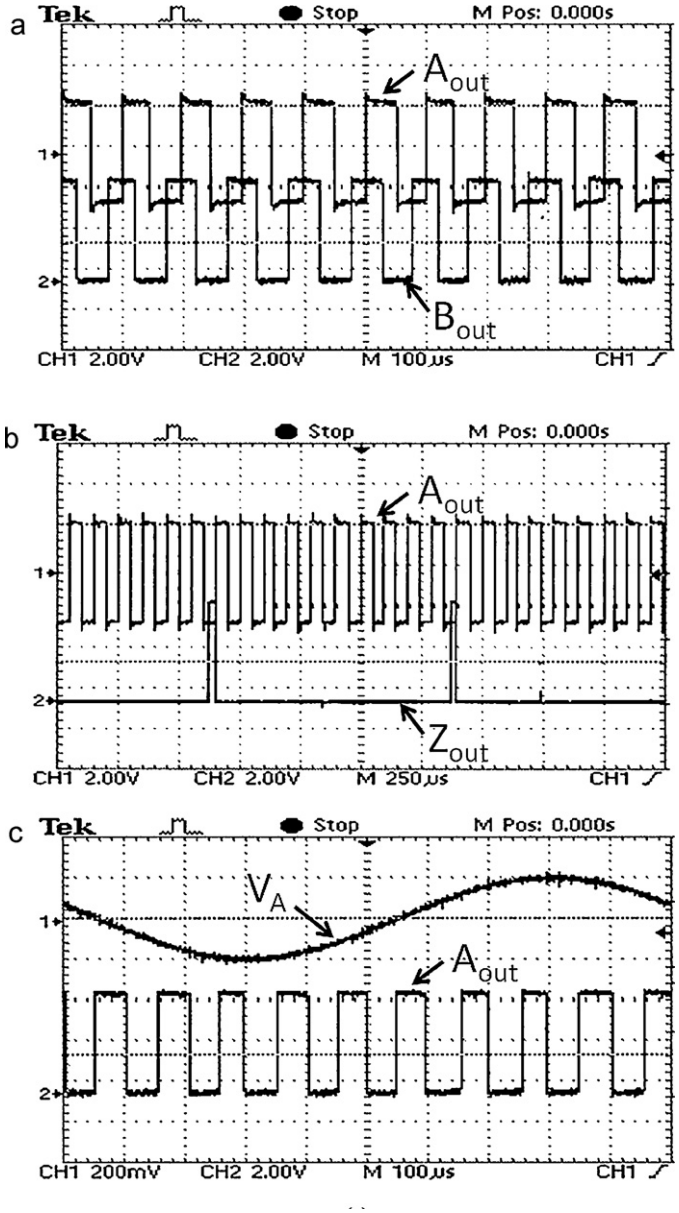

Fig. 23. The measurement results (a) A_{out}, (b) A_{out}, B_{out} and (c) Z_{out} of the proposed chip operated with optical incremental sensors. The frequency of optical incremental sensors is 1 kHz.

Table 3
Comparisons to previous jobs.

	[4]	[6]	This work
Technology		1.2 μm CMOS 2P2M	0.5 μm CMOS 2P2M
Interpolation methodology	PLL-based	ADC-based	Comparator-based
Sampling frequency	Do not need (VCO is applied)	30 MHz	Do not need
Interpolation factor	70	5, 10, 25, 50	5, 10, 40 (optional)
Output format	Sine signals	Counter code	Pulse stream
Calibration method	None	None	Provided
Chip area	N.A.	13 mm^2	3 mm^2
Differential nonlinearity	N.A.	<0.3 counts	<0.5 counts
Integral nonlinearity	N.A.	<0.5 counts	<0.8 counts

less than 1 count. That means that the non-linearity error is all less than 9° under the interpolation number of 10. The proposed chip can attain a characteristic of good linearity.

Finally, measurement results of the proposed chip operated with optical incremental sensors are performed. The frequency of optical incremental sensors is 1 kHz. The interpolation factor is 10. In Fig. 23, the outputs of A_{out}, B_{out}, and Z_{out} are also successfully obtained. The characteristics of the proposed CMOS phase to digital transducer for optical incremental sensors are summarized in Table 2. The characteristics of the proposed chip are compared with previous jobs and organized in Table 3.

5. Conclusion

A CMOS phase to digital transducer for optical incremental sensors is newly proposed. This chip adopts a proposed phase-shift method, which can easily generate phase shifts of signals by using a resistor chain. Owing to the fact that the outputs of the proposed chip are directly digitized, it does not need a ROM component and a faster counter as used in the structures of ADC-based and PLL-based interpolations. The output signals could be also easily sent over a wide range of transmission media, such as PSN, radio, optical, IR, ultrasonic, etc. All the functions and performance of the proposed CMOS phase to digital transducer for optical incremental sensors are successfully tested and proven through measurements. In the future, the developed techniques will be adaptively designed into optical devices, such as optical encoders.

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