A DVS Embedded Power Management for High Efficiency Integrated SoC in UWB System

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***Abstract*—The proposed power management module with 1 V low-voltage PWM controller and dynamic self-biasing mechanism is designed to integrate with ultra-wide band (UWB) system. The on-chip pre-regulator with power conditioning circuit provides a constant and noiseless supply voltage. Instead of using large external compensation circuit, the compensation enhancement multistage amplifier increases system loop gain and stabilizes the system. Moreover, the proposed self-biasing mechanism enhances the power conversion efficiency by 4 % through the handover technique. The fabricated power management module occupies 0.356 mm^2 silicon in 65nm CMOS. With the excellent line/load transient response and the highest efficiency about 93.5%, the proposed power management has the qualification to be integrated in today's system-on-chip (SoC) applications.**

I. Introduction

System-on-a-chip (SoC) design follows the trend of integrating embedded power management module in order to reduce print-circuit-board (PCB) area and enhance power conversion efficiency. Recently, the new integrated technique for SRAM of Sub-V_t microcontroller in 65nm technology tailored for very high digital density and mixed-signal integration applications is present in [1]. However, the switched-capacitor structure with low driving capability is not suitable for UWB system applications by contrast to the inductor-based structure. The inductor-based structure in the conventional power management module [2] has good driving capability. To further reduce the silicon area of this 65 nm UWB system, the proposed power management module adopts low-voltage devices in controller design. In addition, without the bound wire effect in SoC, the quality of output voltage in 65 nm power management module is better than the conventional inductor-based structure. Inevitably, 65 nm CMOS process introduces more design challenges owing to the limitations of the low-voltage deep-submicron devices for analog circuits, especially for low-voltage controller design.

As conceptually illustrated in Fig. 1, the embedded power management module in UWB system contains two individual power sources V_{out1} and V_{out2} to supply radio frequency (RF) and digital circuits, respectively. This proposed architecture minimizes the demand for high-voltage devices by means of low-voltage PWM (LV-PWM) controller with on-chip compensation. Besides, dynamic voltage scaling (DVS) technique and self-biasing mechanism are implemented in the proposed power management to effectively improve the efficiency, and thus extend the battery life.

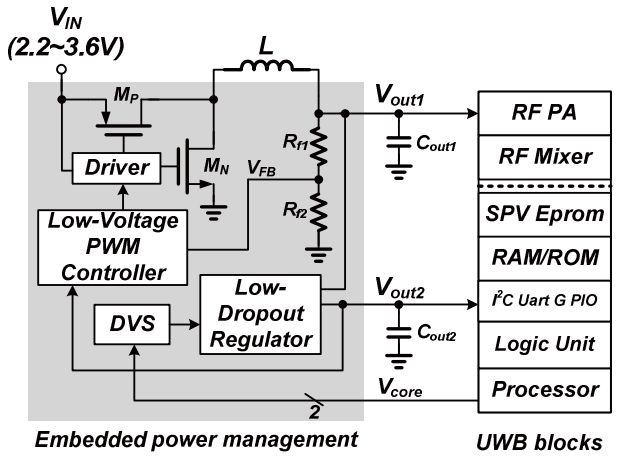


Figure 1. The architecture of proposed power management module in UWB system.

Two figures of merits (FOM1 and FOM2) shown in (1) and (2) evaluate the performance of power management module in steady-state and in transient responses, respectively. The proposed 65 nm 1 V low-voltage controller is described in Section II. Experimental results are shown in Section III. Conclusions are made in Section IV.

$$\text{FOM1} = \frac{Area \cdot V_{out\_ripple}}{\eta \cdot I_{load\_\max}} \quad \begin{cases} Area\text{: chip area} \\ V_{out\_ripple}\text{: output voltage ripple} \\ \eta\text{: conversion efficiency} \\ I_{load\_\max}\text{: maximum load current} \end{cases} \tag{1}$$

$$\text{FOM2} = \frac{P \cdot T_R \cdot V_{drop}}{\Delta I_{load}} \quad \begin{cases} P\text{: power consumption} \\ T_R\text{: transient recovery time} \\ V_{drop}\text{: transient dip voltage} \\ \Delta I_{load}\text{: transient load step} \end{cases} \tag{2}$$

II. Proposed Low-Voltage Circuit Implementation

Low-voltage PWM (LV-PWM) controller betters the embedded power management module in cost and performance. In Fig. 2, the pre-regulator supplies a stable, noiseless and constant power V_{pre} for the LV-PWM controller. The handover decision circuit is implemented to take over the supplying voltage of the LV-PWM controller from V_{pre} to V_{out2} after the start-up procedure to improve power conversion efficiency [3]. Besides, a compensation enhancement multistage amplifier is proposed for low-voltage operation to provide high system loop gain and stabilize the system

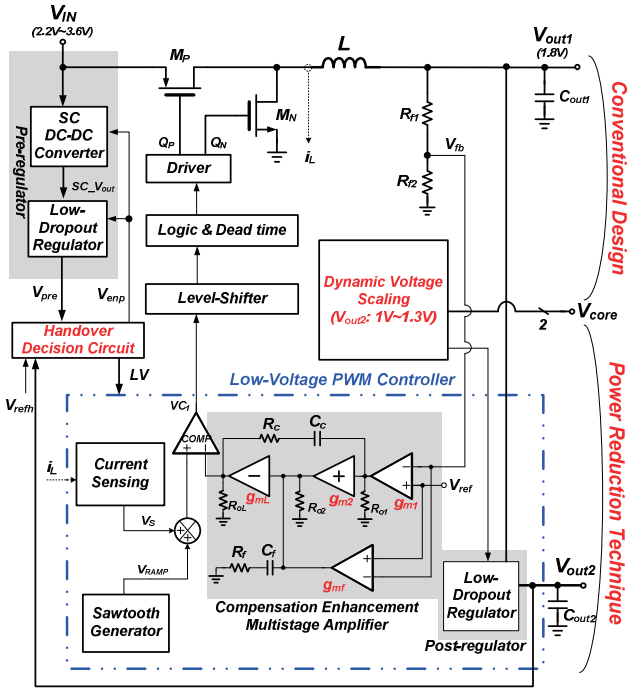


Figure 2. The proposed low-voltage PWM controller and pre-regulator in current-mode DC-DC buck converter with the power reduction technique.

without external components. Moreover, DVS technique is added to modulate output voltage V_{out2} from 1 V to 1.3 V according to the 2-bit V_{core} signal from the UWB processor. This power request can adaptively scales V_{out2} to meet the UWB system performance in different mode operation.

A. Pre-Regulator Design

Generally, low dropout regulator inhabits a drawback of poor efficiency in large conversion ratio [4]-[5]. To supply constant and noiseless power to the core controller, a simple and high efficiency pre-regulator is the design object. In order to increase power conversion efficiency in 65 nm SoC power management module, the pre-regulator, composed of a low dropout regulator and a switched-capacitor (SC) DC-DC converter, is proposed.

In Fig. 3, the proposed pre-regulator can effectively improve the power conversion efficiency through the use of a scaling output voltage. That is, the high input voltage V_{IN} can be stepped down to a lower voltage SC_V_{out} by a predetermined factor (*1/2X*, *2/3X*) automatically. Besides, SC_V_{out} can directly connect to V_{IN} when the input voltage is lower than 2.5V. As a result, the auto-bypass function allows the handset to operate at a lower battery voltage. According to the experimental result, the conversion efficiency can always be kept at 50~80% and the switching ripple of SC_V_{out} can be suppressed due to the post-regulator, designed by a low dropout regulator. Therefore, the 1.2V output voltage of the pre-regulator will be used to supply the proposed LV-PWM controller at start-up period.

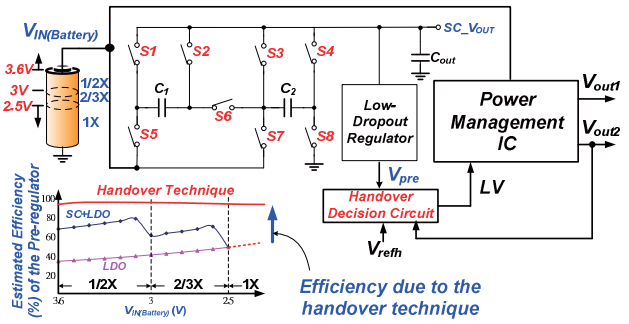


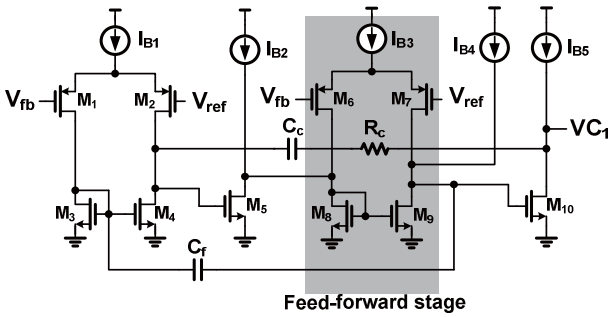
Figure 3. The efficiency improvement method of the proposed pre-regulator from the LDO to the SC+LDO and further to the handover technique.

Besides, the proposed handover technique is activated after the start-up period. Through the handover decision circuit, the V_{out2} takes over the job of the pre-regulator to supply power to the LV-PWM controller. Consequently, the pre-regulator can be shut-down to further enhance the power conversion efficiency. It is an imperative predominance in the highly integrated SoC system.

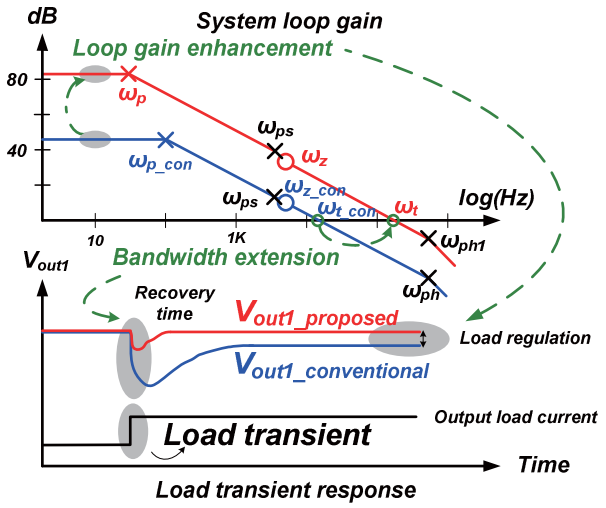
B. Compensation Enhancement Multistage Amplifie

For the LV-PWM controller, low supply voltage limits the gain of error amplifier (EA), implying a deteriorated regulation performance. Fig. 4(a) shows the schematic of the proposed compensation enhancement multistage amplifier (CEMA), which improves both system loop gain and bandwidth. Instead of using large external compensation capacitor [2], a small on-chip capacitor C_c (5 pF) generates a low-frequency pole ω_p as the system dominant pole. The feed-forward gain stage generates the compensation zero ω_z to cancel the output filter pole ω_{ps}. In addition, the resistor R_c can further push the compensation zero ω_z to a lower frequency position to achieve nearly optimum pole-zero cancellation for increasing system stability.

Moreover, another small capacitor C_f (2pF) is implemented to separate the complex poles of the CEMA structure. Compared with the convention EA in Fig. 4(b), fast transient response and good load regulation is achieved by CEMA owing to its enhanced loop gain and optimal system compensation. CEMA not only helps achieve good line/load regulation and on-chip compensation but also decreases the silicon area compared to conventional designs.



(a)



(b)

Figure 4. (a) The circuit of CEMA. (b) The performance of CEMA compared with conventional EA.

C. *Handover Technique for Self-Biasing Mechanism*

Since the pre-regulator generates a noiseless and constant supply voltage for the LV-PWM controller, it suffers extra power consumption from the SC switching conduction loss. Therefore, in order to enhance the power conversion efficiency, the handover decision circuit shown in Fig. 5(a) determines either V_{pre} or V_{out2}.to be the supply voltage for the LV-PWM controller, while V_{out2} naturally provides a stable supply voltage as well as V_{pre}.

When V_{out2} becomes larger than V_{refh} after the soft start period, the handover decision circuit starts to turn the supply voltage from V_{pre} to V_{out2} and achieves self-biasing mechanism. With the delay of D-flip-flops, the supply voltage of the LV-PWM controller can hand over smoothly without incorrect action and shutdown the pre-regulator. Thus, the power conversion efficiency can be enhanced. The time diagram of the handover procedure is shown in Fig. 5(b). Equally important, to ensure correct operation, the pre-regulator would be reactivated again when the post-regulator is disabled.

On the other hand, the dynamic voltage scaling (DVS) is also applied to adjust the output voltage V_{out2} of 1 V to 1.3 V according to the power request from the processor in the UWB system of different mode operations. Owing to the work of self-biasing technique, the LV-PWM controller is designed to operate under 1 V supply voltage in the cause of the idle mode in the UWB system. Therefore, the output voltage of V_{out2} can closely fit the power request and can effectively reduce the power consumption. Furthermore, it will powerfully increase the competitiveness of the proposed power management module in today's SoC applications.

III. Measurement Results

Fig. 6 shows the load transient response from 200 mA to 450 mA with an undershoot voltage of 70 mV and a recovery time of 4 µs, while the load current changes from 450 mA to 200 mA with an overshoot voltage of 50 mV and a recovery

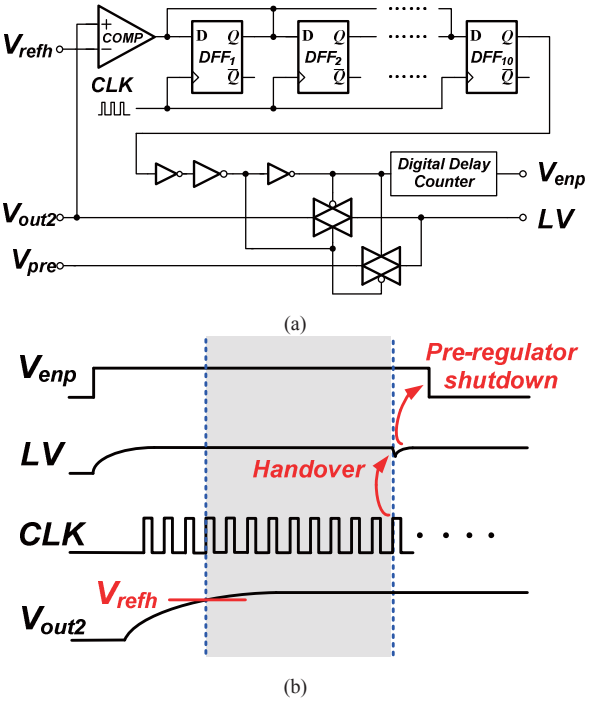


Figure 5. (a) The proposed handover decision circuit for self-biasing (b) Time diagram of the handover sequence.

time of 6 µs. The output voltage (V_{out1}) is 1.8 V with 15 mV voltage ripple. Besides, the quiescent current of the LV-PWM controller is only 50 µA (60 µW @ 1.2 V). Owing to the design of CEMA, the load regulation is 25 mV/A @ V_{IN}=3.3 V, and line regulation of V_{out1} is 16.25 mV/V when V_{IN} steps up from 2.5 V to 3.3 V and vice versa at 200 mA load condition.

The handover technique is shown in Fig. 7. While the pre-regulator is disabled, implying the end of the start-up period, it induces a small output variation, about 150mV, in V_{out1}. Moreover, the pre-regulator would be reactivated when V_{out2} is below 0.9 V in the case of large output voltage variation. Fig. 8 shows the power conversion efficiency of proposed power management module. The handover technique further increases the efficiency in both light load and heavy load by 4% and 2%, respectively.

Table I shows the design specifications. The chip micrograph of the complete UWB system with embedded power management module is shown in Fig. 9. The chip photo of the power management module is emphasized on the left side, which occupies 0.356 mm^2. The die area is effectively reduced by 30% owing to the LV-PWM controller compared to the conventional design with high-voltage devices (3.3 V drain extended device) only. Table II lists the comparisons of two figures of merits (FOM1 and FOM2) for evaluating the steady-state and transient response of the prior power management module.

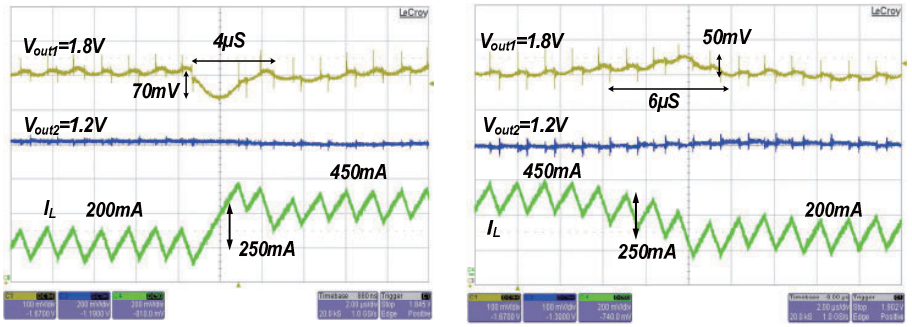


Figure 6. Measured load transient response. (a) The load changes from 200mA to 450mA. (b) The load changes from 450mA to 200mA.

TABLE I : DESIGN SPECIFICATIONS OF PROPOSED POWER MANAGEMENT

Technology	65nm CMOS
Input voltage	2.2V~3.6V
Inductor (off-chip)	4.7μH
Capacitor (off-chip)	4.7μF
On-chip compensation capacitor	5pF
Switching frequency	800KHz
Output voltage 1 (Vout1)	1.8V
Output voltage 2 (Vout2)	1V~1.3V
Maximum load current	600mA
Line regulation	16.25mV/V @Load=200mA
Load regulation	25mV/A @V_{IN}=3.3V
Proposed die area	734μm x 486μm

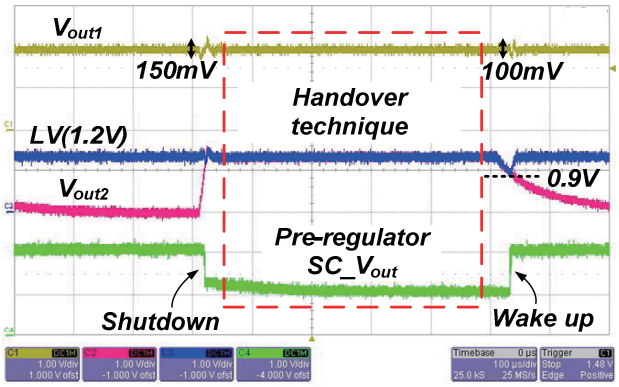


Figure 7. Measured result of handover technique for self-biasing.

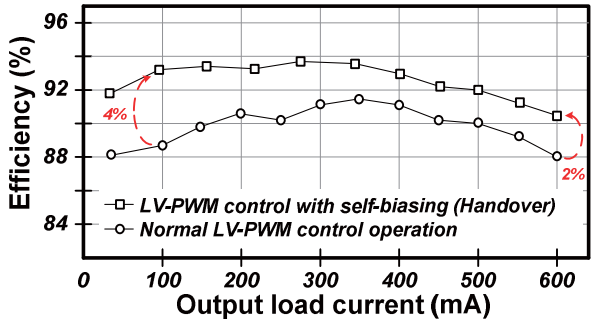


Figure 8. The comparison of power conversion efficiency.

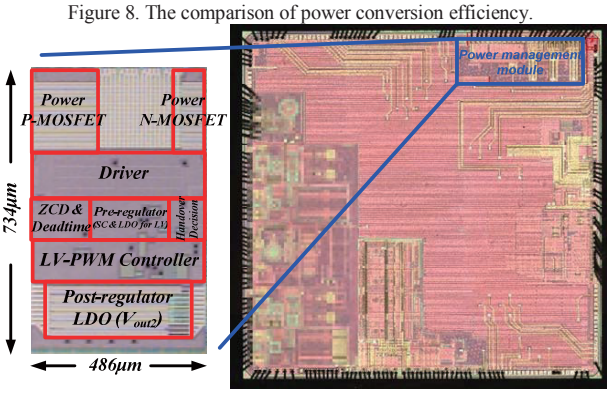


Figure 9. Chip micrograph with UWB system and enlarged proposed power management module.

IV. CONCLUSIONS

A 65 nm power management module with 1 V low-voltage PWM controller and self-biasing mechanism for the UWB system is presented. It provides a good solution for on-chip compensation and compact-sized area by CEMA and LV-PWM controller compared to the conventional design. Both handover technique and dynamic voltage scaling circuit help improve the power conversion efficiency up to 93.5% suitable for SoC applications.

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TABLE II : THE COMPARISONS OF FOM1 AND FOM2 WITH PRIOR ART

	This work	**[2]**	**[3]**	**[4]**	**[5]**
Type	**PWM Buck**	PWM Buck	PFM Buck	LDO	LDO
Technology	**65nm**	0.6μm	0.5μm	90nm	0.35μm
Area (mm^2)	**0.365**	2.87	5.3	0.03	0.0448
Switching Freq. (Hz)	**800K**	500K	3000K	N/A	N/A
Efficiency	**93.5%**	89.5%	89%	50%	83%
Power (μW)	**60**	N/A	N/A	61680	114
Max. current (mA)	**600**	450	400	1000	50
Output ripple (mV)	**15**	20	20	N/A	N/A
Recovery time (μs)	**6**	N/A	N/A	0.0002	2
Voltage drop (V)	**0.070**	N/A	N/A	0.116	0.15
FOM1	**0.01**	0.14	0.29	N/A	N/A
FOM2	**0.11**	N/A	N/A	0.002	0.684