Design, Fabrication, and Reliability of Low-Cost Flip-Chip-On-Board Package for Commercial Applications up to 50 GHz

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***Abstract*— This paper presents a flip-chip-on-board (FCOB) packaging technology using a Rogers RO3210 laminate for microwave applications. Compared to the conventional microwave packaging architecture, the proposed FCOB technology skips one level of the ceramic package and thus results in lower reflections and manufacturing costs. To fulfill the small dimension requirement on printed circuit boards, the coplanar waveguide (CPW) transmission line and flip-chip bump were fabricated on a high-k RO3210 board ($\varepsilon_r = 10.2$) with photolithography and electroplating. The GaAs chip patterned with the CPW line was then flip-chip-mounted onto the RO3210 laminate board. This structure displayed excellent performance from dc to 50 GHz with a return loss S_{11} greater than 18 dB and insertion loss S_{21} less than 0.5 dB. Meanwhile, the flip-chip bonding of the in-house-fabricated $In_{0.52}Al_{0.48}As/In_{0.6}Ga_{0.4}As$ metamorphic high-electron-mobility transistor devices on RO3210 also displayed excellent gain performance with a small degradation of 1 dB from dc to 40 GHz, showing the potential of implementing microwave integrated circuits on RO3210. To enhance the mechanical reliability, an epoxy-based underfill was injected into the flip-chip assemblies. Thermal cycling tests were performed to test the interconnect reliability, and the results indicated that the samples passed the thermal cycling test at least up to 600 cycles, showing excellent reliability for commercial applications. To the best of the authors' knowledge, this is the first study that evaluates the use of the RO3210 laminate for microwave flip-chip in open literature.**

***Index Terms*— Coplanar waveguide, fabrication, flip-chip-on-board, interconnect, metamorphic high-electron-mobility transistor device, microwave, packaging, reliability, RO3210 laminate, underfill.**

I. Introduction

As CONSUMER products and portable devices move to higher frequencies of operation, low-cost, light-weight, and compact packages with good performance are required. Generally, conventional microwave packaging involves three levels of packages: chip to module, module to printed circuit board (PCB), and PCB to motherboard. The transitions between these packaging levels result in significant reflection losses and pull down the radio frequency (RF) performance of the packaged devices. When the operating frequency moves higher, the situation becomes even worse. Besides, conventional bond wire has a significant parasitic inductance and thus induces some unwanted effects at microwave frequencies, which could compromise the device performance after assembly [1]. Hence, low-cost packaging solutions with excellent RF performance are highly sought. In this respect, flip-chip interconnect has gained much attention as a chip-level interconnect because of several advantages, such as shorter interconnect length, higher throughput, and smaller package size [2]–[6]. The integration of chip-on-board (COB) [7] with flip-chip technology by directly mounting chips onto the PCB and bypassing one level of ceramic package can not only save the manufacturing cost but also enhance the packaging performance. This is the so-called flip-COB (FCOB) packaging, which is a technique derived from low-frequency applications [8]. Fig. 1(a) shows the illustration of the conventional microwave package structure and Fig. 1(b) the schematic diagrams of the conventional RF package (two levels) and the proposed FCOB package (one level). As can be seen, the module-level (ceramic) package is eliminated by using the proposed FCOB structure, which can reduce the package cost and enhance the package performance.

In the literature, some investigations on flip-chip aseembly on PCB at the gigahertz frequency range have been reported [9]–[11]. The performance of the flip-chip assembly using coplanar strip transmission line on an RT/Duroid 6010 substrate has been reported, demonstrating a high return loss of up to 50 GHz [9]. Case reported a hybrid microwave integrated circuit amplifier with the flip-chip-attached discrete SiGe heterojuction bipolar transistor microstrip transmission lines and other distributed elements integrated on a Duroid circuit board [10]. The amplifier was designed to operate at the Ku band (12–18 GHz), and the gain (S_{21}) was around 7 dB. Xiao *et al.* reported a flip-chip-assembled 2.4-GHz Si CMOS voltage-controlled oscillator (VCO) with integrated Cu inductors on organic substrates. The flip-chip-assembled VCO showed a phase noise of 108 dBc at 600 kHz offset for a

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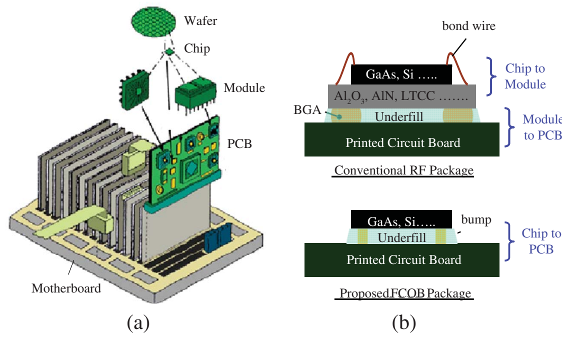


Fig. 1. (a) Illustration of conventional microwave package structure. (b) Schematic diagrams of the conventional RF package (2-levels) and proposed FCOB package (1-level).

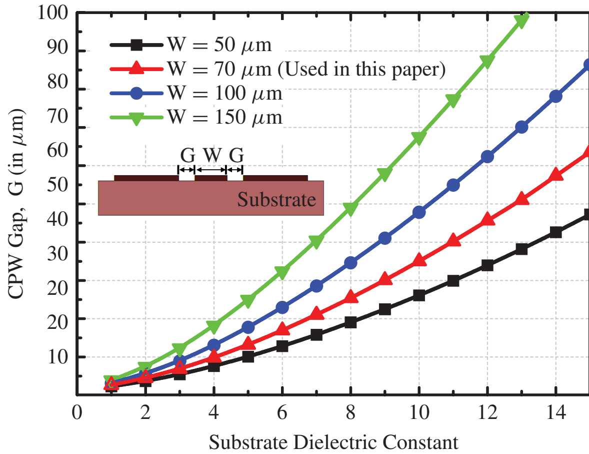


Fig. 2. Signal-to-ground gap (G) of 50 Ω CPW lines with different signal widths (W) versus substrate dielectric constant at 50 GHz.

2.4-GHz carrier [11]. These papers mainly focused on the performance demonstration of the flip-chip die attachments on PCBs. Investigations on the design, fabrication, and reliability remain insufficient.

This paper is organized as follows. In Section II, the design and fabrication concern of a CPW transmission line on PCB is discussed. In Section III, the in-house process flow of the flip-chip assembly on an RO3210 is presented. Sections IV and V present the measurement results of the flip-chip-bonded passive structure and active metamorphic high-electron-mobility transistor (mHEMT) device, respectively. The reliability test result of the FCOB structure with underfill is presented and discussed in Section VI. Finally, this paper concludes in Section VII.

II. CPW Transmission Line on PCB

On a packaging carrier, using CPW transmission line is considered to be more compatible with flip-chip technology [2]–[4]. Since the ground is at the same level as the signal line, the via hole to the backside is not necessary and thus the inductance associated with accessing ground is significantly reduced [12]. The absence of the via hole makes the CPW perform well at high frequencies at low manufacturing cost. However, for microwave/millimeter wave applications, the characteristic impedance-related physical parameters of a CPW line, i.e., signal conductor width (W) and signal-to-ground gap (G), are typically less than 100 μm, which cannot be applied in the conventional PCB process. In the conventional PCB process, the copper cladding on the surface (usually 17 or 35 μm) is wet-etched back for patterning transmission lines and passive components on the board. The wet-etching process produces an undesirable undercut profile and the structure dimensions are difficult to control [13]. Therefore, in this paper, photolithography and electroplating with low-cost film masks are proposed in order to give more precise line resolution on the PCBs.

Fig. 2 shows the G value of 50-Ω CPW lines with different signal widths (W) versus the substrate dielectric constant at 50 GHz. The substrate thickness is 650 μm. In the design rule of CPW transmission line, a low substrate dielectric constant reduces the dimension, which is difficult to fabricate. For example, for a CPW line with $W = 70$ μm on a Rogers RO4003 substrate ($\varepsilon_r = 3.38$), G is only 8 μm. However, the substrate dielectric constant of the PCBs can be tailored using polymer/ceramic composites [14]. The substrate used in this paper is a Rogers series polytetrafluoroethene based RO3210 ceramic-filled laminate reinforced with woven fiberglass and designed for high-frequency applications. Table I shows the comparison of RO3210 versus some other commonly used microwave substrates. As can be seen, RO3210 has a high dielectric constant (ε_r) of 10.2 and a low loss tangent (tan δ) of 0.0027. The high dielectric constant enlarges the dimensions of the CPW line and thus facilitates the fabrication.

TABLE I
Comparison of the Properties and Price of RO3210 Versus Some Other Commonly-Used Microwave Substrates. (The Cost Was Obtained From the Local Substrate Suppliers)

Substrate	X-Y CTE (ppm/K)	Dielectric constant	Loss factor	Cost in USD ($2'' \times 2''$)
GaAs	5.7	12.9	0.0020	88.9
Al_2O_3	6.3	9.8	0.0002	23
AlN	5.27	6.3	0.0120	42
FR-4	15	4.2–4.3	0.0015	2.02
RO3210	13	10.2	0.0027	2.56

III. Package Fabrication

Fig. 3 shows the process flow of the RO3210 board for the flip-chip assemblies. The RO3210 laminate board has an electrodeposited copper cladding on both sides of the sheet. The sheet thickness is about 650 μm and the copper cladding thickness is about 17 μm on each side. In this paper, the photolithography and electroplating processes were implemented in order to give good line resolution on the RO3210 laminate. The commercially available low-cost film mask with patterned silver bromide (AgBr) on plastic film was employed in the photolithography process. The resolution limit of the film mask is around 25 μm. First, a solution of water, sulfuric acid (H_2SO_4), and hydrogen peroxide (H_2O_2) was used to etch away the copper cladding. Then, titanium (Ti) and gold (Au) metal were deposited *in situ* using an

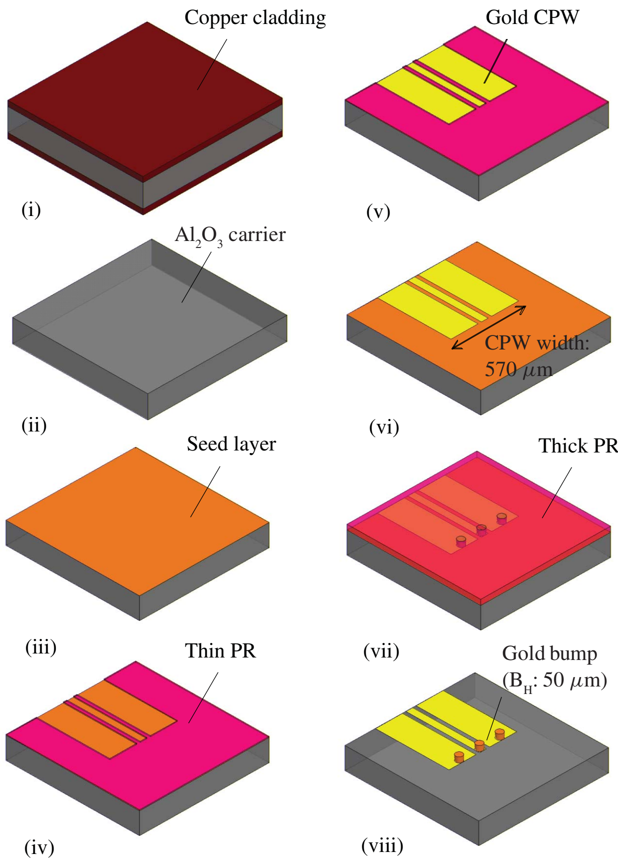
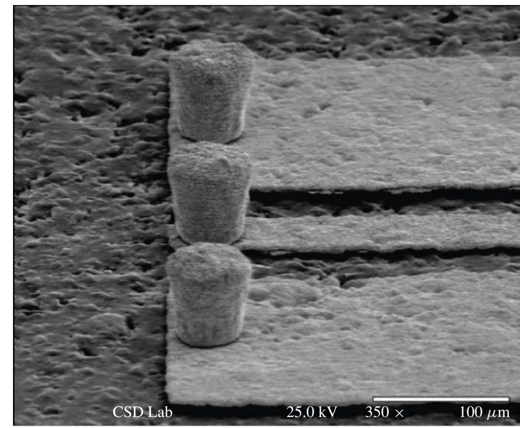
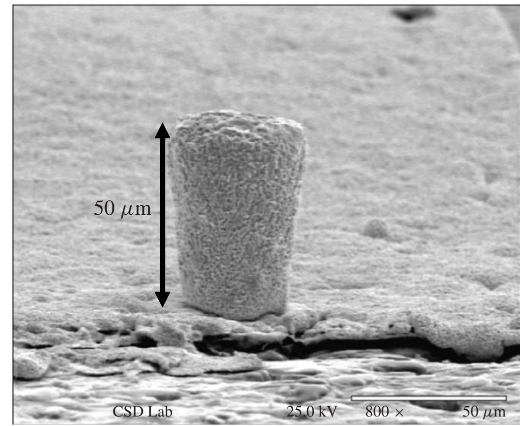


Fig. 3. Process flow of the RO3210 board for flip-chip assembly.



(a)



(b)

Fig. 4. SEM images of the fabricated Au bumps on RO3210 laminate. (a) Au bumps and CPW circuits on RO3210 board. (b) Zoom-in view of an Au bump.

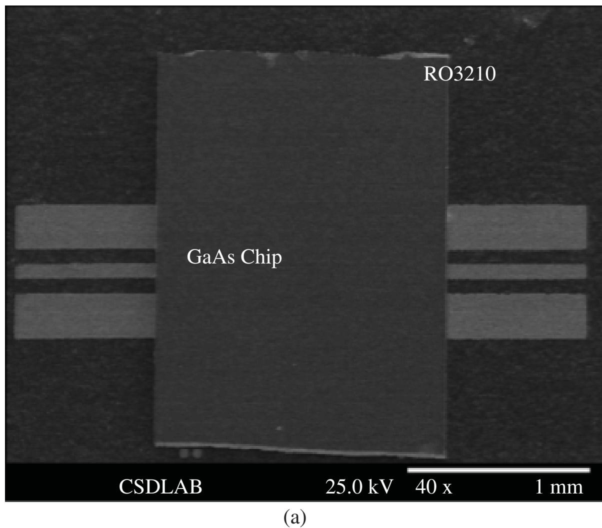
E-gun evaporator onto the RO3210 board with the thickness of 1000 and 2000 Å to form a continuous seed layer for the following Au electroplating. Ti was used as an adhesion layer. A thin photoresist (PR) layer was then patterned on the board for electroplating the CPW circuits. After the electroplating of the Au circuits, the thin PR film was removed. The board was then covered by a thick PR layer patterned to define the positions of the Au bumps, which were formed by electroplating. By controlling the electroplating current density and time, the required bump height was achieved. The Au bump height and diameter in this paper were both around 50 μm. The seed layers were then removed with a KI/I_2 solution for the removal of Au metal, and a dilute hydrogen fluoride solution for the removal of Ti metal. Fig. 4 shows the scanning electron microscopy (SEM) image of the fabricated CPW line with Au bumps on the RO3210 board.

Finally, the Au-to-Au thermocompression bonding was carried out to flip-chip-bond the passive CPW transmission line and active mHEMT device onto the RO3210 board using a precision flip-chip die bonder. After the optimization of the bonding parameters, the temperature of this paper holder was set to 250 °C and the bonding force was adjusted to 20 grams per bump which was maintained for a bonding time of 3 min. Fig. 5 shows the SEM image of the fabricated flip-chip interconnect structure on an RO3210 board. By using the FCOB packaging process, since the chip is directly flip-chip-mounted onto PCB, the ceramic package can be skipped, which results in lower cost and better RF performance.

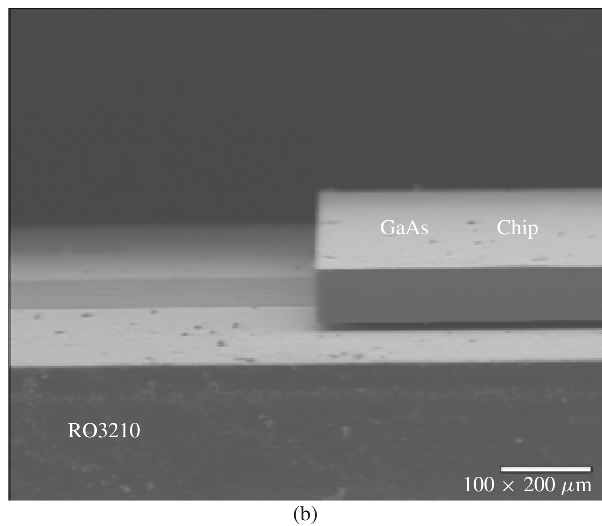
On comparing with the conventional flip-chip carrier on a ceramic-based substrate, the bumping process on RO3210 is almost the same except that the copper cladding needs to be removed in the beginning. Moreover, regarding the flip-chip assembly, the bonding temperature for RO3210 is lower than that of ceramic substrate since the glass transition temperature (T_g) of the organic laminate is around 300 °C. These issues should be carefully considered during carrier fabrication and the assembly process.

IV. Passive Structures

The scattering parameters (S parameters) of the fabricated interconnect structures were characterized to 50 GHz using an on-wafer probing measurement system with a vector network analyzer. The design and optimization of the interconnect structures were carried out by using the simulation tool high-frequency simulation software (HFSS) for the 3-D electromagnetic field analysis. In order to investigate the RF performance on the RO3210 board, a CPW thru line with characteristic impedance of $Z_0 = 50\ \Omega$ was fabricated on the RO3210 board. At the same time, an Al_2O_3 substrate was used for comparison with the same CPW thru-line design ($Z_0 = 50\ \Omega$). The CPW length for both cases was 3000 μm. Finite-ground coplanar waveguide (FGCPW) was employed on the substrates



(a)



(b)

Fig. 5. SEM images of the GaAs chip with flip-chip interconnect structure on RO3210TM board. (a) Top-view. (b) Side-view.

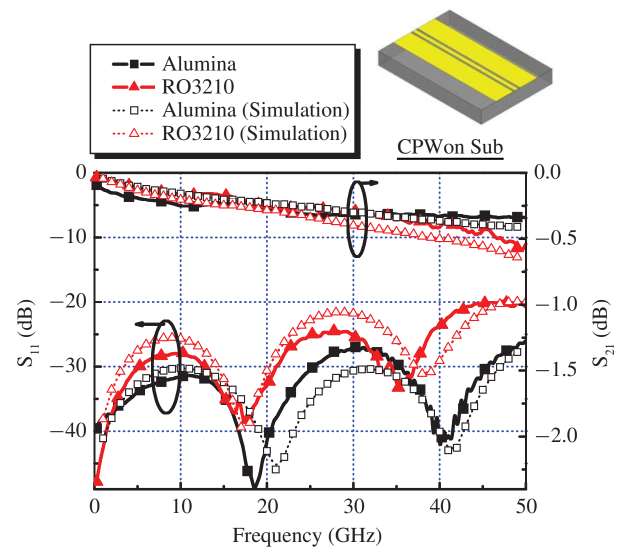


Fig. 6. Measured and simulated S-parameters of the CPW thru line on RO3210 and Al_2O_3.

to suppress the parallel-plate and higher-order modes [15]. Fig. 6 shows the measured and simulated results. As can be seen, a return loss of greater than 20 dB was achieved for both substrates because of the good matching of the 50-Ω impedance. On the other hand, the insertion losses on both substrates suffered the same degree of degradation, i.e., less than 0.4 dB from dc to 40 GHz. After 40 GHz, RO3210 showed poorer performance than Al_2O_3 with an additional loss of 0.3 dB at 50 GHz. The poorer performance of the former can be explained by its material properties: higher loss tangent (0.0027) compared to Al_2O_3 (0.0002). In addition, the surface roughness of RO3210 is greater than that of Al_2O_3(see Fig. 7), which results in a greater insertion loss, especially at higher frequencies. Fig. 7 shows the comparison of the surface roughness of the CPW transmission lines on the Al_2O_3 substrate and the RO3210 laminate.

The GaAs chip patterned with 50-Ω CPW transmission lines was flip-chip-bonded onto the RO3210 board. The total length of the back-to-back interconnect structure was 3000 μm, including 1000 μm on the chip and 2000 μm on the board. Fig. 8 shows both the measured and simulated S-parameters results. As can be seen, the measured return loss was greater than 15 dB from dc to 50 GHz, and the measured insertion loss was about 1.2 dB at 50 GHz. The poor performance is caused by the bump transitions at the flip-chip structures. For a flip-chip interconnect with typical dimensions, the equivalent circuit model shows an overall capacitive property [16], which could degenerate the transition performance. It is suggested that the bump pad be kept as small as possible to reduce the capacitance at the transitions [2], [3], however, it increases the difficulty in the fabrication. The most effective way to improve the interconnect performance is by adopting a high-impedance compensation line in front of the vertical bump transition. The high-impedance line provides an inductive counterpart to compensate for the excessive capacitance at the transition [3], [4]. In this paper, the dimensions of the high-impedance line were 100 μm in length and 30 μm in width (see Fig. 8). As can be seen, the return loss significantly improved after the compensation. From dc to 20 GHz, S_{11} is better than 18 dB, from 20 to 50 GHz, S_{11} is better than 20 dB. The insertion loss is within 0.5 dB from dc to 50 GHz, showing excellent broadband performance for commercial RF applications.

V. Active Discrete mHEMT Device

The in-house-fabricated $In_{0.52}Al_{0.48}As/In_{0.6}Ga_{0.4}As$ mHEMTs were flip-chip-assembled onto a RO3210 laminate with the same compensation design adopted in Section IV. Fig. 9 shows the device structure and the photographs of the mHEMT chip before and after the flip-chip assembly. The gate length of the device was 0.15 μm and the total gate width was 4×40 μm. Fig. 10 shows the measured transconductance (G_m) of the mHEMT device. The transconductance of the mHEMT after flip-chip bonding remained at the same level and shifted to more positive gate bias compared to the bare die. After the flip-chip bonding process, a compressive stress in the assembly was induced due to the coefficient of thermal

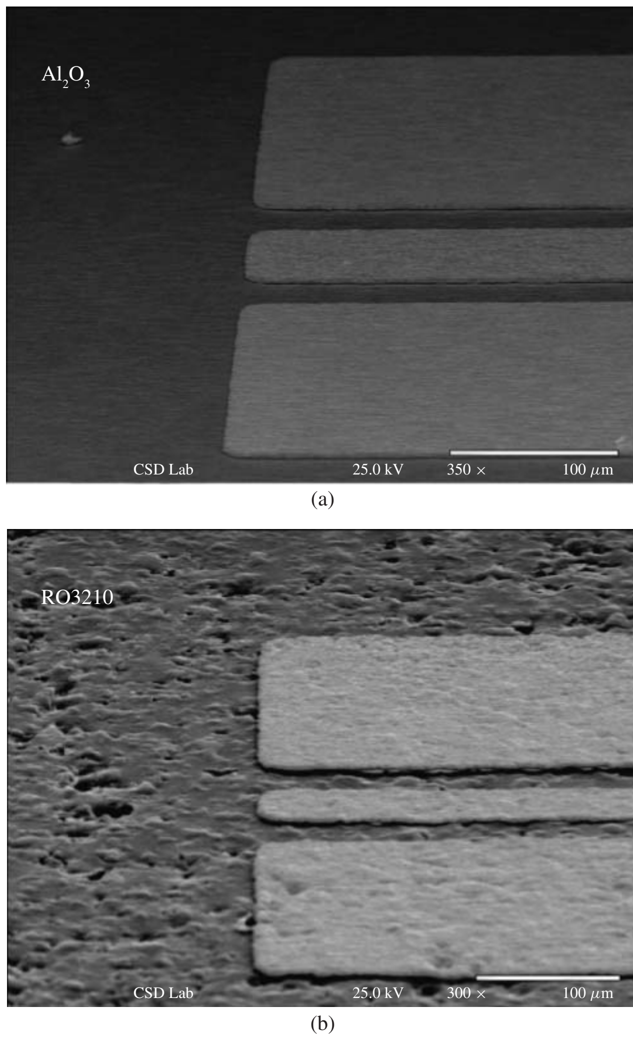


Fig. 7. SEM images of the surface morphologies of the CPW transmission lines on (a) Al_2O_3 and (b) RO3210 laminate.

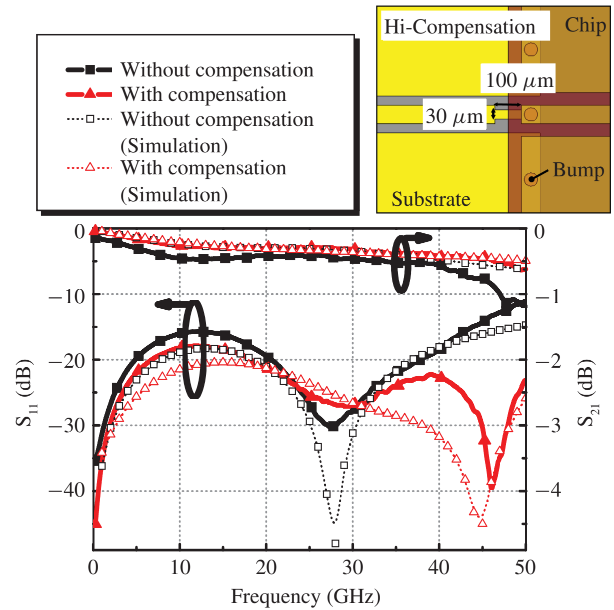


Fig. 8. Measured and simulated S-parameters of the flip-chip interconnect structure on RO3210 board with and without compensation.

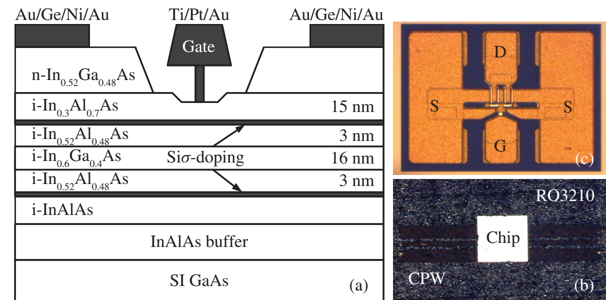


Fig. 9. (a) mHEMT device epitaxial layer structure (cross-sectional view). (b) Photograph of the chip before flip-chip assembly (top-view). (c) Photograph of the chip after flip-chip assembly (top-view).

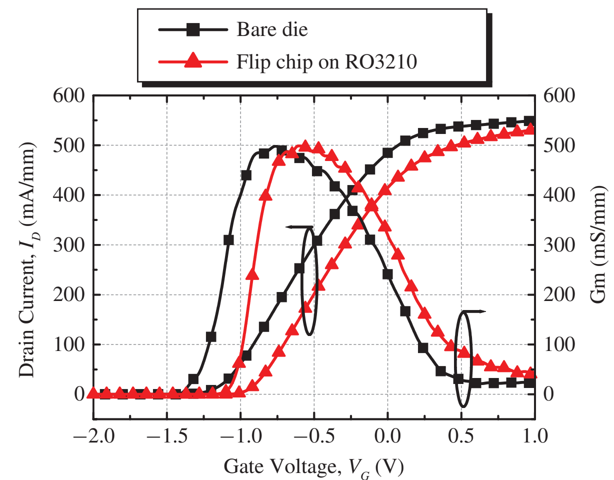


Fig. 10. Measured transconductance (Gm) of the bare and flip-chip packaged mHEMT on RO3210 laminate $V_D = 0.6$ V).

expansion (CTE) mismatch between GaAs (5.7 ppm/°C) and RO3210 (13 ppm/°C). This excessive compressive stress could lead to performance deviation [17], which should be carefully avoided during the assembly.

Figs. 11 and 12 show the measured S-parameters results of the flipped mHEMT on Al_2O_3 and RO3210, respectively. The S parameters were measured under the same bias condition of gate voltage $V_G = -0.15$ V and drain voltage $V_D = 0.6$ V. As can be seen, the extra loss in gain is smaller on Al_2O_3 (< 1.5 dB at 40 GHz) compared to RO3210 (< 2.0 dB at 40 GHz). The losses were due not only to the flip-chip transitions, but also to the long CPW transmission line on the substrates (Al_2O_3 and RO3210). (The total length of the transmission line on the substrate was 2000 μm.) Since RO3210 has higher loss tangent (0.0027) than Al_2O_3 (0.0002), the gain degradation of RO3210 is slightly higher.

VI. Underfill Injection and Reliability Test

Reliability investigation is always essential for commercial applications. For the FCOB structure, there is a large CTE mismatch between GaAs (5.7 ppm/°C) and RO3210 (13 ppm/°C), which is detrimental to the package reliability. The interconnects could fail because of the thermal stress induced during temperature cycling. Besides, the adhesion of

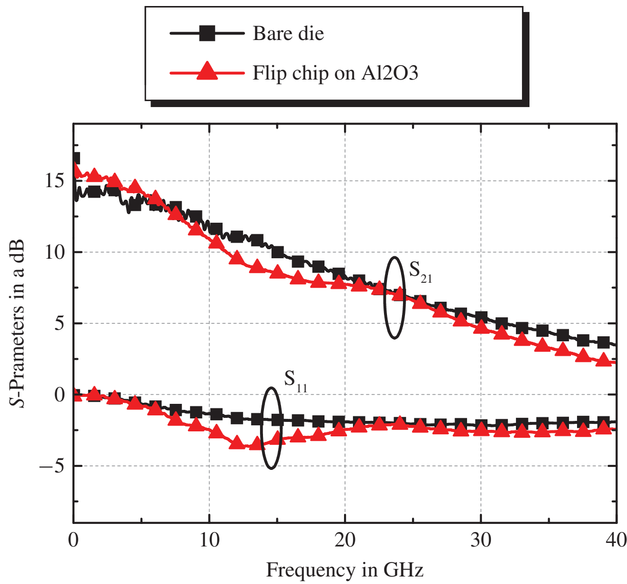


Fig. 11. Measured S-parameter results of the bare and flip-chip packaged mHEMT on Al_2O_3 substrate ($V_G = -0.15$ V, $V_D = 0.6$ V).

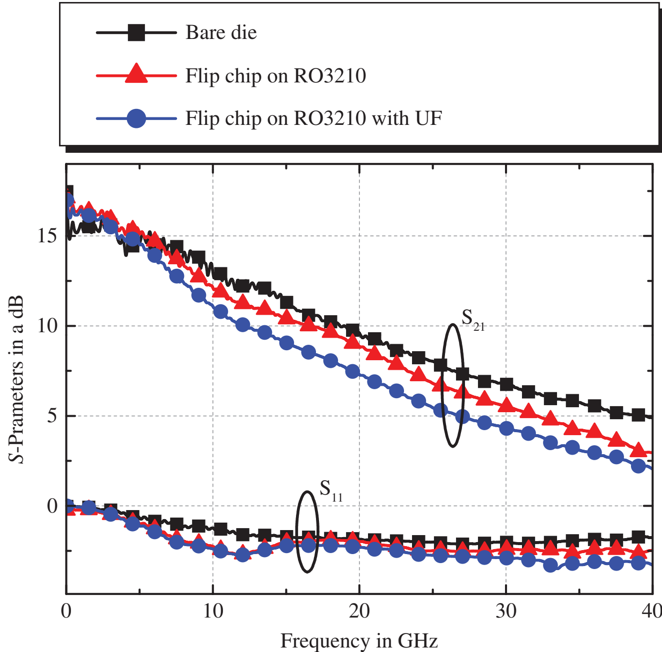


Fig. 12. Measured S-parameter results of the bare, flip-chip packaged mHEMT, and flip-chip packaged mHEMT with underfill on RO3210 laminate ($V_G = -0.15$ V, $V_D = 0.6$ V).

the flip-chip is weak since it relies only on several bump connections, which is sensitive and fragile to mechanical vibrations. Thus, to enhance the mechanical reliability, using an underfill in the flip-chip interconnect is necessary [18]. In this paper, an epoxy-based underfill with dielectric constant $\varepsilon_r = 3.5$ and loss tangent tan $\delta = 0.02$ at 10 MHz was injected into the flip-chip assemblies by the capillary underfill process and then cured at 150 °C for 2 h. The reliability of the flip-chip assemblies on RO3210 board with and without underfill was tested using the thermal cycling test. Fig. 13 shows the temperature profile of the thermal cycling test used

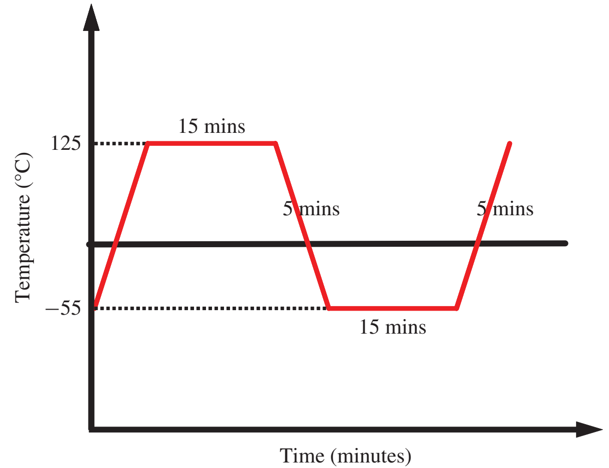


Fig. 13. Temperature profile of the thermal cycling test (Specification of JEDEC standard).

TABLE II
THERMAL CYCLING TEST RESULTS

FCOB without underfill				
	0 cycle	200 cycles	400 cycles	600 cycles
Resistance (Ω)	2.07	2.77	1.88	-
Failure	0/3	0/3	2/3	3/3
FCOB with underfill				
	0 cycle	200 cycles	400 cycles	600 cycles
Resistance (Ω)	1.97	2.44	1.99	2.55
Failure	0/3	0/3	0/3	0/3

in this paper (per JEDEC standard). The temperature range of the test was −55 to 125 °C with a 15-min dwell time. Table II shows the test results. Three samples with underfill and three samples without underfill were tested. For the flip-chip assemblies without underfill, two samples failed as the temperature cycling reached 400 cycles. All three samples without underfill failed after 600 cycles. The GaAs chips peeled off from the substrate bonding. The attachment of the chip to the substrate became weak as fatigue failure occurred at the bump–transition interface. For the flip-chip assemblies with underfill, as temperature cycling reached 600 cycles, no failure was observed. This is because the underfill redistributed the excessive stress and provided mechanical stability to the flip-chip structures.

However, the injection of the underfill could compromise the performance of the packaged devices [18]. As the epoxy-based underfill is filled in the flip-chip assemblies, an additional loss arises because of the higher loss tangent of the epoxy (tan $\delta = 0.007 \sim 0.02$) compared to its value in air (tan $\delta \sim 0$). As can be seen in Fig. 12, from dc to 40 GHz, an average additional loss of 1 dB was induced as a result of the introduction of the underfill.

VII. CONCLUSION

The design, fabrication, and reliability of an FCOB package on a Rogers RO3210 laminate were studied up to 50 GHz. The Au CPW transmission line ($W = 70$ μm and $G = 40$ μm) and pillar bump (diameter $= 50$ μm) were successfully fabricated

on a high-*k* RO3210 laminate with photolithography and electroplating processes. The Au-to-Au thermal compression method was performed to flip-chip-bond the passive CPW transmission line and active discrete mHEMTs onto the RO3210 board. The passive flip-chip on RO3210 showed excellent performance up to 50 GHz, with a return loss S_{11} larger than 18 dB and insertion loss S_{21} within 0.5 dB. The electrical performance of the flip-chip-assembled in-house-fabricated mHEMT on RO3210 exhibited only a small gain degradation (less than 1.0 dB) from dc to 40 GHz, showing the potential of implementing MICs on the RO3210 board. Moreover, an underfill was applied to enhance the mechanical reliability of the packaged device on RO3210, resulting in an additional loss of 1 dB from dc to 40 GHz. Thermal cycling tests were performed to test the interconnect reliability, and the results indicated that the samples with underfill passed the thermal cycling test up to 600 cycles. These results demonstrate the feasibility of using FCOB packaging technology on RO3210 laminates for commercial applications up to 50 GHz. To the best of our knowledge, this is the first study that evaluated the use of RO3210 laminate for microwave flip-chip in the open literature.

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