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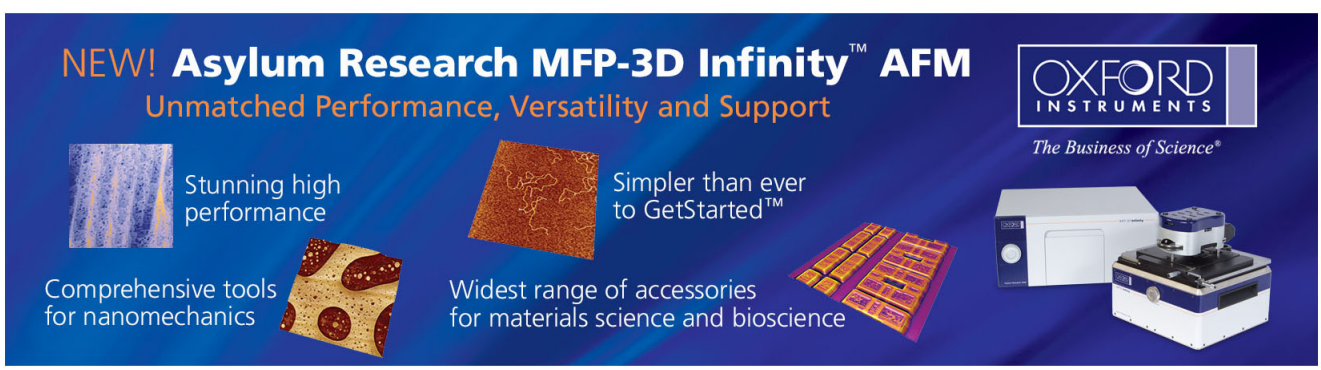

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Gate-all-around polycrystalline-silicon thin-film transistors with self-aligned grain-growth nanowire channels

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In this letter, gate-all-around (GAA) polycrystalline silicon thin-film transistors (TFTs) with self-aligned grain-growth channels were fabricated using excimer laser crystallization (ELC) on a recessed-nanowire (RN) structure. Via the RN structure constructed by a simple sidewall-spacer formation, location-controlled nucleation and volume-confined lateral grain growth within the RN body during ELC process have been demonstrated with only one perpendicular grain boundary in each nanowire channel. Because of the high-crystallinity channel together with GAA operation mode, the proposed GAA-RN TFTs show good device integrity of lower threshold voltage, steeper subthreshold slope, and higher field-effect mobility as compared with the conventional planar counterparts. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.3691184]

Low-temperature polycrystalline silicon thin-film transistors (TFTs) have been widely used as pixel-switching elements in active-matrix display panels. Their further evolution aims at enlargement of the matrix/circuit scale, and system integration into the panel, which demands the enhancement of the TFTs' electrical performance and geometric scalability. To meet these requirements, several attempts on modifying the device structures and process techniques have been made.[1–3] Nanowire-based polycrystalline silicon TFTs with gate-all-around (GAA) or multiple-gate structures have recently been reported to enhance gate controllability, thus suppressing effectively the short channel effects for geometry scaling.[4–7] However, most of them were prepared by solid-phase crystallization, which resulted in numerous intra- and inter-grain defects in device channels, thus causing poor field-effect mobility. Excimer laser crystallization (ELC) has become a promising method for its great potential in processing high-quality silicon grains without causing damage to glass substrates. Moreover, several modified ELC techniques for controlling the grain size and grain-boundary location of polycrystalline silicon thin films have been developed to improve electrical performance. These techniques included sequential lateral solidification,[8] the grain filter method,[9] additional reflective or antireflective capping layer,[10] phase-modulated ELC,[11] dual-beam excimer laser annealing,[12] double-pulsed laser annealing,[13] selectively floating a-Si active layer,[14] selectively enlarging laser crystallization,[15] and so on. However, there is a relatively little research on ELC of nanowire-type amorphous Si. In this letter, we adopted a recessed-nanowire (RN) structure for self-aligned control of the solidification direction in the device channel region of GAA TFTs during excimer laser irradiation.

The key steps involved in processing of RN polycrystalline silicon TFTs are schematically shown in Fig. 1. A 50-nm-thick Si_3N_4 (as etch-stop layer) and a 200-nm-thick tetra-ethyl-ortho-silicate (TEOS) SiO_2 (as sacrificial layer) films were sequentially deposited by low-pressure chemical vapor deposition (LPCVD) systems. Several strips with step height of 100-nm were patterned on the surface of the sacrificial SiO_2 layer by reactive ion etching (RIE), as shown in Fig. 1(a). After conformal deposition of a 100-nm-thick a-Si layer, g-line lithography was used to pattern photoresist (PR) to define the source/drain (S/D) pads, which overlapped on the two edges of those patterned SiO_2 strips. Subsequently, RIE was employed to remove the a-Si. The a-Si nanowire channels were patterned self-aligned to the sidewall of the SiO_2 strips by simply sidewall spacer formation between the S/D pads, as shown in Fig. 1(b). After the PR removal [Fig. 1(c)], a 100-nm-thick SiO_2 layer was capped to prevent the pattern shrinkage when a-Si nanowires were crystallized by KrF ($\lambda = 248$ nm) excimer laser irradiation with 320 mJ/cm^2 at room temperature.[16] Figure 1(d) shows its corresponding cross-sectional illustration along the AA′ direction of Fig. 1(c). Then, the suspending nanowires were constructed after both the capped SiO_2 and SiO_2-strips were etched away (down to the Si_3N_4 etch-stop layer) by a HF etchant. The 25-nm-thick TEOS SiO_2 and the 200-nm-thick phosphorous *in-situ* doped polycrystalline silicon were conformally deposited by the LPCVD system as the gate insulator and the gate electrode, respectively. After gate patterning, self-aligned phosphorous S/D implantation was performed at 30 keV to a dose of 5×10^{15} cm^{-2} and a 300-nm-thick passivation oxide layer was deposited, followed by S/D activation. Finally, contact opening formation and metallization were carried out to complete device fabrication without any further hydrogen plasma passivation. For comparison, the conventional planar (CP) excimer-laser polycrystalline silicon TFTs were fabricated by the same process sequence.

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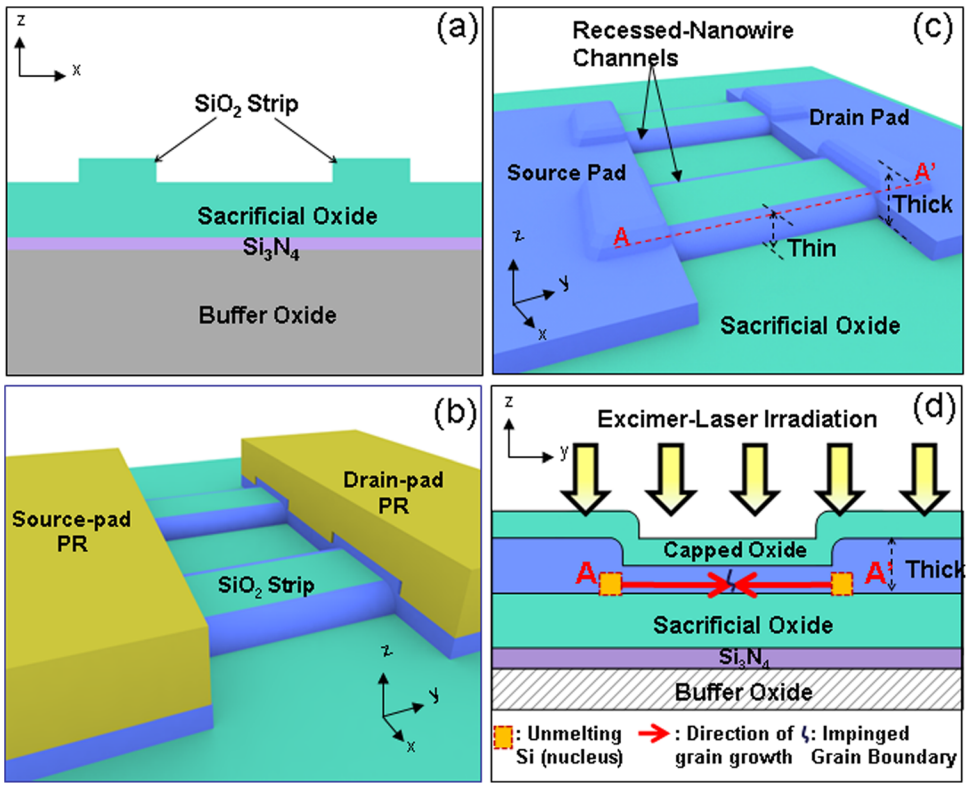

FIG. 1. (Color online) Schematic diagrams of the key fabrication steps for GAA-RN TFTs: (a) the formation of SiO_2 strips, (b) and (c) the formation of a-Si deposition, nanowires, and S/D pads, and (d) the cross-sectional illustration of the capped-oxide deposition and excimer-laser crystallization along AA′ direction of (c).

In the super lateral growth (SLG) model, the un-melted islands act as solidification seeds, from which a lateral grain growth commences.[17–19] According to the SLG model, a lateral temperature gradient is created between the thin and thick regions, and un-melted solid Si particles act as the seeds for lateral crystallization. If the thick region of the a-Si film is thick enough, it will be partially melted, and a lot of un-melted solid seeds will remain near the step boundary. As a result, a lateral temperature gradient is produced between the local thin and thick regions of the a-Si film, and grains will grow laterally from the un-melted solid seeds towards the completely melted region. In the proposed RN structure, as shown in Fig. 1(d), the a-Si region in the nanowire channel is thinner than that of the oxide strip sidewall of the S/D pad adjacent to the nanowire. Thus, with complete melting in the a-Si nanowire body and partial melting at the oxide-strip sidewall a-Si of the S/D pad, a lateral temperature gradient will exist between the completely melted liquid-phase region and un-melted solid-phase seeds (marked, respectively, by A and A′ in Fig. 1(d)). Thus, via the RN structure, location-controlled nucleation and volume-confined lateral grain growth within the RN body during the ELC process can proceed. Figures 2(a) and 2(b) show the corresponding SEM micrographs of excimer laser-crystallized RN structure with the laser energy density of 320 mJ/cm^2 before and after Secco etching, respectively. The grain boundary in the RN nanowire can be clearly seen after Secco etching treatment. Because of the collision between the solidification fronts of the two S/D pads, there is only one perpendicular grain boundary existed in the middle of each RN channel. Notably, owing to the nanometer-sized volume of nanowire, only one nucleus at each border between the S/D-pad and the nanowire region (marked, respectively, by A and A′ in Fig. 1(d)) can survive as the seed crystal and then grows laterally towards the volume-confined completely melted nanowire region, which accounts for the absence of parallel grain boundary in the RN channel. Figure 3 shows the cross-sectional transmission electron microscopy image of the fabricated GAA TFT with resulting excimer-laser crystallized RN channels. As can be

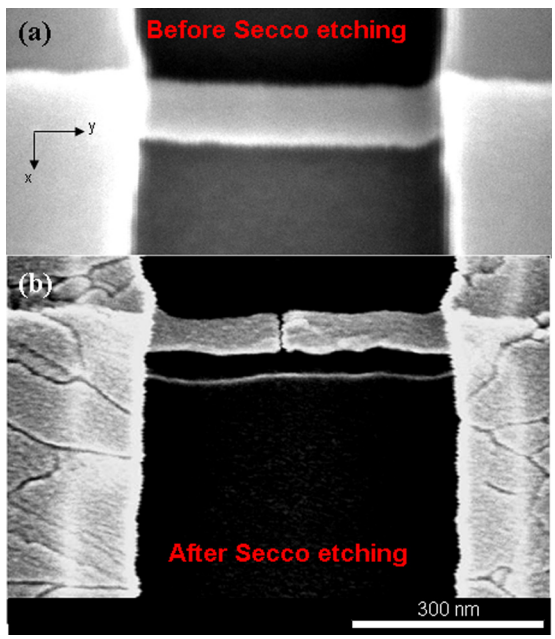

FIG. 2. (Color online) SEM images of recessed nanowire with excimer laser crystallization (a) before and (b) after Secco-etching treatment.

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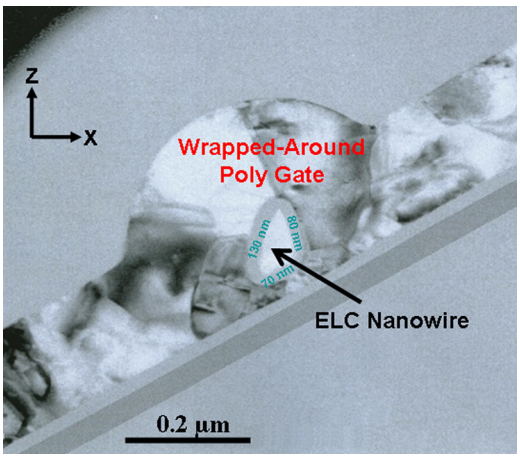

FIG. 3. (Color online) Cross-sectional transmission electron microscopy image of the fabricated GAA-RN TFTs.

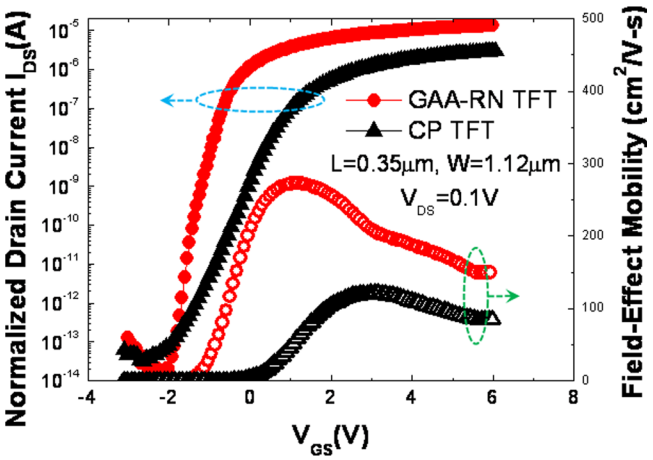

FIG. 4. (Color online) Transfer characteristics of GAA-RN and CP TFTs.

seen, there is good step-coverage on the GAA structure both for the TEOS gate oxide and phosphorous *in-situ* doped polycrystalline silicon gate. The vertical sidewall thickness, the horizontal width, and the bevel length of each NW channel are about 80, 70, 130 nm, respectively. Thus, the total surrounding width of each nanowire channel is 280 nm. Transfer characteristics of GAA-RN and CP TFTs are compared in Fig. 4. These devices have a gate length (L) of 0.35 μm and a channel width (W) of 1.12 μm, where the W of GAA-RN TFTs is defined by four nanowires with a two-dummy-strip structure. The normalized drain current was defined as (measured I_{DS}) $\times \frac{L}{W}$. The threshold voltage (V_{th}) was defined as the gate voltage required to obtain a normalized drain-current of 1×10^{-8} A at $V_{DS} = 0.1$ V. The subthreshold swing (SS) was extracted at $V_{DS} = 0.1$ V. The field-effect mobility was extracted from the peak linear transconductance at $V_{DS} = 0.1$ V. For the GAA-RN devices, the linear region approaching $V_{DS} = 0$ V of output characteristics performs good ohmic performance, which confirms there is no non-ideal contact effect due to the nanowire to thick S/D contacts. Owing to high-quality Si channel and GAA operation mode, the proposed GAA-RN TFTs exhibit better electrical characteristics than the conventional ones. In comparison, the mobility increases from 121 to 273 cm^2/Vs, the V_{th} decreases from 0.4 to −0.94 V, and the SS decreases from 374 to 142 mV/decade.

In summary, via the proposed RN structure formed by a simple sidewall-spacer formation, volume-confined lateral grain growth within nanowire body during ELC has been demonstrated to form an only one perpendicular grain boundary in each Si nanowire channel. Owing to high-quality silicon channel and GAA operation mode, the proposed GAA-RN TFTs reveal high-performance characteristics as compared with the conventional planar ones.

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