# A Battery-Free 217 nW Static Control Power Buck Converter for Wireless RF Energy Harvesting With $\alpha$-Calibrated Dynamic On/Off Time and Adaptive Phase Lead Control

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***Abstract*—A battery-free nano-power buck converter with a proposed dynamic on/off time (DOOT) control can achieve high conversion efficiency over a wide load range. The DOOT control can predict the on/off time at different input voltages without a power consuming zero current detection (ZCD) circuit, as well as suppress static power in idle periods. To adapt to the fluctuations in a harvesting system, the proposed $\alpha$-calibration scheme guarantees accurate ZCD over process, voltage variation, and temperature (PVT) in the DOOT to improve power conversion efficiency. Furthermore, the adaptive phase lead (APL) mechanism can improve inherent propagation delay attributable to low-power and non-ideal comparator, thus improving load regulation by a maximum of 30 mV. The test chip was implemented in 0.25-$\mu$m CMOS process with a die area of 0.39 mm$^2$. Experimental results showed 95% peak efficiency, low static power of 217 nW and good load regulation of 0.1 mV/mA, which are suitable for RF energy harvesting applications.**

***Index Terms*—Adaptive phase lead (APL), battery-free, buck converter, dynamic on/off time (DOOT), energy harvesting, low power, radio frequency (RF), zero current detection (ZCD).**

## I. Introduction

RAPID advances in integrated circuit technology have resulted in the miniaturization of medical monitoring instruments in portable devices for healthcare applications. Specifically, sensor networks have become a hot topic for the processing of the medical signals in silicon systems. For example, a bio-medical sensor network is claimed to be capable of automatic monitoring, recording, reporting, and alarming functions. Sustainable silicon systems can be used for many purposes, such as in research on physiological signals, monitoring of patients, remote home care, and so on.

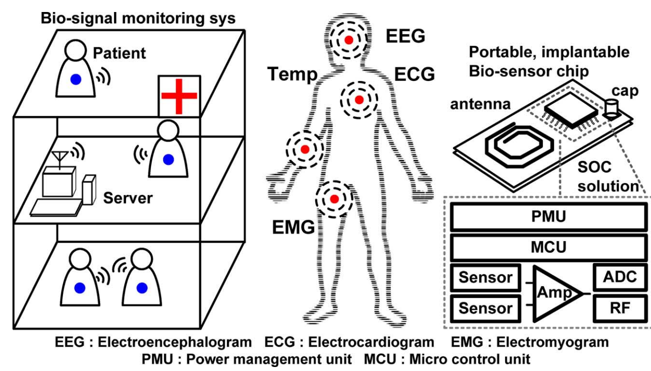


Fig. 1. Wireless bio-sensor network.

As illustrated in Fig. 1, each patient wears several sensor nodes responsible for specific physiological signals in several small monitoring systems. Through wireless communication, the central health server can collect the sensed data. Each sensor node works as a micro system that has to be sustained for a long time because of the inconvenience of changing the battery. Thus, a power system should be carefully designed to have long battery-life or to utilize battery-free silicon systems for sustainability.

Traditionally, battery supplied power is a common choice for such wireless sensor nodes. An ultra-low power-sustained system with the power scale of approximately several microwatts is now possible because of advanced silicon technology. Previous studies have demonstrated the excellent performance of low-power circuit designs in the field of bio-medical applications, as reported by [1], [2], and [3]. An energy harvesting self-powered or self-rechargeable power supply has become more and more important in the present research trends on battery-free operation because of the low-power characteristic of biomedical applications. The use of a self-powered biomedical and wireless sensor system is an emerging method to save energy and consequently extend the standby period. Without any battery exchange, the primary cost for the preservation of sensor nodes can be reduced, and the system life cycle can be further extended.

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A large number of battery-free power sources are available, including vibration, thermoelectric generators, solar cells, electromagnets, and piezoelectric conversion. Ambient radio frequency (RF) power signals from cellular-phones and access points (AP) can be used to harvest environmental energy [4]. The RF energy transfer technique can be roughly classified as either a near or far field transmission. Near field transmission is the inductive coupling between two transmission coils, which can be applied in a short range to produce a relatively large amount of power up to several milliwatts. On the other hand, far field transmission utilizes an antenna as a receiver to collect microwaves in certain frequencies and then converts the collected signal into energy. The energy density of microwaves degrades in terms of exponential shape with distance, so the collected power available for back end usage is very limited. The RF powering scheme has the advantage of being a long distance power supply and also enables ambient energy recycling in a far field application [5]. To satisfy both the near and far field transfer schemes, the converter should be capable of operating over a wide load range (i.e., 1 $\mu$W to tens of mW) with high efficiency.

In recycling ambient power or extremely low RF power (i.e., 0.1 to 200 $\mu$W), a DC/DC converter requires: 1) a nano-watt controller to prevent the harvesting system from dissipating a large amount of power; 2) fast transient response to overcome peak power in data transmission; and 3) better load regulation to guarantee the correct operation of sensors and analog front-end circuits. Previous studies on DC/DC converters were well-designed for different energy harvesting sources such as, thermoelectric, RF and vibration. However, the different structure designs consumed several microwatts [6], [7]. The design of the charge pump has the power efficiency lower than that of the switching converter [6]. Some of the switching regulator structures require external reference voltage and biasing current [7]. Because the input voltage may vary in a wide range (as 1.2$\sim$2.5 V) so to mitigate efficiency constraints, the switching regulator architecture is selected instead of a linear regulator owing to large energy loss on the dropout voltage [8], [9]. The design of the charge pump, which has power efficiency lower than that of the switching converter [6], requires an external reference voltage and biasing current [7]. The resistor emulation boost topology may not be sufficiently energy efficient in ultra low power conditions [10]. Therefore, the variable pulse width generator implemented by the analog-to-digital converter (ADC) [11] and the digital calibration [7] are inappropriate for reducing power consumption.

In this paper, a low power DC/DC switching converter suitable for RF power applications is proposed with a nano-watt control. A ripple-control method is adopted to obtain fast response and energy efficient characteristics [12], [13]. However, in conventional ripple-control methods [14], the constant on-time technique requires a power consuming zero current detection (ZCD) circuit to determine a correct off-time. Generally, for rapid switching at an accurate zero current, the ZCD mechanism requires a power-consuming comparator. In contrast, the constant off-time technique is a power consuming method at light loads and is unsuitable for harvesting systems. To eliminate the use of a power-consuming ZCD circuit and to operate in an energy efficient discontinuous conduction mode (DCM) control, the low-power dynamic on/off time (DOOT) control along with a digital $\alpha$-calibration method, is proposed. Furthermore, with the adaptive phase lead (APL) control, the delay of low-power analog circuits can be compensated to enhance load regulation performance.

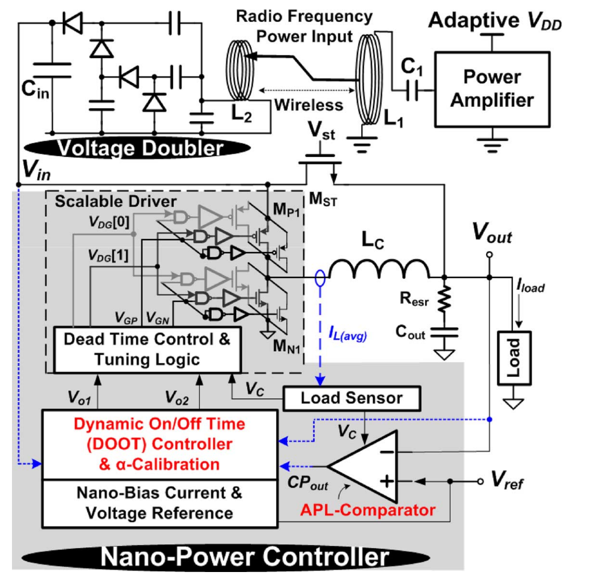



Fig. 2. Wireless RF power input and the function block of nano-power converter.

This paper is organized as follows. The structure of an energy harvesting circuit is depicted in Section II. Section III illustrates the proposed DOOT control and the $\alpha$-calibration scheme. The low-power bias and voltage reference circuit and the APL comparator are described in Section IV. Experimental results are shown in Section V. Finally, a conclusion is drawn in Section VI.

## II. Structure of Energy Harvesting Circuit

To meet the requirements of a harvesting system, the nano-power converter is designed to contain a low-power DC/DC converter with DOOT control and an APL comparator for good load regulation and energy efficiency. The schematic diagram of the entire system is illustrated in Fig. 2. The coupling inductor or antenna followed by a voltage doubler receives external RF power from the power amplifier to charge capacitor $C_{\rm in}$. A greater number of cascade levels of the voltage doubler can yield higher output voltage, but will result in lower efficiency. The buck converter transfers energy from $C_{\rm in}$ to the output capacitor $C_{\rm out}$ to drive the sequent system. For high performance operation, the driving voltage is regulated at 1 V, which is equal to the reference voltage. Without the feedback resistors, static power consumption can be effectively reduced. To achieve low power operation, the nano-bias current and voltage reference are utilized to generate bias current and reference voltage [15], [16].

A low bias current is known to result in slow response and propagation delay in analog circuits. It also deteriorates the quality of the power supply, thus reducing the operation performance of the sequent system. A conventional harvesting system therefore requires a post-regulator, such as a low-dropout (LDO) regulator, to ensure load regulation. However, an LDO regulator consumes a great deal of power and a large silicon area. In this paper, an APL-comparator is proposed to improve the response time and load regulation without increasing costs on power and silicon area. Basically, the APL-comparator obtains loading information from the load sensor and adaptively moves the compensation zero toward the origin to enhance load regulation. Simultaneously, power consumption can be minimized compared with conventional designs.

The proposed DOOT controller can generate the on-time and off-time periods to control the power metal-oxide semiconductor field-effect transistors (MOSFETs), $M_{P1}$ and $M_{N1}$. For higher efficiency, the DOOT converter designed in the DCM operation, which can dynamically adjust switching frequency according to load condition. As a result, large switching loss can be reduced for high conversion efficiency compared with fixed frequency pulse-width modulation (PWM) control at light loads. However, the power saving performance may be deteriorated by large losses dissipated at the body diode conduction of the power MOSFET attributable to the inaccurate zero current switching [17], [18]. In other words, a high-precision and fast-response comparator is required to rapidly switch off the power MOSFET when the inductor current reaches zero. The design methodology used for conventional converters is to increase the driving current of the comparator, but this method consumes large amount of power. Thus, a variable pulse width generator implemented by a low-power ADC [7] calibrated by a digital calibration circuit [6] is inappropriate for reducing power consumption. The proposed DOOT controller utilizes analog prediction to accomplish precise zero current switching at the power MOSFET. This controller can also minimize conduction loss caused by the inaccurate ZCD and eliminate the power consumption of fast comparators in conventional designs.

Furthermore, the performance of the proposed DOOT controller without a digital calibration circuit is deteriorated by the process, voltage variation, and temperature (PVT) effect. In the current study, the digital calibration circuit, named as the $\alpha$-calibration scheme, is introduced to calibrate the analog prediction parameter. Based to the $\alpha$-calibration results, the proposed DOOT controller can be free from the PVT effects even when the pre-defined values deviate from the ideal values. Moreover, the $\alpha$-calibration scheme will be shut-down to further decrease power consumption when the harvesting system is in normal operation.

Last, the shoot-through current caused by the drivers and the frequent switching of power MOSFETs may result in power losses. To ensure high conversion efficiency, non-overlapping and scalable drivers are used to drive the scalable power MOSFETs according to load information. Through scalable driving [19], conduction and switching losses can be minimized through different input and load ranges. The entire harvesting system is deliberately designed for power reduction and improving accuracy in each control module. Thus, the high efficiency and good load regulation of the harvesting system can be guaranteed.

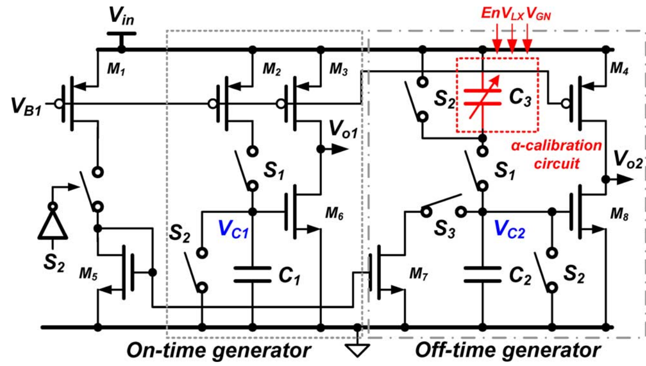



Fig. 3. Proposed DOOT circuit with the $\alpha$-calibration circuit.

## III. Proposed DOOT Control and Implementation

### A. Dynamic On/Off Time Implementation

The proposed DOOT control is based on a fundamental theory, which defines the charging slope $S_1$ and the discharging slope $S_2$ of an inductor current are related to the input voltage $V_{\rm in}$ and the output voltage $V_{\rm out}$ as illustrated in (1)

$$S_1 : S_2 = \frac{(V_{\rm in} - V_{\rm out})}{L} : \frac{V_{\rm out}}{L}. \tag{1}$$

In steady state, when a dynamic equilibrium is established, the power MOSFET $M_{N1}$ turns off precisely when the inductor current decreases toward zero. In other words, no extra loss is incurred during the discharge phase, thus minimize the switching loss. To eliminate the use of power-consuming ZCD circuit and to generate an accurate on/off time for zero current switching, the low-power DOOT circuit, as depicted in Fig. 3, is proposed. This circuit is composed of an on-time and an off-time generator. As expressed in (2), the on-time and the off-time values are designed to be proportional to $V_{\rm out}$ and $(V_{\rm in} - V_{\rm out})$, respectively, to achieve a balanced on/off time in steady state

$$\frac{(V_{\rm in} - V_{\rm out})}{L} \times t_{on} = \frac{V_{\rm out}}{L} \times t_{\rm off} \text{ in steady state.} \tag{2}$$

Here, conventional power-consuming comparator is removed to save power through the use of the comparison point set by the threshold voltage of two transistors $M_6$ and $M_8$. Moreover, the constant current mirrored to transistors $M_2$ and $M_7$ is used to charge and discharge the capacitors $C_1$ and $C_2$. The input voltage $V_{\rm in}$ is divided by the dividing capacitors $C_2$ and $C_3$ to ensure that the voltage $V_{C2}$ across the $C_2$ will be a ratio of the input voltage, as expressed in (3), where $\alpha$ is the ratio of $C_2$ to $C_3$

$$V_{C2} = \frac{\alpha}{1+\alpha} V_{\rm in} \text{ where } \alpha = \frac{C_2}{C_3}. \tag{3}$$

When the $V_{\rm out}$ is smaller than the $V_{\rm ref}$, the DOOT control starts the on-time period. Meanwhile, the power MOSFET $M_{P1}$ is turned on to increase the inductor current. During the on-time period, as depicted in Fig. 4(a), the switch $S_1$ is turned on to charge the $C_1$ and to determine the on-time as expressed in (4)

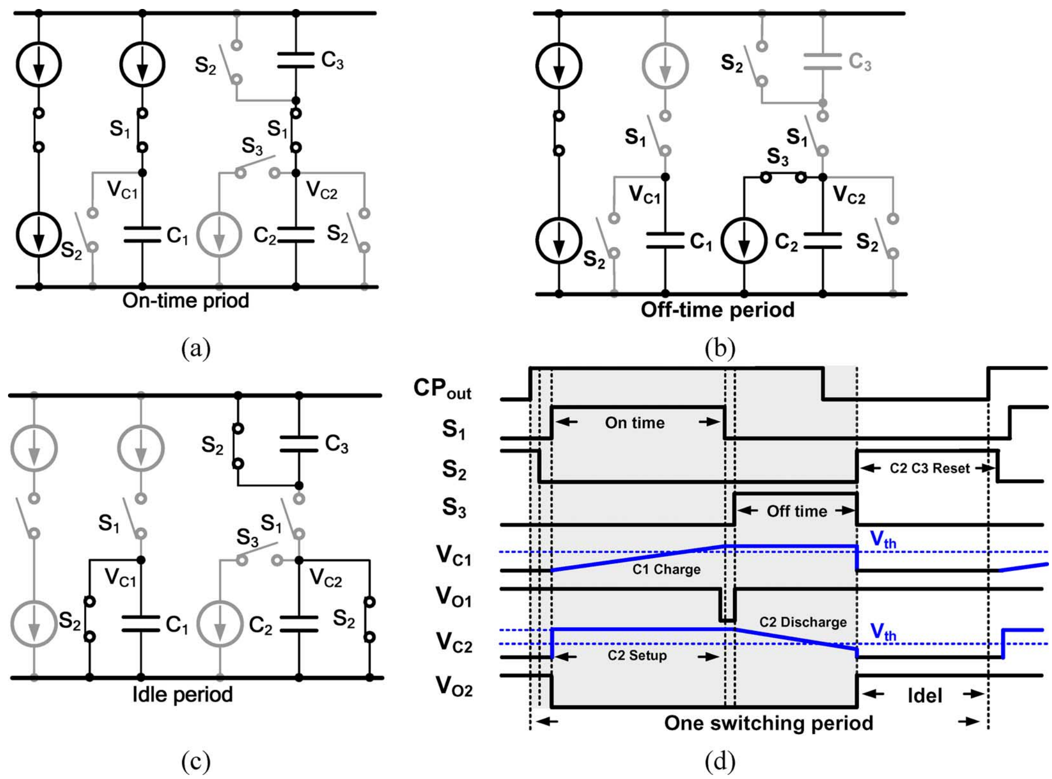



Fig. 4. Operation topologies in the DOOT controller. (a) The on-time period. (b) The off-time period. (c) The idle period. (d) The timing diagram of the DOOT controller.

where the charging current $I_c$ for the $C_1$ is decided by the current source $M_2$. Simultaneously, $V_{\rm in}$ information is sampled by the capacitors $C_2$ and $C_3$

$$T_{\rm ON} = \frac{V_{th({\rm M6})} \cdot C_1}{I_c}. \quad (4)$$

The on-time period $T_{\rm ON}$ is ended once $V_{C1}$ is higher than the threshold voltage $V_{th({\rm M6})}$ of the transistor $M_6$. Then, the output voltage $V_{o1}$ of the on-time generator is set to low to indicate the end of the on-time period. Through the non-overlapping driver, the power MOSFETs $M_{P1}$ and $M_{N1}$ are turned off and on, respectively.

Consequently, as illustrated in Fig. 4(b), the DOOT controller enters the off-time period controlled by the off-time generator. The power MOSFET $M_{N1}$ is turned on to decrease the inductor current. Owing to the sample of $V_{\rm in}$ during the on-time period, the charge on the capacitor $C_2$ is proportional to $V_{\rm in}$. After closing the switch $S_3$, the discharging current $I_c$ is decided by the current source $M_7$ and the off-time period can determined by (5)

$$T_{\rm off} = \frac{\left(\frac{\alpha}{1+\alpha} \cdot V_{\rm in} - V_{th({\rm M8})}\right) \cdot C_2}{I_c}. \quad (5)$$

Similarly, if the voltage $V_{C2}$ across $C_2$ is smaller than the threshold voltage $V_{th({\rm M8})}$ of the transistor $M_8$, the off-time period is stopped. Meanwhile, the signal $V_{o2}$ will be set to high subsequently turn off power MOSFET $M_{N1}$. Assuming the transistors $M_6$ and $M_8$ have the same threshold voltage. The relationship between the threshold voltage ($M_6$ or $M_8$) and the $V_{\rm out}$ can be scaled by a normalized factor. The normalized factor is selected to be the value of $(\alpha/1 + \alpha)$. As a result, the on-time expressed in (4) is proportional to $V_{\rm out}$ whereas the off-time shown in (5) is proportional to $(V_{\rm in} - V_{\rm out})$. According to the voltage-second balance principle [20], the relationship between the on-time and the off-time values can be derived as shown in (6), which is similar to the basic operation of buck converters

$$\frac{(V_{\rm in} - V_{\rm out})}{L} \times \frac{V_{th({\rm M6})} \cdot C_1}{I_c} = \frac{V_{\rm out}}{L} \times \frac{\left(\frac{\alpha}{1+\alpha} \cdot V_{\rm in} - V_{th({\rm M8})}\right) \cdot C_2}{I_c}. \quad (6)$$

For simplicity, $C_1$ and $C_2$ have the same value and are well matched by the centroid layout matching skill. The designed value of $V_{\rm out}$ is 1 V. Therefore, (6) can be simplified as (7)

$$(V_{\rm in} - 1) = \left(\frac{\alpha}{1+\alpha} \cdot \frac{V_{\rm in}}{V_{th({\rm M6,M8})}} - 1\right). \quad (7)$$

Obviously, when the value of $\alpha$ can be properly selected to satisfy (7), an energy balance between the on-time and off-time periods can be achieved. Consequently, the proposed DOOT controller can adjust the on-time period adaptively to decide upon the input voltage and to achieve the zero current switching mechanism by utilizing $V_{C2}$ across $C_2$. Furthermore, in Fig. 4(c), the DOOT controller is shut-down and then enters the idle period for greater power savings when $V_{\rm out}$ is higher than $V_{\rm ref}$. $V_{o1}$ and $V_{o2}$ are both set to low to fully turn off the

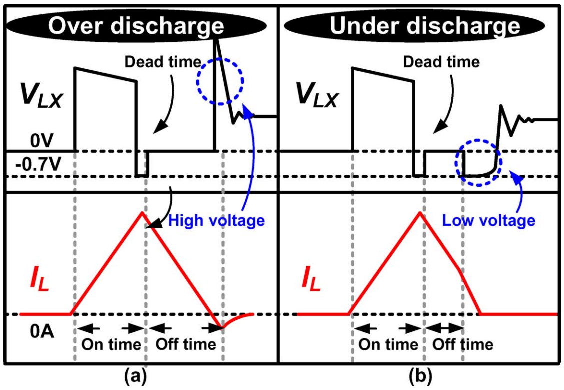



Fig. 5. ZCD operation. (a) A too long off-time status. (b) A too short off-time status.

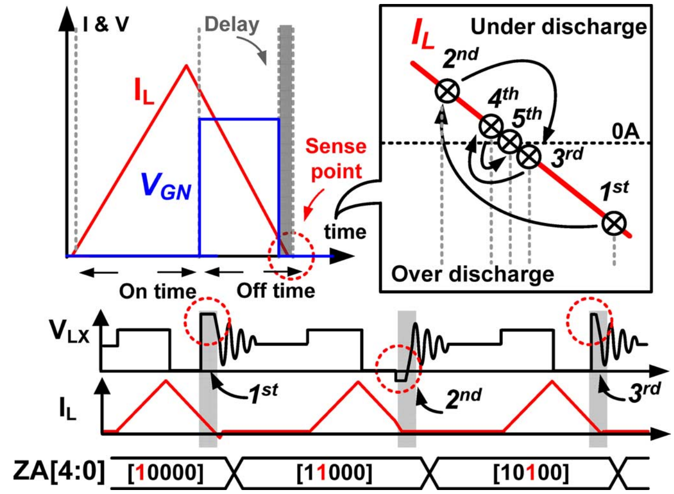



Fig. 6. $\alpha$-calibration scheme.

power MOSFETS $M_{P1}$ and $M_{N1}$. According to the output load condition, the switching period is extended to reduce switching loss. Thus, light-load efficiency can be significantly increased. The timing diagram of the DOOT controller is shown in Fig. 4(d).

### B. Implementation of the $\alpha$-Calibration Scheme

A number of non-ideal effects were observed, including capacitor mismatch, threshold voltage variation, transition point variation of the digital circuit, and current mismatch. These non-ideal effects will affect the timing balance of the proposed DOOT control, resulting in a difference between ratio of on-time and off-time and the desired value. As a result, a great deal of power loss will occur with inaccurate zero current switching.

As shown in Fig. 5(a), the timing of zero current switching is overly late. In other words, an overly long off-time will induce the reversed inductor current to dissipate a great deal of power. In contrast, an overly short off-time will induce the conduction of the body diode to result in conduction loss and in extra loss induced by the reverse recovery of the body diode, as shown in Fig. 5(b). An overly long or overly short off-time will result in extra power loss, thus significantly degrading power conversion efficiency. Therefore, an accurate ZCD to accomplish near zero current switching becomes more important to achieve high efficiency.

To overcome the non-ideal effects, the $\alpha$-calibration scheme is introduced to adjust the value of $C_3$ to meet the requirement of (7). When the value of $C_2$ is kept constant, the $\alpha$-calibration scheme can slightly tune the scaled input voltage $V_{\text{in}}$ on $V_{C2}$. Thus, the off-time period can be modified to accurately predict the zero current, that is, the near zero current switching. For the condition of overly long off-time, the discharging time has to be reduced through the decrease in the value of $C_3$. On the other hand, if the off-time period is overly short, the value of $C_3$ is extended to ensure correct zero current switching.

Therefore, the binary search algorithm is selected as the operating principle of the $\alpha$-calibration scheme as shown in Fig. 6. The $\alpha$-calibration circuit, as illustrated in Fig. 7(a) senses the value of $V_{LX}$ at the end of the off-time period to determine whether the off-time is overly long or overly short. The sensing information will be converted by a 5-bit successive approximation register (SAR), as shown in Fig. 7(b) to form a binary search.

Fig. 7(c) presents the circuit implementation of the 5-bit SAR circuit, which is composed of five registers with a multiplexer (MUX) and a D flip-flop (DFF). The sensing inverter generates the transition signal *Comp*, which is used to decide the status of an overly long or overly short ZCD and then stores the value in the SAR register. To initiate the calibration procedure, the most significant bit (MSB), $ZA[4]$, is set to high. Consequently, the sensing inverter generates the sensing result determined by $V_{LX}$. If $V_{LX}$ is low in the condition of an overly short off-time, logic "high" will be inputted into the 5-bit SAR to increase $C_3$. In contrast, a high value of $V_{LX}$, that is, an overly long off-time, indicates that the 5-bit SAR will decrease $C_3$. After each comparison, the current working register will trigger the next register to set the control code $ZA[\text{n}-1]=1$ for the sequent comparison and will then receive the comparison result from the *Comp* to adjust the output $ZA[\text{n}]$ to be one or zero.

After 5-cycles of comparison, the determination of the least significant bit occurs, and the last DFF will be triggered to high and then locked out. The output of the 5-bit SAR will be held to derive the accurate off-time value. An additional signal *"Lock"* derived from the off-chip control can lock out the 5-bit SAR or allow the LSB of the 5-bit SAR to continuously work. Finally, the calibration is finished, and the $\alpha$-calibration circuit (including the sensing inverter) is shut down to save power. The tuning range of $\alpha$-calibration can bear the tolerance of input voltage range from 1.2 to 2.5 V. The current mismatch can be up to 110% at the input voltage of 1.5 V.

## IV. APL Control Under Nano-Power Biasing Source

Due to low-power operation, the biasing circuit is designed as a nano-power biasing source. However, the low bias current will deteriorate the performance of the comparator, and consequently affect regulation performance. Thus, the APL-comparator is proposed to enhance the load regulation.

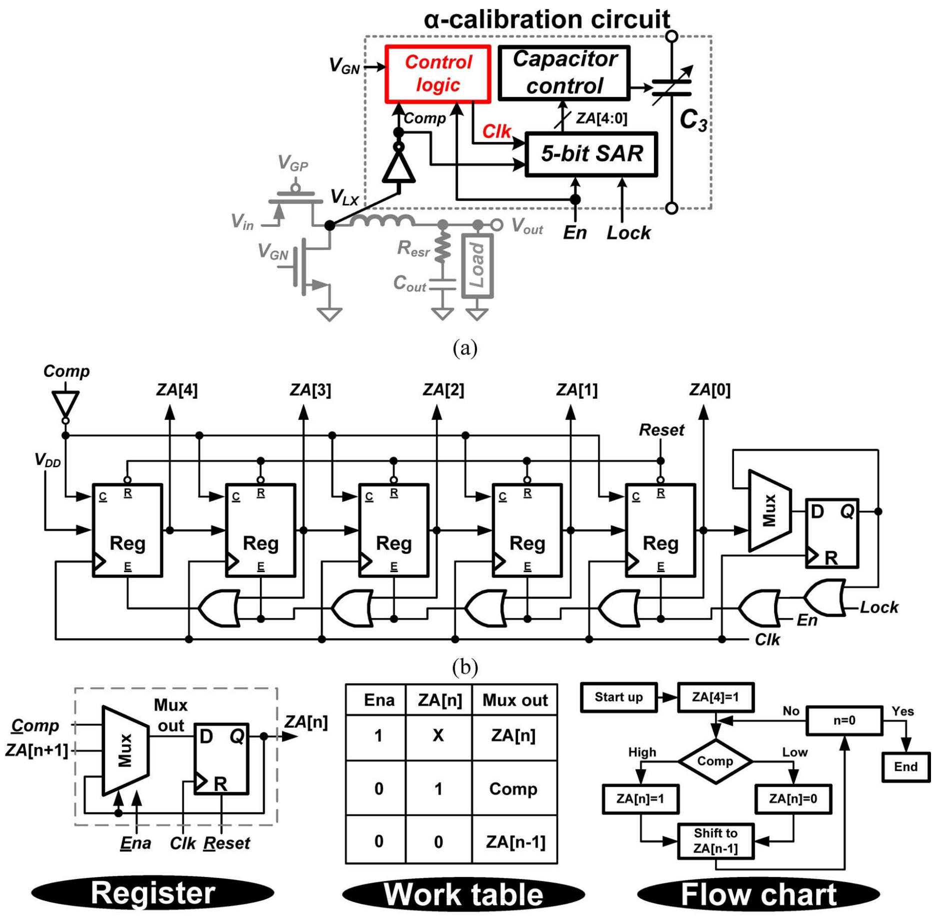



Fig. 7. (a) $\alpha$-calibration circuit. (b) 5-bit successive approximation register (SAR) circuit. (c) The register, the work table, and the flow chart.

### *A. Nano-Power Bias Circuit*

Fig. 8 shows the nano-power biasing current and voltage generator [15], [16] in the DOOT controller. The 5 V- negative-channel metal-oxide semiconductor (nMOS) transistors, $M_1$ and $M_3$, operated at the sub-threshold region acquire a nano-ampere quiescent current, $I_B$, which has a positive temperature coefficient. A 5 V-nMOS transistor $M_{10}$ has a large threshold voltage with a negative temperature coefficient, thus the temperature influence of the bias current is compensated. The output $V_{\rm ref}$ can be derived in (8) where the $M$ is the ratio of the mirror current and the $V_T$ is thermal voltage

$$V_{\rm ref} = V_{th({\rm M5})} + \left(\frac{(\sqrt{M}-1)+\sqrt{M}}{(N-1)}\right) \times m V_T \sqrt{\frac{\frac{W_4}{L_4}}{\frac{W_{10}}{L_{10}}}} \ln\left(\frac{\frac{W_3}{L_3}}{\frac{W_1}{L_1}}\right) \text{ where } N = \sqrt{\left(\frac{\frac{W_4}{L_4}}{\frac{W_2}{L_2}}\right)}. \quad (8)$$

In this work, the reference voltage $V_{\rm ref}$ is generated at 1 V, which is equal to $V_{\rm out}$, and a nano-ampere biasing current can be implemented. For a small silicon area and nano-watt requirement, the quiescent current of the DOOT controller can really be reduced.

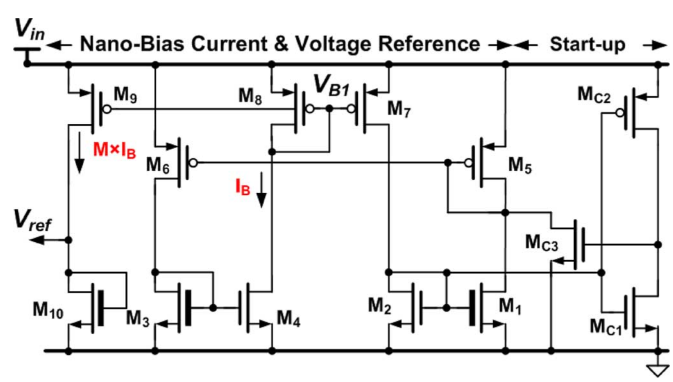



Fig. 8. Nano-power biasing current and reference voltage generator.

### *B. APL Comparator*

Since the tail current in the feedback comparator consumes only nano-ampere and thus results in a large propagation delay, the load regulation is seriously deteriorated. At light loads as shown in Fig. 9(a), the propagation delay of the comparator results in a slight output voltage drop during the delay period. However, at heavy loads, as depicted in Fig. 9(b), the output voltage drops rapidly during the delay period. The large output voltage drop not only affects the accuracy of $V_{\rm out}$, but also decreases the stability of the system. That is, as depicted in

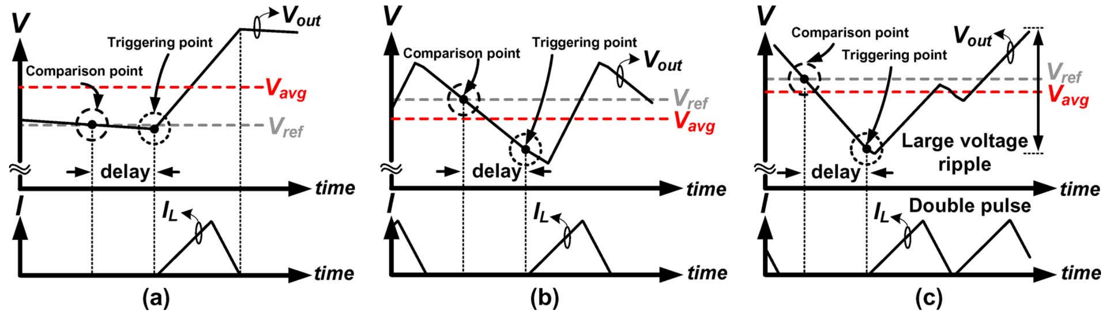



Fig. 9. (a) At light load condition. (b) At heavy load condition. (c) Double pulse condition at heavy loads.

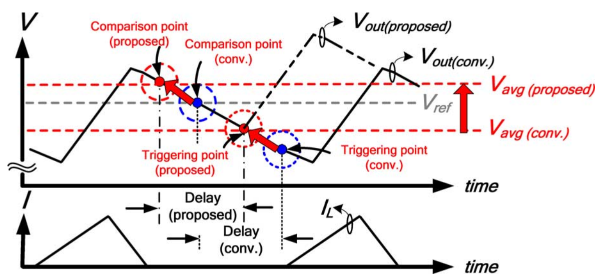
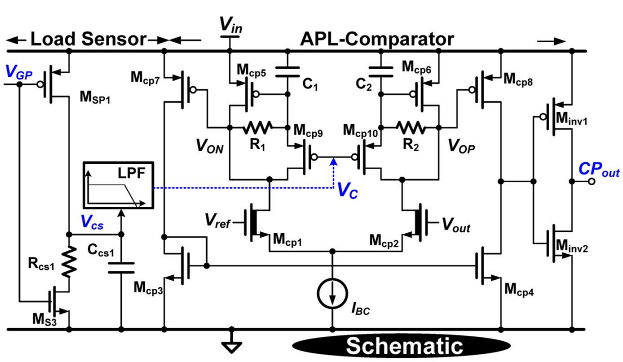
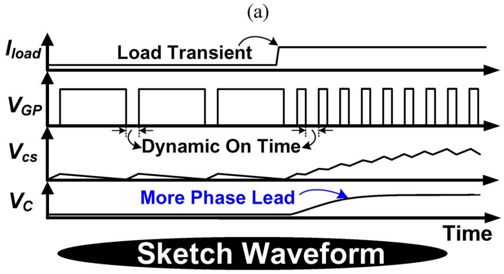



Fig. 10. Illustration of the adaptive phase leading control.




(a)




(b)

Fig. 11. (a) Schematic. (b) Timing diagrams of the load sensor and the APL-comparator.

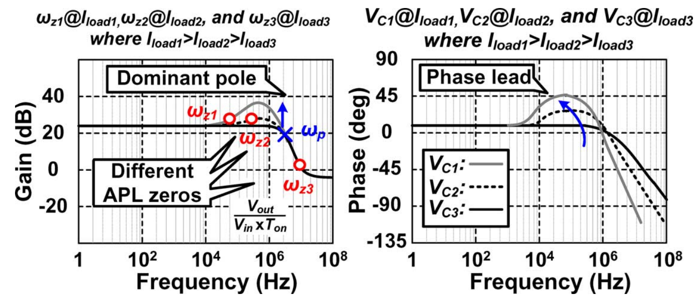



Fig. 12. Frequency response of the phase leading.

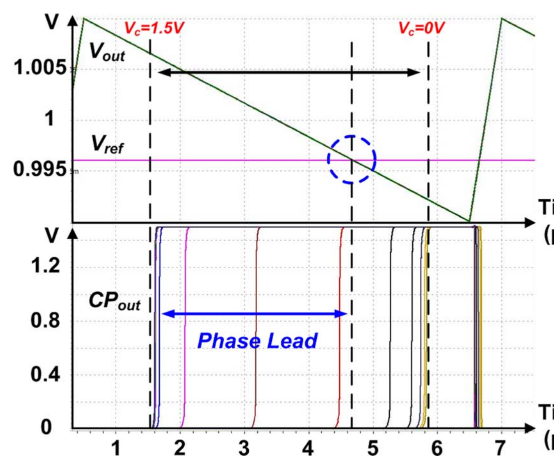



Fig. 13. Different transition thresholds contributed by the proposed APL comparator.

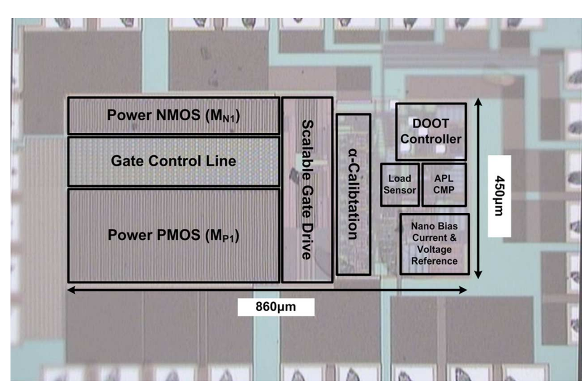



Fig. 14. Chip micrograph.

Fig. 9(c), the output voltage is regulated within double pulses, which greatly enlarge the output voltage ripple.

To compensate the delay attributable by nano-power biasing without inflating the power consumption of the comparator, an APL control is proposed, as shown in Fig. 10. The APL comparator shifts the comparison point to an earlier position under the same propagation delay. As a result, the triggering point will also be shifted to an earlier position. That is, the average output voltage $V_{\rm avg}$ is shifted back to its well-regulated voltage level, thus compensating the load regulation.

Fig. 11(a) presents a schematic of the load sensor and the APL-comparator with a central symmetry structure. The input pair of the APL-comparator employs the low-threshold-voltage transistors, $M_{cp1}$ and $M_{cp2}$, to improve the input common mode

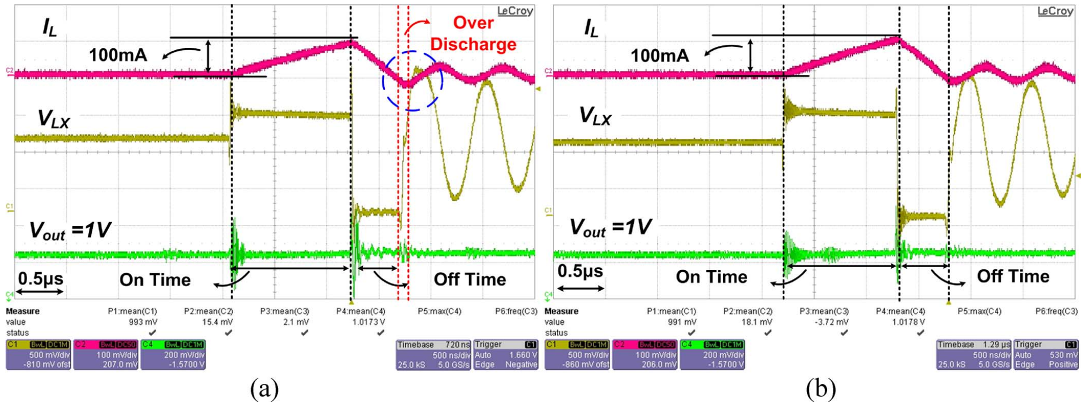



Fig. 15. Measured waveforms (a) before $\alpha$-calibration and (b) after $\alpha$-calibration in steady state.

TABLE I
STATIC POWER DISSIPATION TABLE

| | |
|---|---|
| Supply Voltage ($V_{in}$) | 1.2V |
| Output Voltage($V_{out}$) | 1V |
| Loading Condition | 1µA |
| Conduction Loss | 60nW |
| Driving Loss | 42nW |
| Dynamic On/off Time Generator | 7nA (avg.) |
| Voltage & Current Bias | 95nA |
| APL Comparator | 75nA |
| α-Calibration | N/A (Not operating in steady state) |
| Load Sensor | 4nA (avg.) |
| Controller Static Current | 181nA |

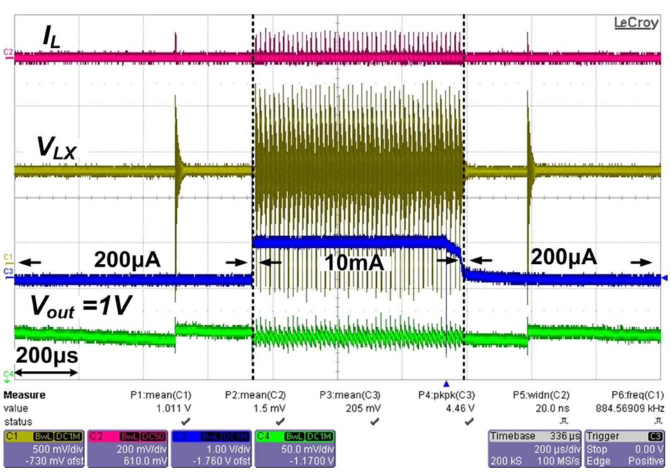



Fig. 16. Load transient response.

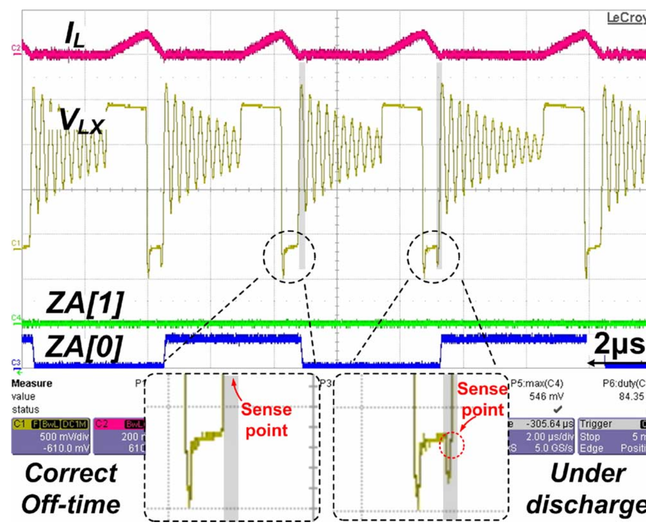



Fig. 17. Capacitance selection by $\alpha$-calibration circuit to determine the accurate off-time.

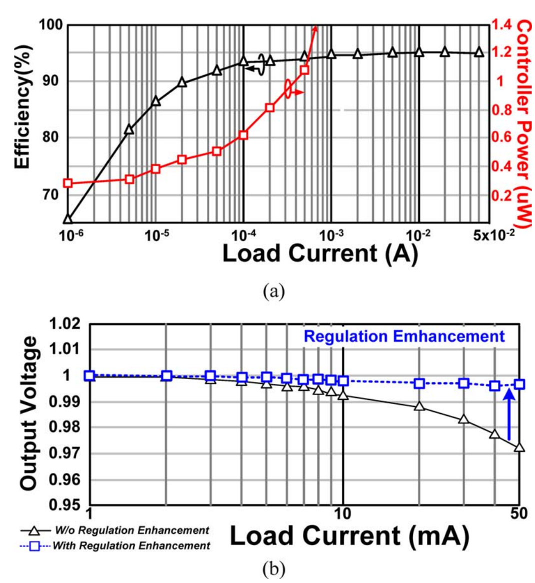



Fig. 18. Measurement of (a) controller power dissipation, efficiency, and (b) load regulation.

range (ICMR). In the DCM control, the switching frequency is proportional to the energy delivered to the output load. As the input voltage rises, a higher input voltage will lead to the rising of peak inductor current simultaneously, which indicates the energy delivered to the output and the loading condition. The load sensor provides the loading condition through $V_C$ based on switching frequency and input voltage. Fig. 11(b) shows the switching frequency and voltage relationship between $I_{\mathrm{load}}$ and $V_C$. The sensing method disuses the conventional current sensing scheme, thus saving a large amount of power. When the load current is smaller than several milliamperes, the performance of load regulation and conduction loss is fine. That is, the accuracy of the load sensor will not affect the performance. Therefore, the sensing range of the load sensor is focused on the current range above 10 mA.

TABLE II
COMPARISON TABLE

| | This Work | Inge Doms et al. [6] | Eric et al. [7] | Jun Yi et al.[8] | Suhwan Kim et al. [22] |
|---|---|---|---|---|---|
| Technology | 0.25 μm CMOS | 0.35 μm CMOS | 0.13 μm CMOS | 0.18 μm CMOS | 0.5 μm CMOS |
| Harvesting Source | RF signal | Thermoelectric | Thermoelectric | RF signal | Fuel Cell |
| Inductor | 3.3 μH | N/A | 4.7 μH | N/A | 150 μH |
| Capacitor | 4.7 μF | 175 pF | 10 nF | 1.055nF | 100 nF |
| Max Efficiency | 95 % | 82 % | 80 % | 16.4 % | N/A |
| Input Voltage | 1.2 to 2.5 V | 0.5 to 1 V | 20 to 250 mV | N/A | 0.6 V(Fuel Cell) 3.7 V (Li Ion) |
| Output Voltage | 1 V | 2 V | 1 V | 0.5 to 7V | 1 V |
| Static Power | 217 nW | 1.4 μW | 1.1 μW | 18 μW | 5 mW |
| Voltage Ripple | < 30 mV (1.2V Vin) | N/A | 20 mV | N/A | 50 mV |
| Load Regulation | 0.1 mV/ mA | N/A | N/A | N/A | N/A |
| Line Regulation | 3 mV/ V | N/A | N/A | N/A | N/A |
| Chip Size | 0.39 mm$^2$ | 3.06 mm$^2$ | 0.12 mm$^2$ | 0.56 mm$^2$ | 0.5 mm$^2$ (controller) |

In frequency domain, the first stage gain of the APL comparator is expressed as (9). In the transfer function, the compensation zero $\omega_{Z,\text{com}}$ and the dominate pole $\omega_P$ are shown in (10) and (11), respectively. When the $\omega_{Z,\text{com}}$ is smaller than $\omega_P$, the phase leading effect is derived to enhance load regulation.

$$A_{O1} = \left|\frac{V_{OP} - V_{\text{ON}}}{V_{\text{ref}} - V_{\text{out}}}\right| = \frac{gm_{cp1}}{gm_{cp5}} \cdot \left(\frac{1 + s(R_{cp9} \| R_1)C_1}{1 + s\frac{1}{gm_{cp5}}C_1}\right) = \frac{\left(1 + \frac{s}{\omega_{Z,\text{com}}}\right)}{\left(1 + \frac{s}{\omega_P}\right)} \tag{9}$$

$$\omega_{Z,\text{com}} = -\frac{1}{(R_{cp9} \| R_1) \cdot C_1} = -\frac{1}{R_C \cdot C_1} \text{ where } R_C = R_{cp9} \| R_1 \tag{10}$$

$$\omega_P = -\frac{1}{\frac{1}{gm_{cp5}} \cdot C_1}. \tag{11}$$

An increasing load current will increase $V_C$. Thus, the transconductance $g_{mp9}$ is decreased to move $\omega_{Z,\text{com}}$ toward the origin to increase phase lead. As illustrated in Fig. 12, a larger the value of $V_C$ denotes increased phase lead to compensate the effect attributable to the propagation delay, thus enhancing load regulation. The maximum leading phase is designed at approximately $V_{\text{out}}/(V_{\text{in}} * T_{\text{ON}})$, which is the highest operation frequency for the DCM control and is inversely proportional to the on-time pulse.

On the other hand, from the point of view of time domain, $V_C$ is utilized to control $g_{mp9}$, which serves as an adjustable resistor. Two parallel resistors $R_1$ and $R_{cp9}$ in series with $C_1$, construct a low pass filter at the gate of $M_{cp5}$. When a sudden disturbance occurs on the differential pair $M_{cp1}$ and $M_{cp2}$, the gate voltage of $M_{cp5}$ can not change instantly. Thus, an early transition occurs in the APL-comparator because $V_{\text{ON}}$ will have a large drop before $M_{cp5}$ can catch up. As $V_C$ varies from 0 to 1.5 V, the transition threshold variation of the APL comparator output $CP_{\text{out}}$ is shown in Fig. 13. The phase leading transition point is also highly related to the transition threshold of the back end inverter, so both the comparator and the inverter should be engaged simultaneously. The APL control remains in the low quiescent current of the comparator, but achieves good load regulation attributable to the phase leading.

## V. EXPERIMENTAL RESULTS

The proposed nano-power converter was fabricated in 0.25 $\mu$m CMOS process [21]. The chip area is 0.39 mm$^2$. The chip micrograph is shown in Fig. 14. Majority of the occupied silicon area is accounted for the implementation of embedded power switches and scalable gate control circuit.

Fig. 15 shows the inductor current $I_L$, the output voltage $V_{\text{out}}$, and $V_{LX}$ in steady state. The on/off time of the nano-power converter before $\alpha$-calibration is shown in Fig. 15(a), wherein the off-time generated by the DOOT controller is not perfectly matched with the zero current switching point. That is, an overly long off-time over discharges the inductor and results in the occurrence of a reverse current. The reverse current, which is obviously indicated by the waveform of $V_{LX}$ as shown in Fig. 15(a), degrades the power conversion efficiency. After the application of the $\alpha$-calibration scheme, Fig. 15(b) shows a calibrated off-time, which is well matched with the zero current switching point. High power conversion efficiency can be guaranteed.

The measured load transient waveform is shown in Fig. 16 where the load current changes from 200 $\mu$A to 10 mA and *vice versa*. $V_{\rm in}$ from the voltage doubler is approximately 1.5 V and $V_{\rm out}$ is regulated at 1 V. The switching frequency at 10 mA is higher than that at 200 $\mu$A. At heavy loads, the scalable gate driver will automatically turn on more power MOSFETs to reduce the on-resistance for low conduction loss according to the load sensor. Thus, high power conversion efficiency can also be ensured at heavy loads.

After off-time calibration contributed by the proposed $\alpha$-calibration circuit, when the locked out scheme of the 5-bit SAR is disabled by the external pin "*Lock*", the LSB ($ZA[0]$) can continue receiving the control signal *Comp* and continuously adjust the off-time. $ZA[0]$ should be adjusted back and forth from 1 to 0, because only a slight capacitance difference exists in the LSB of the tuning capacitor array. Most of the times, the off-time difference is not very obvious. The measurement of continuous adjustment is shown in Fig. 17. The off-time difference can be observed through the periodic drop of $V_{LX}$ at the end of the off-time.

Fig. 18 shows the measurement of load regulation, efficiency, and power. The output voltage is decreased by the increasing of load current because of the inherent delay of the comparator. The load sensor and the APL-comparator can detect the load current and have a phase lead effect to improve load regulation. The compensated comparator also eliminates the double pulse instability at heavy loads. When the input voltage is 1.2 V, the measured power efficiency is 61% at $I_{\rm load} = 1$ $\mu$A whereas the maximum efficiency is 95% at $I_{\rm load} = 20$ mA. The quiescent current of the DOOT controller is 181 nA (217 nW) when the input voltage is 1.2 V. Table I presents the test condition with the power consumption of each function blocks. Comparisons with other low-power converter methodologies are shown in Table II.

## VI. Conclusion

The proposed nano-power buck converter for RF energy harvesting system with DOOT control can minimize power dispassion down to 217 nW at 1 $\mu$A loading condition and consequently achieve high efficiency over wide load and input voltage ranges. The proposed $\alpha$-calibration scheme solves the inaccurate off-time resulting from PVT effects to simultaneously minimize conduction and switching losses. Nano-power bias circuit consumes low static power and generates a 1 V reference voltage to eliminate the need for feedback resistors. Furthermore, the APL control compensates the propagation delay attributable to the low quiescent current comparator, thus ensures good load regulation. The test chip occupies an active area of 0.39 $\text{mm}^2$ through fabrication in 0.25-$\mu$m CMOS process. Experimental results show that the correct operation of the nano-power buck converter, where 95% peak efficiency is achieved with an accurate ZCD.

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