

## Resistive switching characteristics of nickel silicide layer embedded HfO<sub>2</sub> film

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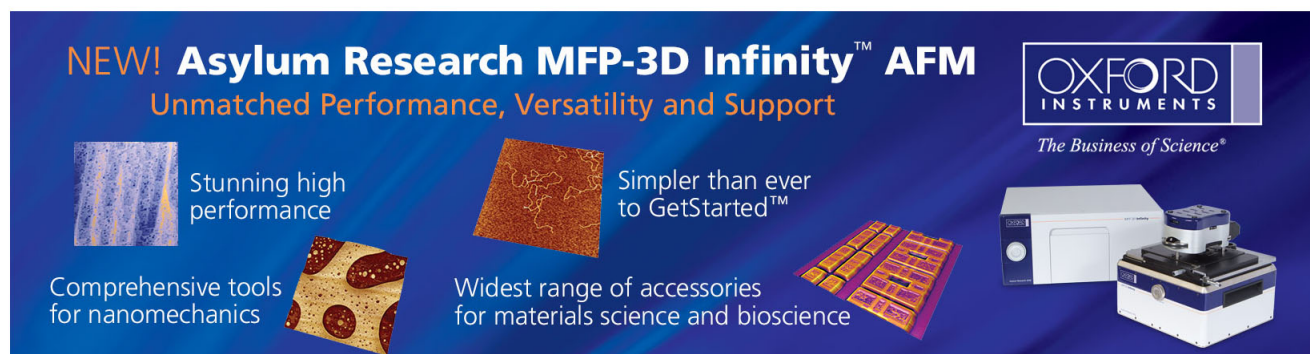
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# Resistive switching characteristics of nickel silicide layer embedded HfO<sub>2</sub> film

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Resistive switching behavior of the Ti/HfO<sub>2</sub>:NiSi:HfO<sub>2</sub>/Pt memory structure is investigated. Auger electron spectroscopy analysis indicates no metal diffusion from the electrodes and silicide layer on high-k film. Cross-sectional transmission electron microscopic micrographs revealed the thicknesses of the HfO<sub>2</sub> and silicide layer. Significant decrease of forming voltage is observed for the 550 °C, 1 min annealed device embedded with nickel silicide (NiSi) layers. Entire device shows bipolar switching properties with very low set/reset voltage. The optimized annealed device with NiSi embedded layer exhibits improved memory performances such as good on/off ratio ( $>10^2$ ), long retention more than  $10^4$  s, and reasonable endurance ( $>10^3$  cycles). A conducting filament model based on two stacks structure is employed to well explain the switching behaviors. © 2012 American Institute of Physics. [<http://dx.doi.org/10.1063/1.3694045>]

Resistance switching memory (RRAM) has attracted an immense interest for non-volatile semiconductor memory technology and applications,<sup>1–7</sup> because it has reversible and reproducible resistive switching (RS) characteristics induced by electrical or Joule heating effect.<sup>1,2</sup> A wide range of materials such as perovskite oxide, ferromagnetic material, transition metal oxides, and chalcogenides have been widely investigated to realize the resistive switching behaviors.<sup>1–7</sup> Metal elements or oxygen vacancies are usually considered as the active and indispensable components constituting the conducting filaments. Resistive switching mechanism is the formation and rupture of conductive filaments, caused by an appropriate applied voltage between top and bottom electrodes.<sup>1–4</sup> Many previous experiments demonstrate the presence of conducting filaments and the conducting filaments' ruptured position.<sup>2–7</sup> However, it still faces severe problems such as the stochastic formation and rupture of the filaments, which causes fluctuation during continuous switching cycles. It is indispensable to hunt for an effectual system to improve the stability of the resistive switching characteristics. For this reason, a few metal-oxide systems has been investigated on various methods such as metal doping,<sup>1,2</sup> inserting nanocrystals,<sup>6,7</sup> implanting Ti or Au,<sup>8,9</sup> and embedding metal layer<sup>10</sup> into the oxide, for the formation and improvement of resistive switching by increasing the device yield or narrowing the switching voltage distribution.<sup>9–12</sup>

In this study, we embedded the nickel silicide (NiSi) layer into hafnium oxide based devices to reduce the variations of memory states, because NiSi has a large work function (work function  $\sim 5.0$ – $4.7$  eV), making low temperature process, device fabrication compatibility, and so on.<sup>13</sup> Hafnium oxide (HfO<sub>2</sub>) based RRAM devices exhibited excellent switching characteristics and reliable data retention but showed huge variations in memory states due to higher degrees of random formation and rupture of conducting fila-

ments.<sup>14,15</sup> The switching performances and mechanism in the hafnium oxide film are associated with the charged oxygen vacancies. At nanometer scale devices, the quantities of oxygen vacancies determine the forming voltage ( $V_f$ ) and the switching characteristics, which is a significant issue to be investigated. In addition, we have also studied the physical and resistive switching properties of ultra-thin nickel silicide layer embedded hafnium oxide film.

A 10-nm thin HfO<sub>2</sub> film was grown using the Hf[N(C<sub>2</sub>H<sub>5</sub>)(CH<sub>3</sub>)<sub>4</sub>], so called TEMA and H<sub>2</sub>O precursors at 250 °C by atomic layer deposition (ALD) on the Pt/Ti/SiO<sub>2</sub>/Si substrate. Then, Ni/Si/Ni (0.4 nm/0.8 nm/0.4 nm) multilayer thin film was deposited on the HfO<sub>2</sub> film by e-beam evaporation with a nominal deposition rate of  $<0.1$  Å/s. After the deposition of Ni/Si multi layers, another 10 nm thick HfO<sub>2</sub> film was deposited on it by the same process to form HfO<sub>2</sub>:NiSi:HfO<sub>2</sub> sandwich structure. Subsequently, the devices were post metal annealed (PMA) at 400–550 °C for 1–2 min in N<sub>2</sub> ambient for silicidation. A Ti/Pt (50 nm/20 nm) top electrodes (circular diameter: 150  $\mu$ m) were deposited by e-beam evaporation to form Pt/Ti/HfO<sub>2</sub>:NiSi:HfO<sub>2</sub>/Pt/Ti/SiO<sub>2</sub>/Si structure for memory device characterization. A 20 nm thick HfO<sub>2</sub> control device (without NiSi layer) was also prepared and annealed under the same conditions as a control sample for comparison. Crystal structures of the films were studied using glancing angle x-ray diffraction (XRD) (Bede D1). Film compositions at different depth were also studied using auger electron spectroscopy (AES) (VG Scientific Microlab 310F). To probe the thickness and composition of the layers, cross-sectional transmission electron microscopic (XTEM) observations were performed using JEOL JEM-2010F. The electrical switching characteristics of the fabricated RRAM devices were measured using an Agilent 4155C analyzer.

Typical XRD spectra of the as-deposited and 550 °C, 1 min annealed NiSi embedded devices are shown in Fig. 1(a). It shows diffraction peaks of (210), (002), (101), (012), (021), (031), (113), and (200), which is partially crystallized HfO<sub>2</sub> after annealing. No signature of NiSi phases is

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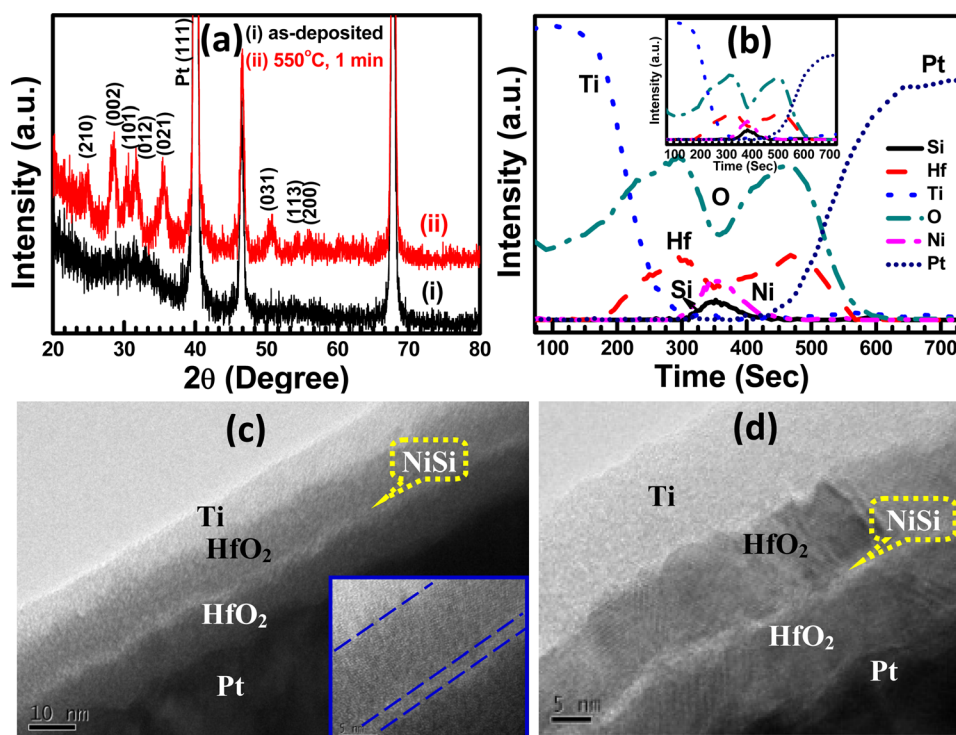
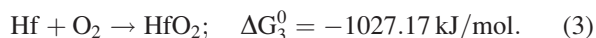
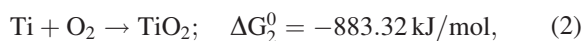
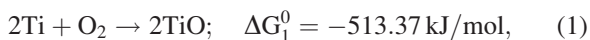


FIG. 1. (Color online) (a) Typical XRD spectra of the as-deposited and 550 °C, 1 min annealed NiSi embedded device; (b) AES spectra of the as-deposited device and inset shows the spectra of 550 °C, 1 min annealed silicide embedded device; (c) typical cross-sectional TEM image of as-deposited HfO<sub>2</sub> based RRAM device with embedded NiSi layer, inset shows the high resolution view; and (d) XTEM image of the 550 °C, 1 min annealed device.

observed due to very small thickness ( $\sim 1.5$  nm) of silicide layer. There are no metal/semiconductor such as Ti, Ni, Si, and Pt atoms inter-diffusion at high- $k$  HfO<sub>2</sub> observed even after annealing based on the measurement and analysis of the AES spectra, as shown in Fig. 1(b). But, intermixing of the NiSi layer is confirmed from the AES spectra. As seen from the inset of Fig. 1(b), the oxygen atoms concentration increases after 140 s and again decreases after 190 s compared to the spectra of as-deposited film of Fig. 1(b), due to the migration of oxygen atoms. It indicates that the formation of interfacial TiO<sub>x</sub> layer at Ti/HfO<sub>2</sub> interface by the diffusion of oxygen atoms from the HfO<sub>2</sub> layer to the Ti top electrode after annealing. These results corroborate the results obtained from the XTEM EDX analysis. Formation and stability of TiO, TiO<sub>2</sub>, and HfO<sub>2</sub> can be explained by thermo-dynamical consideration using Gibbs free energy. The formation equations of these oxides can be expressed as<sup>16</sup>



From the Eqs. (1)–(3), it can be observed that the Gibbs free energy ( $\Delta G_3^0$ ) of HfO<sub>2</sub> is more negative than those of TiO and TiO<sub>2</sub>, signifying that the HfO<sub>2</sub> is more stable than TiO or TiO<sub>2</sub>. This is indicated that the oxygen ions can easily drift from the quite unstable titanium oxide layer to the HfO<sub>2</sub> layer or vice versa depending on the applied electric field, during switching process. For this memory structure, titanium oxide acts as an oxygen reservoir. This thermodynamic prediction also fits well with the experimental results. Good interfaces of Pt/HfO<sub>2</sub> and HfO<sub>2</sub>/NiSi layers are observed for

the as-deposited and annealed devices [Figs. 1(c) and 1(d)]. But, no distinguishable interfacial TiO<sub>x</sub> and HfO<sub>y</sub> layers are identified from the spectra of annealed device as shown in Fig. 1(d). Total active layer thickness (HfO<sub>2</sub>:NiSi:HfO<sub>2</sub>) is found to be  $\sim 21$  nm. The high resolution image of the as-deposited device, inset of Fig. 1(c), shows the  $\sim 1.5$  nm thick Ni-Si-Ni layer sandwiched between the HfO<sub>2</sub> layers. It is very difficult to find individual interface layers of Ni and Si for the as-deposited devices. This is may be due to the partial intermixing of Ni and Si during top HfO<sub>2</sub> deposition at 250 °C. After annealing at 550 °C, 1 min, the complete silicidation with thickness of  $\sim 1.5$  nm is observed [Fig. 1(d)]. Crystallinity of HfO<sub>2</sub> layer after annealing is detected from the lattice fringes. The XTEM results corroborate the results obtained from XRD and AES.

A forming process is necessary for this memory structure to initiate the resistive switching behaviour, by which the pristine device is subjected to a high voltage stress inducing a soft dielectric breakdown.<sup>2–7</sup> Fig. 2(a) shows the typical I-V forming curve and corresponding reset process of the different annealed NiSi layer embedded HfO<sub>2</sub> films. The forming voltages are decreased with an increase of annealing temperature, as shown in Fig. 2(b). A high forming voltage of  $\sim 8.9$  V is required for the as-deposited device and it is decreased significantly to  $\sim 4.7$  V for the optimized 550 °C, 1 min annealed device. When we increase the annealing time for 2 min, the forming voltage is slightly increased, due to the increased crystallinity of HfO<sub>2</sub>,<sup>17,18</sup> observed from the XRD spectra [Fig. 1(a)], and change of silicide's resistivity.<sup>19,20</sup> There are negligible change in leakage current during forming process, indicates the good uniformity and stoichiometry of the dielectric film [Fig. 2(a)]. We consider that this decrease of forming voltage is due to two reasons. First, this improvement is due to the effect of conductive silicide layer. Second, the oxygen atoms migrating from HfO<sub>2</sub>



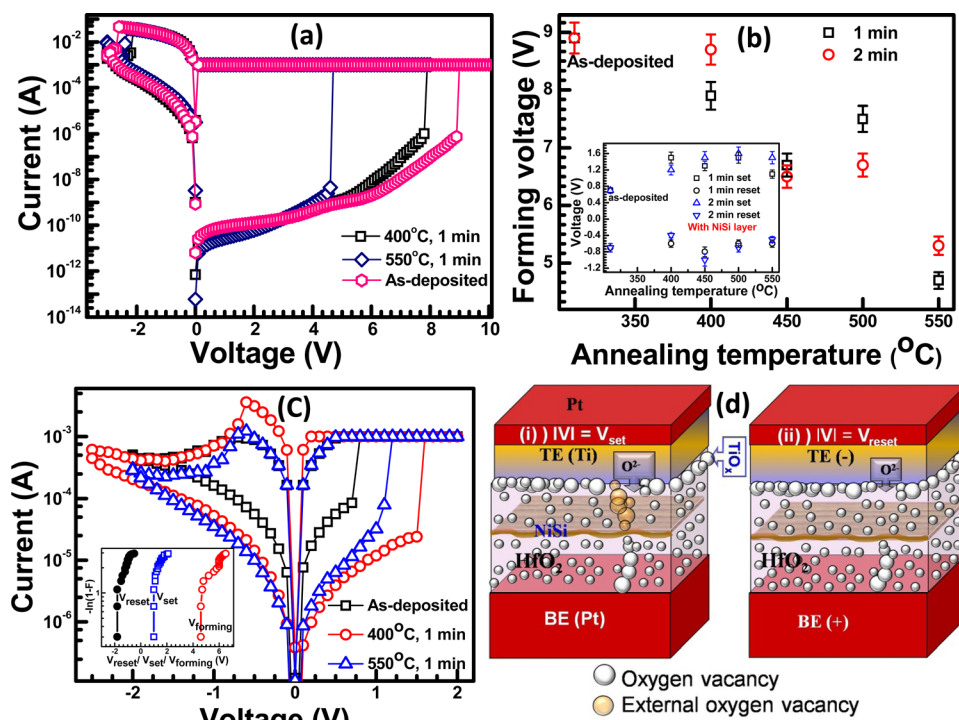


FIG. 2. (Color online) (a) Typical forming curve and corresponding “reset” curve of as-deposited, 400 °C and 550 °C, 1 min annealed Ti/HfO<sub>2</sub>:NiSi:HfO<sub>2</sub>/Pt devices; (b) variation of forming voltage of the different devices annealed at different temperature and time, inset shows the variations of “set/reset” voltages; (c) I-V switching characteristics of those devices, inset shows weibull distributions of forming, set and reset voltages of 550 °C, 1 min annealed NiSi embedded devices; (d) schematic description of switching mechanism (i) set and (ii) reset processes.

to reactive Ti top electrode at high temperature annealing form TiO<sub>x</sub> layer that deteriorates the dielectric strength of the buried HfO<sub>y</sub> film. But, we think that the first reason is more dominant to improve the forming voltage for our devices. At the same PMA temperature, the reduction of forming voltage in silicide layer embedded devices are much better than that in the control devices, due to the reduction of effective thickness by conductive nickel silicide layer.

After forming process, typical bipolar *I-V* hysteresis curves are observed during bias sweeping for the as-deposited and annealed devices with and without NiSi layer embedded structure [Fig. 2(c)]. During “set” process, a positive voltage sweep ( $V_{\text{set}} \sim 0.7$  to  $1.5$  V) with a current compliance of 1 mA triggers the conduction, and the resistance is switched from high resistance state (HRS) to low resistance state (LRS). Afterward, a negative voltage sweep of  $V_{\text{reset}} \sim -0.7$  to  $-1$  V causes abrupt decrease of current and the device is switched back to HRS (denoted as “reset” process). The polarity dependence of “set” and “reset” transition indicates bipolar RS characteristics. Significant changes on the whole switching parameters are observed on various annealed devices with NiSi layers, after testing at several switching cycles. The silicide layer embedded devices annealed at 550 °C, 1 min shows superior properties compared to others in terms of forming voltage, “set/reset” voltage, endurance and resistance ratio between two resistance states. The NiSi layer embedded device with a longer annealing time shows poor switching properties than the optimized one. This is due to the formation of high resistive di-silicide phase and good crystallinity of HfO<sub>2</sub> film. It was reported that the annealing temperature and time affect significantly the resistivity of silicides.<sup>19,20</sup> On the other hand, the devices annealed at lower temperature also show good LRS to HRS ratio, small “set/reset” voltage, but poor cycling. This is due to the incomplete silicidation at lower annealing tempera-

ture. As observed from the inset of Fig. 2(b), the “reset” voltages for all devices are almost the same, but the “set” voltages are increased slightly. Though the oxide thicknesses of all devices are almost identical and the switching mechanism during “set” process attributed by the filament formation. Furthermore, “set” voltages are increased rapidly from 1 to 2.6 V for the control devices (without NiSi embedded layer) after annealing (not shown here). The increase of “set” voltage after annealing can be explained by the crystallization of HfO<sub>y</sub> dielectrics. Switching parameters also depend on the interfacial TiO<sub>x</sub> layer thickness at the Ti/HfO<sub>2</sub> interface. The thickness of this oxygen reservoir increases with the increase of annealing temperature and time. Slight decrease of “set/reset” voltages of the silicide layer embedded device after 550 °C, 1 min annealing is due to the effect of crystallinity of silicide layer and higher TiO<sub>x</sub> layer thickness, which will be discussed briefly later. “Set” and “reset” voltages of the optimized 550 °C, 1 min annealed silicide embedded devices are 1.1 V and  $-0.6$  V, respectively. Statistical distributions of “forming”, “set” and “reset” voltages of the 550 °C, 1 min annealed silicide embedded devices are shown in the inset of Fig. 2(c).

Switching mechanism of high-*k* oxide based resistive switching memory devices is based on the formation and rupture of polarity dependent percolated conduction channels, known as filaments, formed by oxygen vacancies in oxide films, which leads to the formation of a robust but reversible conducting pathway.<sup>1–15</sup> A thin conducting silicide layer between the HfO<sub>2</sub> dielectric films initiate to formation and rupture of the conducting filaments by enhancing local electric field and reducing the effective HfO<sub>2</sub> thickness.<sup>21</sup> High compliance current of 1 mA is used during forming process to avoid the current overshoot issue for high quality oxide film, such as ALD grown HfO<sub>2</sub> film.<sup>8,22</sup> When a positive bias larger than threshold voltage is applied, the

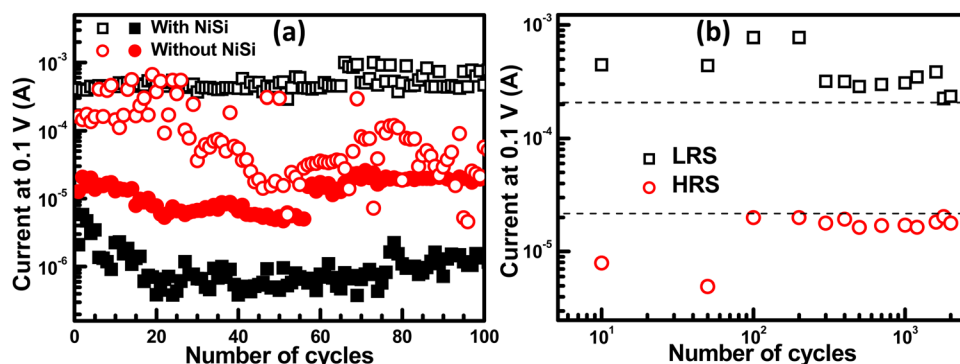


FIG. 3. (Color online) (a) Comparison of endurance properties of 550 °C, 1 min annealed NiSi embedded device with control device and (b) typical long term endurance data of the optimized NiSi embedded device.

device is switched from HRS to LRS, i.e., ON state, by making a conducting path in  $\text{HfO}_2$ . In binary oxide based RRAM, the existence of oxygen ions and/or oxygen vacancies would play a significant role in resistive switching, leading to reduction and oxidization of conducting filaments. Formation and rupture of the filaments always occur at anode interface. Usually Ti is an oxygen gettering metal, and it is easily formed an ultrathin  $\text{TiO}_x$  layer at the interface. Ti top electrode can modify the oxygen contents, oxygen vacancies, oxygen ions, and oxygen-related defects distributions at  $\text{HfO}_2$  films and further causes the formation of both  $\text{TiO}_x$  and oxygen deficient  $\text{HfO}_y$  layers. The formation of  $\text{TiO}_x$  layer at the interface is detected from the AES spectra (Fig. 1(b)). The thickness of this  $\text{TiO}_x$  layer is increased or decreased during voltage sweeping to make volatile thick or thin  $\text{TiO}_x$  layer.

Switching mechanism of the silicide layer embedded devices is shown schematically in Fig. 2(d). We consider that there are two RRAM stacks, stack 1 is the  $\text{Ti}/\text{HfO}_2/\text{NiSi}$  and stack 2 is  $\text{NiSi}/\text{HfO}_2/\text{Pt}$ , which are separated by the silicide layer. As seen from the TEM image (Fig. 1(d)), the silicide thickness is not homogeneous. At some places it is percolated or agglomerated and little thicker. After forming process, the localized conduction filament consisting of oxygen vacancies is formed between top and bottom electrode through the agglomerated and thicker part of the intermediate conducting NiSi layer because of local electric field enhancement and the device is switched to LRS [(i) of Fig. 2(d)]. After applying negative voltage equal to or more than reset voltage on top electrode, the oxygen ions are drifted to stack 1 from the interfacial oxygen reservoir ( $\text{TiO}_x$ ) to reoxidize the conducting filament completely at stack 1 by local Joule heating effect and the device is switched back to HRS [(ii) of Fig. 2(d)]. Here, the conducting filaments below the metallic silicide layer are expected to remain unaffected, since the oxygen ions cannot pass through the electronic conductor silicide and drift to stack 2.<sup>21</sup> A high voltage ( $\sim 4.7$  V) is required during forming process due to the formation of filament between two electrodes. But, during “set” process only filament is formed at stack 1 only, as a result lower voltage ( $\sim 0.8$  V) is required. It was shown in Fig. 2(b) that at higher annealing time the forming voltage and “set” voltages are increased because the conductivity of the silicide layers decreases.

Nickel silicide layer embedded  $\text{HfO}_2$  devices exhibit good reliabilities. Figure 3(a) shows the comparison of en-

durance properties of the control devices without embedded NiSi layer and the 550 °C, 1 min annealed NiSi layer embedded devices up to first successive 100 cycles. As seen from the figure, the NiSi layer embedded devices show much more stable cycling properties at the both resistance states than those without NiSi layers. The resistance ratio is decreased and finally two resistance states are overlapped before 100 cycles for the control devices only. This indicates the improvement of endurance properties due to the effect of intermediate silicide layer. Endurance of the optimized NiSi embedded devices is exceeded  $2 \times 10^3$  cycles, as shown in Fig. 3(b). Currents at HRS and LRS are increased from  $7.9 \mu\text{A}$  to  $20 \mu\text{A}$  and decreases from  $99 \text{ mA}$  to  $2 \text{ mA}$ , with an increase of cycling number, respectively. Gradual decreasing of the resistance ratio during cycling is due to the degradation of LRS current, which comes from the non-ideal current compliance nature of the analyzer system.<sup>4</sup> This problem can be resolved completely by using a good current limiter from the memory circuit.<sup>4</sup> Retention properties of those with and without silicide embedded devices annealed at 550 °C, 1 min are examined for more than  $10^4$  s, at 0.1 V, as shown in Fig. 4. Both the devices show no sign of any degradation in retention lifetime.

In conclusion, the NiSi layer embedded in ALD grown  $\text{HfO}_2$  resistive switching memory structure showed superior resistive switching characteristics suitable for nonvolatile memory devices. Crystal structure, compositional profiles at

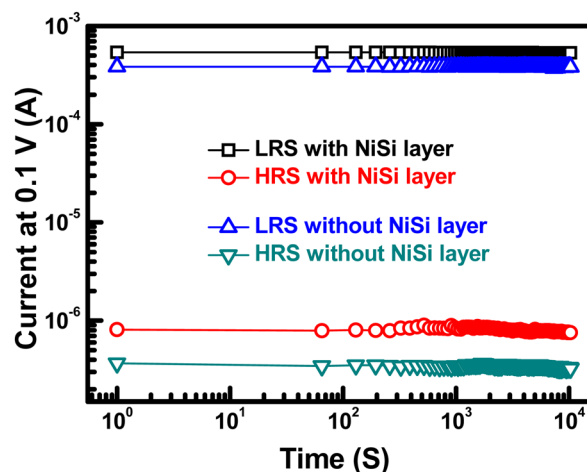


FIG. 4. (Color online) Typical retention characteristics of 550 °C, 1 min annealed NiSi embedded and without NiSi embedded devices.

different layers, and formation of silicide layer by thermal annealing have been confirmed from the XRD, AES, and HRTEM analyses. Bipolar resistive switching properties have been observed for all the devices. Forming and “set” voltages of the NiSi layer embedded devices are notably decreased after annealing at 550 °C, 1 min. The effect of Ti top electrode and NiSi layer on switching mechanism has been investigated. Good resistance ratio, long retention time up to  $10^4$  s and acceptable endurance more than  $10^3$  cycles are observed for the optimized annealed device with NiSi embedded layer. Therefore, the Ti/HfO<sub>2</sub>/NiSi:HfO<sub>2</sub>/Pt sandwich structure has high potential for practical nonvolatile memory applications.

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