Power-Tracking Embedded Buck–Boost Converter With Fast Dynamic Voltage Scaling for the SoC System

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***Abstract*—A power-tracking embedded buck–boost converter with a fast dynamic voltage scaling (F-DVS) function is proposed to power the system-on-a-chip (SoC) system. To meet the power request of the SoC for different operation functions, fast up/down-tracking is implemented to achieve the F-DVS function. Recycling energy is also derived to minimize power dissipation during the down-tracking period. In addition, the peak current control and valley current control methods are utilized in the buck and boost operations, respectively, to minimize the effect of switching noise in high switching operation for compact solution. Moreover, the self-tuning pulse skipping mechanism extends the effective duty cycle to achieve voltage regulation and improves efficiency when the input voltage is close to that of the output. Through F-DVS, the tracking speed from 3 to 2 V and vice versa are 15 and 20 μs, respectively, with a high switching frequency of 5 MHz.**

***Index Terms*—Buck–boost (BB) converter, dc–dc converter, dynamic voltage scaling (DVS), peak current control (PCC), power tracking, pulse skipping, system-on-a-chip (SoC), valley current control (VCC).**

I. Introduction

SYSTEM-ON-A-CHIP (SoC) system is a design trend in today's consumer portable devices. Power management module is demanded to have high efficiency, low output voltage ripple, and fast transient response at the same time. To effectively power the battery-operated portable system, dc–dc converter is utilized to provide a constant output voltage over a wide input voltage range from the Li-ion battery [1]–[3]. The buck–boost (BB) converter [4]–[20] can operate in either the buck or boost operation to convert a regulated output voltage according to the input voltage condition. However, the transition between these two different operations may result in large output voltage ripple due to their different operated characteristics. Thus, it is important to ensure smooth transition between the two operations in BB converter. As reported in [8], a three-mode dual-frequency two-edge modulation scheme is implemented to handle the transition when the input voltage level is close to that of output. In addition, the feedforward control scheme is utilized to improve the mode transition and the line transient response in voltage-mode BB converters [10]–[12]. The transient response should be taken into consideration owing to the diffident power requests from the distinct operation modes in the SoC system. Although a digital control scheme is proposed to enhance the transient response [13], a digital signal processing unit is needed to provide the control signals.

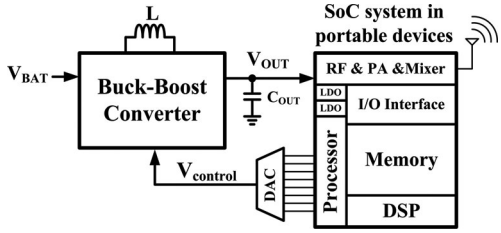

Fig. 1. System application of the PTE-BB converter for the SoC system in portable devices.

Fig. 1 shows the system application of the proposed power-tracking embedded BB (PTE-BB) converter. To power the function blocks in the SoC system, the PTE-BB converter can automatically switch the operation modes to generate a regulated output voltage $V_{\rm OUT}$ with different input voltage $V_{\rm BAT}$. For example, high-efficiency RF power amplifier is a critical part of the SoC system. The required power depends on the different operation mode, such as the demands for a large power supply to achieve data transmission [15]–[19]. In the conventional dynamic voltage scaling (DVS) design [21]–[24], the settling time for achieving output voltage position is determined by the system loop response. However, the slow voltage tracking speed deteriorates the performance of the RF circuit, since the supply power is insufficient at the beginning of the data transmission period. As a result, the proposed PTE-BB converter presents a fast DVS (F-DVS) function that can achieve fast voltage-tracking response and precise voltage position through the signal $V_{\rm control}$ sent from the SoC system. The optimum value of $V_{\rm control}$ is generated from the processor and converted by the digital-to-analog

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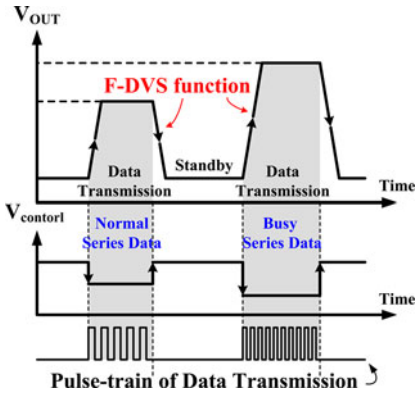

Fig. 2. Operations of the F-DVS function in the data transmission periods of the RF circuit in the SoC system.

converter (DAC) to indicate the different energy request of the SoC system to power management. Thus, high performance and high efficiency can be simultaneously achieved.

The operation of the proposed F-DVS function is shown in Fig. 2. When the data transmission period is activated, the signal $V_{\rm control}$ starts up-tracking response in the PTE-BB converter to raise the output voltage for improving the driving capability. In addition, a larger power request is obtained by the busy series data transmission. $V_{\rm OUT}$ is returned to its nominal value when the data transmission period is over in order to minimize the power consumption for extending the battery life. Similarly, the signal $V_{\rm control}$ also enables the down-tracking response to meet the power demand in the standby period. Therefore, the F-DVS function of the PTE-BB converter achieves both fast voltage-tracking and adjustable output voltage. Moreover, to avoid the effect of system instability resulting from the switching noise in high switching operation, the PTE-BB converter utilizes the dual-mode operation, which includes the peak current control (PCC) [25] in the buck operation and the valley current control (VCC) in the boost operation, respectively. The self-tuning pulse skipping (SPS) mechanism is also implemented to achieve the smooth mode transition in the BB converter when the value of $V_{\rm BAT}$ is closed to that of $V_{\rm OUT}$.

In this paper, the structure of the proposed PTE-BB converter is described in Section II. The system operation is illustrated in Section III. Detailed circuit implantation is presented in Section IV. Experimental results are shown in Section V. Finally, the conclusion is made in Section VI.

II. Proposed BB Converter Structure

The structure of the PTE-BB converter is shown in Fig. 3. The current-mode control is utilized to achieve fast transient response, better line rejection capability, and on-chip system compensation scheme at the same time. In addition, the output voltage ripple is minimized especially for some noise-sensitive blocks, such as the RF circuits in the SoC system. Using the high switching frequency in dc–dc converter can decrease the output voltage ripple and reduces the value of off-chip inductor to further reduce the printed circuit board area.

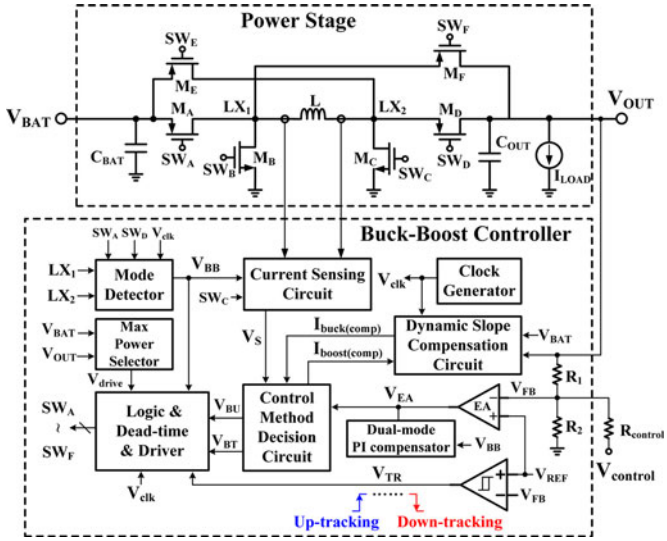

Fig. 3. Proposed structure of the PTE-BB converter with the F-DVS function.

The power stage in the PTE-BB converter contains six power switches, M_A–M_F, to achieve the energy transition and the F-DVS function. The signal $V_{\rm TR}$ generated by the hysteresis comparator enables the F-DVS function through the rising and falling edge triggers to achieve the up-tracking and down-tracking of the output voltage, respectively. The resistors R_1 and R_2 form the voltage feedback to regulate the output voltage. The error signal $V_{\rm EA}$ generated by a high-gain error amplifier makes a comparison with the summing signal, which is the summation of the current-sensing signal V_S and the slope compensation signal, in order to generate the control duties, $V_{\rm BU}$ and $V_{\rm BT}$, for the buck and boost operations, respectively. Besides, the current-sensing circuit realizes the high-speed current sensing at the high switching operation.

The dynamic slope compensation (DSC) circuit produces the slope compensation signals, $I_{\rm buck(comp)}$ and $I_{\rm boost(comp)}$, to avoid the subharmonic oscillation in the PCC or VCC methods, respectively. The mode detector circuit is used to determine the operation mode by generating the $V_{\rm BB}$ signal in the PTE-BB converter based on the conditions between the battery and the output. The master and slave control scheme is implemented with the SPS mechanism to ensure smooth mode transition. As such, the signal $V_{\rm BB}$ with a low value indicates the buck operation, while the boost operation is utilized when $V_{\rm BB}$ is forced to high. Moreover, the dual-mode proportional-integral (PI) compensator [26] guarantees the on-chip compensation through the system pole-zero cancellation in the current-mode control. The clock generator carries out the system clock $V_{\rm clk}$ with 5 MHz for high switching pulse width modulation (PWM) operation. The dead time and driver circuit, which are supplied by the supply voltage $V_{\rm drive}$ generated through the maximum power selector, produce the control signals $\rm SW_A$–$\rm SW_F$ to drive the power switches, M_A–M_F, respectively, thereby enhancing the driving ability and avoiding the shoot-through current.

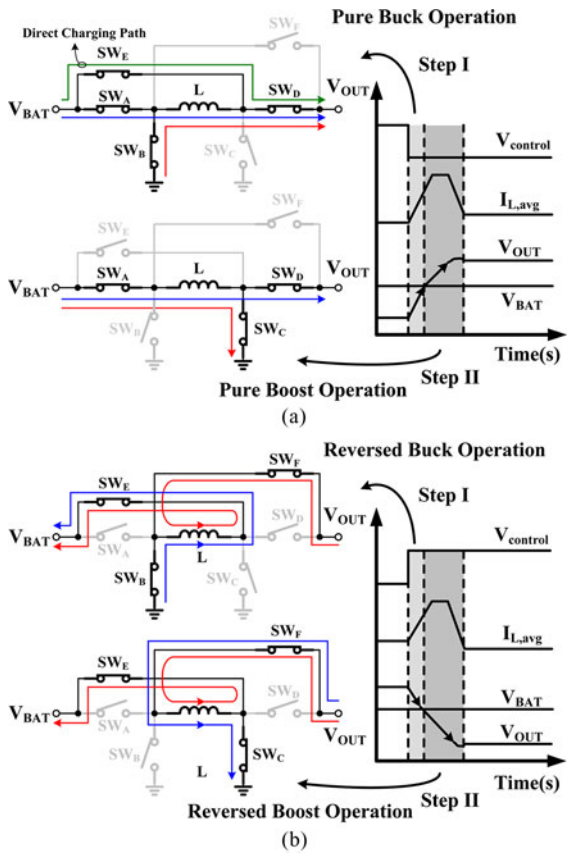

Fig. 4. F-DVS function contains fast (a) up-tracking and (b) down-tracking.

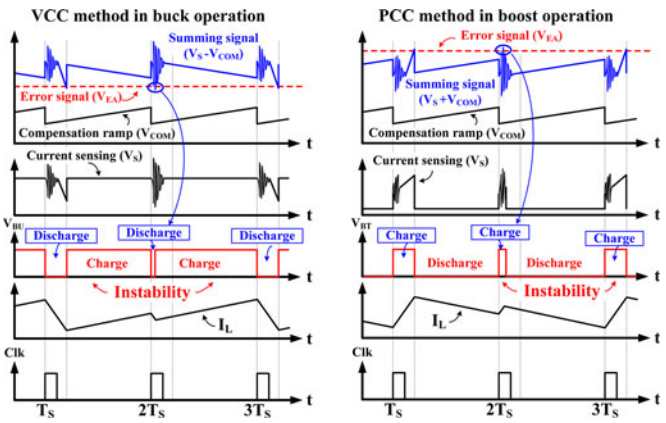

Fig. 5. Duty cycle modulation considers the noise effect in the BB converter when the value of V_{BAT} is close to that of V_{OUT}. (a) VCC method in the buck operation. (b) PCC method in the boost operation.

III. System Operation

A. F-DVS Function

Fast transient response and short settling time are necessary to achieve the F-DVS function in the PTE-BB converter for the SoC system. Particularly, a high voltage supply is needed to provide better driving capability during the data transmission period. Fig. 4(a) shows the operating scheme of fast up-tracking with energy delivering path defined in the F-DVS function. The up-tracking process is divided into two steps in order to effectively control the inductor current. In step I, if V_{BAT} is larger than V_{OUT}, the PTE-BB converter operates in pure buck operation with a maximum charging current control. Furthermore, a direct charging path, which is composed of the power switches with M_E and M_D, is adopted to accelerate the tracking speed, especially under the condition wherein only a small voltage difference between V_{BAT} and V_{OUT} is derived at the beginning of the tracking response. In addition, once V_{OUT} exceeds the value of V_{BAT} in the up-tracking response, the control scheme ends the direct charging path and enters into step II with a pure boost operation. The operation is switched to the boost operation and uses a maximum charging current control until V_{OUT} approaches the desired regulated voltage. Thus, with the two-step up-tracking procedure, V_{OUT} can be raised up rapidly to meet the power request of the SoC system.

On the other hand, when the data transition ends, the system returns to the standby mode for power saving. The F-DVS function provides a fast down-tracking scheme as shown in Fig. 4(b). The down-tracking process is also divided into two steps to effectively achieve voltage tracking. The PTE-BB converter operates the reversed buck operation in step I to transfer the excessive energy back to the input through inductor when V_{OUT} is larger than V_{BAT}, achieving a fast down-tracking response and the minimized power dissipation. Moreover, step II is activated when V_{OUT} is lower than the value of V_{BAT} that the PTE-BB converter can deliver the energy from C_{OUT} to battery through the maximum charging current control. Finally, step II ends until the value of V_{OUT} is close to the desired value. The power dissipation is minimized because of the recycled energy procedure during the down-tracking period. Therefore, the proposed PTE-BB converter simultaneously improves the voltage-tracking speed while extending the battery life.

B. PCC and VCC Methods for PTE-BB Converter

In the design of BB converter, it is difficult to maintain a low output voltage ripple when the value of V_{OUT} is close to that of V_{BAT}. If V_{BAT} is a little larger than V_{OUT}, the duty cycle of the buck operation would approaches nearly 100%, which is difficult to guarantee through the system control scheme because of the interference in duty modulation generated from the switching noise and the driver delay. Similarly, the duty cycle in the boost operation is also hard to approaches 0% when the value of V_{BAT} is a little smaller than that of V_{OUT}.

The current-sensing method in the current-mode control includes the PCC and VCC methods. If the VCC method is considered as the modulation method in the buck operation, the switching noise would have a serious influence on the duty modulation when V_{BAT} and V_{OUT} are nearly equal. Fig. 5(a) shows the instability caused by the switching noise effect in the buck operation with the VCC method, which leads to the increase of output voltage ripple. With the VCC method, the inductor starts to discharge through the positive trigger of the system clock V_{clk}. The switching noise results in the instability due to the short inductor discharging period, which is limited by the large duty cycle. The large output ripple worsens the supply quality

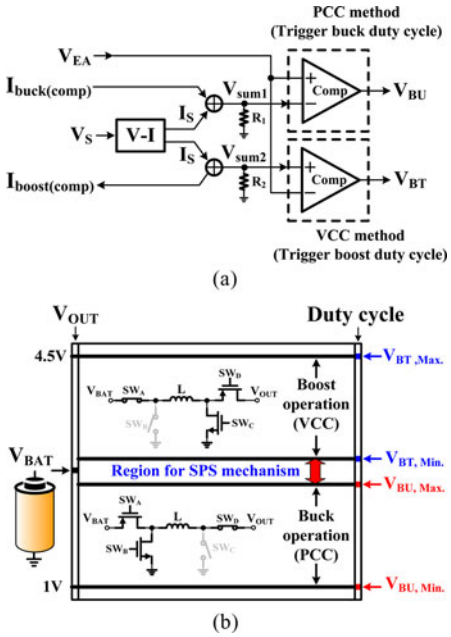

Fig. 6. (a) Control method decision circuit. (b) Indication of the PCC method, VCC method, and SPS mechanism with different input/output voltage conditions.

of the BB converter. In commercial products, the blanking time used in the current-sensing circuit can prevent the interference with the undesired switching noise, but it induces a minimum value for the duty cycle. This means that the blanking time restricts the BB converter to extend the duty cycle once the value of V_{BAT} is close to that of V_{OUT}. As a result, the PCC method is more suitable than the VCC method in the buck operation.

As V_{BAT} decreases, the operation changes from the buck operation to the boost operation when V_{BAT} becomes smaller than V_{OUT}. Thus, the duty cycle is reset from 100% to 0%. Fig. 5(b) shows the PCC method used in the boost operation. The switching noise causes system instability due to the short inductor charging period. The blanking time technique is also applied to solve the instability issue caused by the switching noise in high switching operation. However, it fails to work correctly once the duty cycle approaches 0%, indicating that the VCC method must be adopted in the boost operation.

C. Control Method Decision and SPS Mechanism

The BB converter aims to work properly with a small voltage difference between V_{BAT} and V_{OUT}. Nevertheless, the selection of either the PCC or VCC modulation methods determines the stability of BB converter shown in Fig. 5. The settling time of the voltage-tracking response may be extended due to the improper control method when the desired regulated voltage is set near V_{BAT} that deteriorates the performance of SoC systems. Thus, the proposed PTE-BB converter combines both the PCC and VCC methods in the buck and boost operations, respectively, to derive a stable operation in the wide input voltage range as well as a small output voltage ripple.

The control method decision circuit shown in Fig. 6(a) modulates the duty cycle from the error signal V_{EA}, the sensing signal

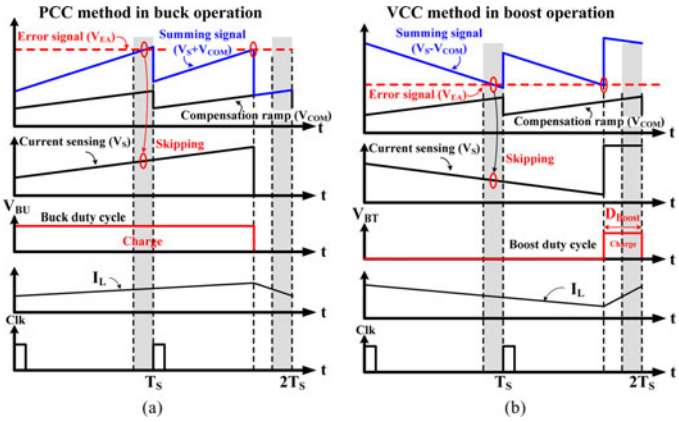

Fig. 7. Proposed PTE-BB converter uses the SPS mechanism. (a) PCC method in the buck operation. (b) VCC method in the boost operation.

V_S, and the slope compensation signal V_{COM}. V_{COM} is derived from the compensation currents, $I_{\mathrm{bcuk(comp)}}$ and $I_{\mathrm{boost(comp)}}$, in the buck and boost operations, respectively, to prevent subharmonic oscillation. Consequently, V_{BU} and V_{BT} can be used to trigger the buck and boost operations, respectively. As shown in Fig. 6(b), the PCC method operates in the buck operation because the VCC method suffers from the problem of having a short inductor discharging period if the value of V_{BAT} is close to that of V_{OUT}. Moreover, utilizing the VCC method in the boost operation is a better choice since the PCC method has a short inductor charging period when the low-duty cycle issue occurs.

The SPS mechanism depicted in Fig. 7 is utilized to extend the effective duty cycle, and thereby improving the regulation performance, minimizing the output voltage ripple, as well as eliminating the random transition between the two operations when the value of V_{BAT} is close to that of V_{OUT}. As a result, the power conversion efficiency can be enhanced. The PCC method in buck operation shown in Fig. 7(a) defines a 10% duty cycle at the end of a PWM switching cycle. When V_{BAT} decreases to reach V_{OUT} with an increasing duty cycle, the switching would be bypassed by means of prohibiting the inductor discharge period in order to extend the duty cycle. Therefore, the effective duty cycle is stretched so as to ensure the summing signal intersecting with the signal V_{EA} within the period of the 90% duty cycle at the next PWM switching cycle. It can alleviate the instability of the BB converter and the switching noise derived from the power stage. Similarly, as shown in Fig. 7(b), the VCC method in the boost operation is achieved with the SPS mechanism to regulate the output voltage if V_{BAT} continuously decreases to become much smaller than V_{OUT}. The effective duty cycle can be extended to overcome the challenge of low-duty condition. In addition, the mode transition would occur if the continuous counting of the skip number exceeds an auxiliary value, leading to the achievement of the optimal transition boundary in the proposed PTE-BB converter. The blanking time is also used in the current-sensing procedure to abate the effect resulted from the switching noise; this is because the SPS mechanism can extend the effective duty cycle in the PTE-BB converter. Given that the reduction of the switching period can

also improve the power conversion efficiency and guarantees the voltage regulation at the same time.

D. System Compensation in the PTE-BB Converter

The current-mode PTE-BB converter can be achieved using both the PCC and VCC methods. However, the system loop compensation network must be adjusted according to the distinct control methods. The control-to-output transfer function [27] of the PCC method in the buck operation $T_{\rm buck}$ is expressed as, as shown (1), at the bottom of this page, where $G_{\rm buck}$ is the loop gain, $M_{\rm buck}$ is the inductor current slope, and $M_{\rm comp\_buck}$ is the slope compensation signal. The current-mode control can separate the complex poles generated by the off-chip inductor and capacitor at power stage so as to derive only a single low-frequency pole $\omega_{p1(\rm buck)}$, which is load-dependent and inversely proportional to the output load resistance $R_{\rm LOAD}$ and the output capacitor $C_{\rm OUT}$. The first nondominant pole $\omega_{p2(\rm buck)}$ is located near to the switching frequency because of the current-mode control. The utilization of the slope compensation can determine the location of $\omega_{p2(\rm buck)}$. The equivalent series resistance (ESR) on the output capacitor also contributes a left-half plane (LHP) zero $\omega_{z(\rm buck)}$. The expressions of $\omega_{p1(\rm buck)}$, $\omega_{p2(\rm buck)}$, and $\omega_{z(\rm buck)}$ are expressed in (2). As a result, the PI compensator can be adopted to compensate the system in the PCC method buck operation:

$$\begin{aligned}\omega_{p1(\rm buck)} &= \frac{1}{C_{\rm OUT}R_{\rm LOAD}}\\ \omega_{p2(\rm buck)} &= \frac{M_{\rm buck}}{(M_{\rm buck}+M_{\rm comp\_buck})D_{\rm buck}T}\\ \omega_{z(\rm buck)} &= \frac{1}{R_{\rm ESR}C_{\rm OUT}}.\end{aligned} \tag{2}$$

In addition, the control-to-output transfer function of the VCC method in the boost operation $T_{\rm boost}$ is expressed as, as shown (3), at the bottom of this page, where $G_{\rm boost}$ is the loop gain. $M_{\rm boost}$ and $M_{\rm comp\_boost}$ are the inductor current slope and the slope compensation signal, respectively. Similarly, the current-mode control in the boost operation generates a load-dependent pole $\omega_{p1(\rm boost)}$ and a nondominant pole $\omega_{p2(\rm boost)}$ that are affected by the slope compensation. However, a right-half plane (RHP) zero is derived at the power stage in the boost operation, which deteriorates the system phase margin. However, it can be moved from RHP to LHP if the ESR on the output capacitor is carefully selected. Nevertheless, a large ESR, which may increase the output voltage ripple, is not suitable for SoC applications. Hence, a high-frequency RHP zero exists in the boost operation of the PTE-BB converter because the interference on the system bandwidth is alleviated by using the small off-chip inductor with high switching operation. The respective expressions of $\omega_{p1(\rm boost)}$, $\omega_{p2(\rm boost)}$, and $\omega_{z(\rm boost)}$ are shown as follows:

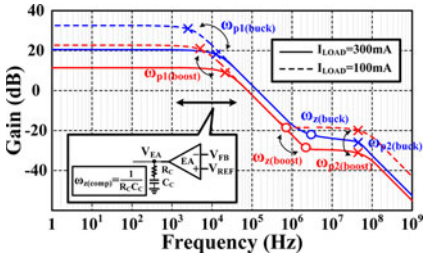

Fig. 8. Frequency response of the proposed PTE-BB converter with both the buck and boost operations under different load conditions.

$$\begin{aligned}\omega_{p1(\rm boost)} &= \frac{2}{C_{\rm OUT}R_{\rm LOAD}}\\ \omega_{p2(\rm boost)} &= \frac{M_{\rm boost}}{(M_{\rm boost}+M_{\rm comp\_boost})D_{\rm boost}T}\\ \omega_{z(\rm boost)} &= \\ &\frac{1}{(C_{\rm OUT}R_{\rm ESR}/(1-D_{\rm boost}))-(L/(1-D_{\rm boost})R_{\rm LOAD})}.\end{aligned} \tag{4}$$

The control-to-output frequency responses of the PTE-BB converter with the PCC method in buck operation and the VCC method in boost operation are shown in Fig. 8. The proposed dual-mode PI compensator can be used to achieve system compensation to ensure a large system bandwidth and an adequate phase margin.

$$\begin{aligned}T_{\rm buck}(s) &= G_{\rm buck}(s)\frac{1+sR_{\rm ESR}C_{\rm OUT}}{(1+sC_{\rm OUT}R_{\rm LOAD})\,(1+s(M_{\rm buck}+M_{\rm comp\_buck})D_{\rm buck}T/M_{\rm buck})}\\ &= G_{\rm buck}(s)\frac{1+(s/\omega_{z(\rm buck)})}{\left(1+(s/\omega_{p1(\rm buck)})\right)\left(1+(s/\omega_{p2(\rm buck)})\right)}\end{aligned} \tag{1}$$

$$\begin{aligned}T_{\rm boost}(s) &= G_{\rm boost}(s)\frac{1+s\,(C_{\rm OUT}R_{\rm ESR}/(1-D_{\rm boost})-L/(1-D_{\rm boost})R_{\rm LOAD})}{(1+s(C_{\rm OUT}R_{\rm LOAD}/2))\,(1+s(M_{\rm boost}+M_{\rm comp\_boost})D_{\rm boost}T/M_{\rm boost}))}\\ &= G_{\rm boost}(s)\frac{1+s/\omega_{z(\rm boost)}}{\left(1+(s/\omega_{p1(\rm boost)})\right)\left(1+(s/\omega_{p2(\rm boost)})\right)}\end{aligned} \tag{3}$$

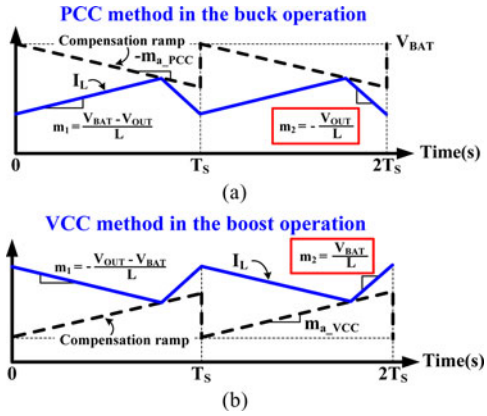

Fig. 9. Slope compensation (a) in the buck operation with the PCC method and (b) in the boost operation with the VCC method.

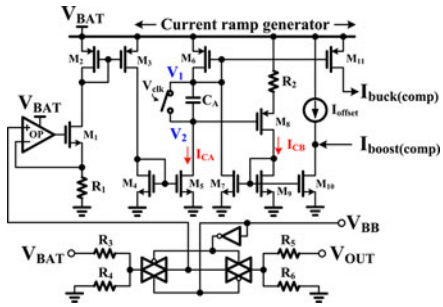

Fig. 10. Schematic of the DSC circuit.

IV. Circuit Implementation

A. DSC Circuit

Slope compensation is required to prevent subharmonic oscillation, and thereby ensuring system stability when the duty cycle in the current-mode control is larger than 50%. To compensate for the PCC and VCC methods in the buck and boost operations, respectively, two distinct slope compensation signals were utilized in the proposed PTE-BB converter. The slope compensation schemes for the PCC and VCC methods are shown in Fig. 9(a) and (b), respectively. The slope compensation coefficient m_{a_PCC} for the PCC method must be proportional to V_{OUT} in the buck operation. On the other hand, V_{BAT} is proportional to the slope compensation coefficient m_{a_VCC} for the VCC method in the boost operation. As a result, the proposed DSC circuit can generate the slope compensation coefficient, which is adjusted by the V_{BAT} and V_{OUT} for the PCC and VCC methods, respectively. It can minimize the interference on the bandwidth of the current loop resulted from the variations of V_{BAT}, V_{OUT}, or the switching noise.

Fig. 10 shows the DSC circuit, which generates the slope compensation signal according to the different operation modes. The voltage-to-current (V–I) converter consisting of the operational amplifier M_1 and the resistor R_1 converts the current I_{CA} using V_{OUT} and V_{BAT} in the PCC method of the buck operation and the VCC method of the boost operation, respectively. V_{clk} resets the charge on the capacitor C_A when it is set to high at the beginning of every switching cycle. When V_{clk} is set to low, I_{CA} starts to charge the capacitor C_A, which carries out a sawtooth waveform at node V_2. The voltage across the capacitor C_A is approximately equal to the voltage across the resistor R_2 since the source–gate voltages of M_6 and M_8 are approximately equal. Hence, the MOSFET M_8 and the resistor R_2 form another V–I converter to generate a sawtooth current I_{CB}. In the PCC method of the buck operation, the slope compensation signal $I_{\mathrm{buck(comp)}}$ is derived from the current mirror structure I_{CB} which is proportional to V_{OUT} owing to the wide range duty cycle, as follows:

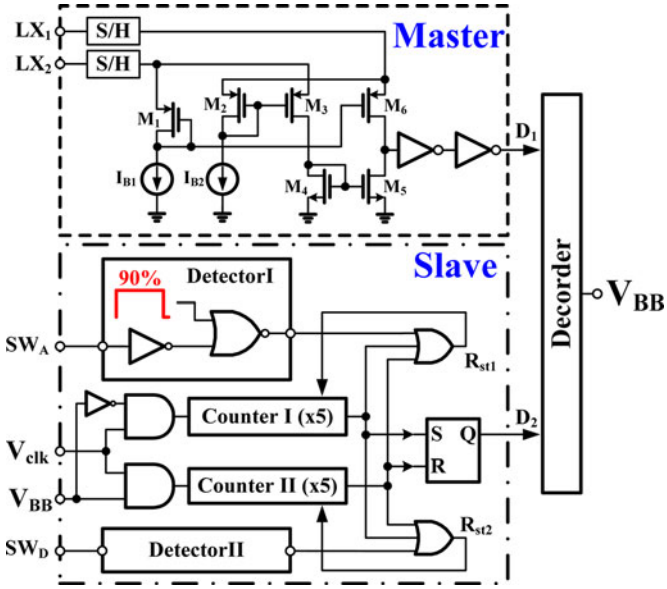

Fig. 11. Schematic of the mode detector circuit with the SPS mechanism.

$$I_{\mathrm{buck(comp)}} = I_{\mathrm{CB}} = \frac{R_6}{(R_5 + R_6)} \cdot \frac{V_{\mathrm{OUT}} \cdot \Delta t}{R_1 \cdot R_2 \cdot C_A}. \quad (5)$$

Similarly, to achieve the system slope compensation, I_{CA} must be proportional to V_{BAT} in the VCC method of the boost operation. Thus, the slope compensation signal $I_{\mathrm{boost(comp)}}$ is derived as

$$I_{\mathrm{boost(comp)}} = I_{\mathrm{offset}} - \frac{R_4}{(R_3 + R_4)} \cdot \frac{V_{\mathrm{BAT}} \cdot \Delta t}{R_1 \cdot R_2 \cdot C_A}. \quad (6)$$

In addition, as I_{CA} increases, the voltage V_2 decreases due to the discharge of capacitor C_A. Thus, the compensation currents, $I_{\mathrm{buck(comp)}}$ and $I_{\mathrm{boost(comp)}}$, would increase and decrease, respectively, so as to dynamically adjust the slope compensation signal to improve the system response.

However, at the moment of transition between the buck and boost operations, the output voltage ripple may be increased because of the different operation modes. The slope compensation signal is added to the current-sensing signal in the PCC method, but is subtracted to the current-sensing signal in the VCC method owing to the opposite duty modulation scheme in order to achieve a stable current-mode operation. Thus, a voltage gap is realized, in which the summing signal becomes discontinuous and causes an abnormal operation and large output voltage ripple at the mode transition point. To achieve a smooth mode transition, the offset current I_{offset}, as defined in (7), is

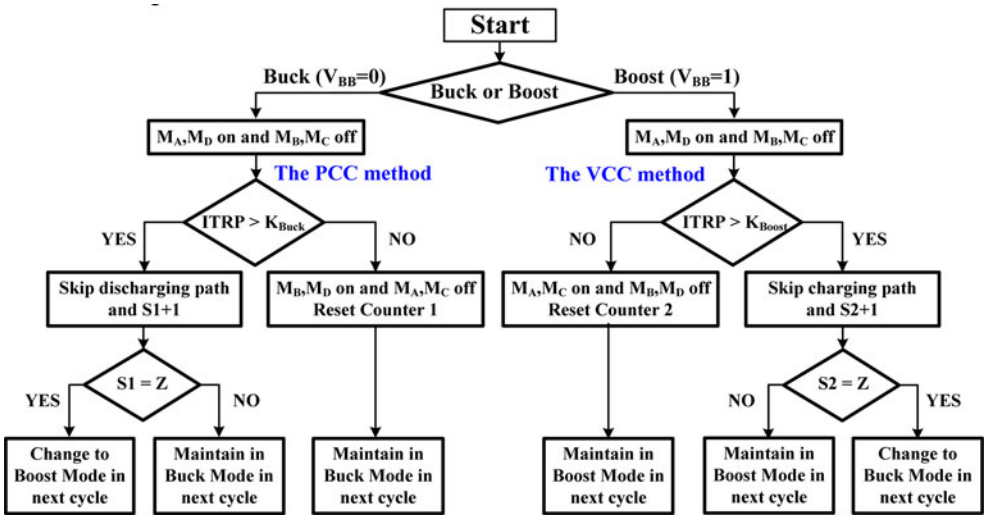

Fig. 12. Flow chart of the SPS mechanism in the proposed PTE-BB converter.

introduced to reduce the output voltage variation [28]. I_{offset} depends on the input and output voltages, which is adopted in the DSC circuit. The summing coefficients, k_1 and k_2, are proportional to V_{OUT} and V_{BAT}, respectively:

$$I_{\text{offset}} = k_1 V_{\text{OUT}} + k_2 V_{\text{BAT}} = \frac{R_6}{(R_5 + R_6)} \cdot \frac{V_{\text{OUT}}}{R_1} + \frac{R_4}{(R_3 + R_4)} \cdot \frac{V_{\text{BAT}}}{R_1}. \quad (7)$$

B. Mode Detector Circuit

The mode detector circuit with the SPS mechanism shown in Fig. 11 is implemented to determine either the buck or the boost operation according to the relationship between V_{BAT} and V_{OUT}. To achieve an accurate mode transition between the two operations over a wide load range for minimizing output voltage ripple, the on-resistance R_{SW} of each power MOSFET must be considered. Consequently, the theoretical boundary condition of the mode transition is depicted in

$$V_{\text{BAT}} - 2(I_{\text{load}} \times R_{\text{SW}}) = V_{\text{OUT}}, \qquad \text{if } \text{LX}_1 = \text{LX}_2. \quad (8)$$

The operation of the mode transition is divided into the master and the slave controls. The master control works when V_{BAT} and V_{OUT} differ significantly from each other, operating with the simultaneous on state of power switches, *A* and *D*, and deciding the operation mode by comparing LX_1 and LX_2 directly. The two pairs of common-gate amplifiers form a comparator that realizes a push–pull stage at its output node in order to enhance the transient speed.

The slave controller consists of two counters and logic gates to improve the transition accuracy through the pulse-skip function when the value of V_{BAT} is extremely close to that of V_{OUT}. Unlike some prior arts including the BB mode as a buffer operation for smooth mode transition, the proposed SPS mechanism can skip energy paths automatically to extend the effective duty cycle to overcome the boundary condition in the BB converter over a wide voltage range.

In the buck operation, a pulse signal defined as 90% of the whole PWM duty cycle is triggered by the system clock V_{clk}. *Counter I* calculates the number of skipping pulses to determine the mode transition for power saving. *Detector I* would output a reset pulse signal, which is derived from the NOR operation of the control signal SW_A and the 90% duty cycle when the buck duty cycle exceeds the effective value to enable *Counter I* to prepare for mode transition. As a result, the PTE-BB converter switches from the buck operation to the boost operation when the number of skipping pulses exceeds the designed value. Similarly, the operation in the boost operation is also controlled by the same mechanism controlled by the *Detector II* and *Counter II*. It can also ensure the smooth mode transition when the value of V_{BAT} is extremely close to that of V_{OUT}. The flow chart of the SPS mechanism is depicted in Fig. 12. The variable ITRP represents the interconnection of the error signal and the summing signal. The 90% duty cycle in the PCC method of the buck operation and the VCC method of the boost operation are represented by K_{Buck} and K_{Boost}, respectively. The variable *Z* is the designed value in the counter that determines the activity of mode transition between the buck and the boost operations.

C. Current-Sensing Circuit

A simple way of current sensing is achieved by inserting the sensing resistor into the series of the inductor current path. However, the efficiency is seriously deteriorated at the heavy load conditions. The proposed current-sensing circuit depicted in Fig. 13 can reduce unnecessary power loss without using power-dissipated sensing resistor.

The transistor M_S produces the sensing current I_{sense} during the turn-on period of the power switch M_A. The source-to-drain voltages of M_A and M_S are approximately equal because of the implementation of the common-gate amplifier, which is composed of M_3–M_7. M_1 is ON and M_2 is OFF during the turned-on period of M_A. Bias current I_B results in the current difference between the sensing currents, I_{sense} and I_{sense1}. To enhance the current-sensing accuracy, transistor M_9, which has the same

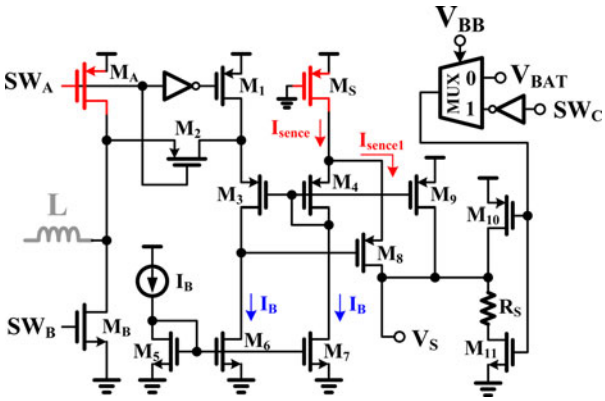

Fig. 13. Schematic of the current-sensing circuit.

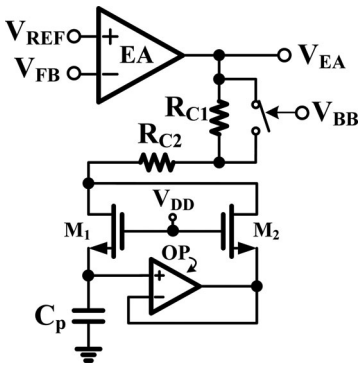

Fig. 14. Dual-mode PI compensator.

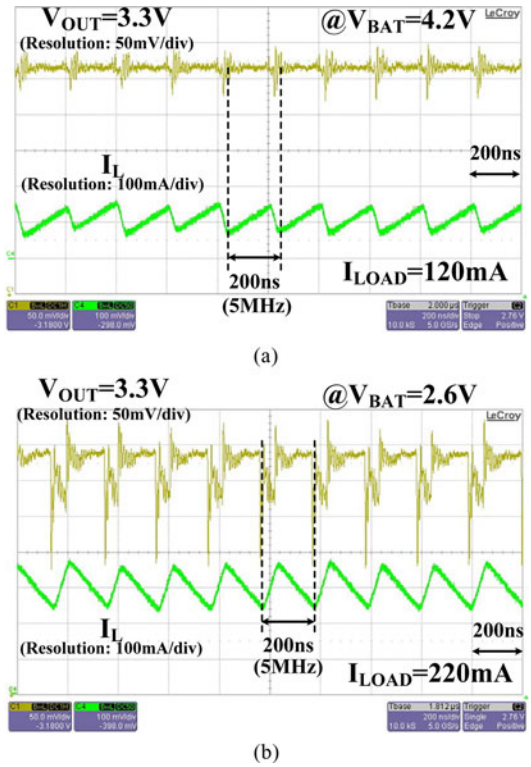

Fig. 15. Measured steady-state operation of the PTE-BB converter. (a) Buck operation with load current of 120 mA when $V_{\mathrm{BAT}} = 4.2$ V and $V_{\mathrm{OUT}} = 3.3$ V. (b) Boost operation with load current of 220 mA when $V_{\mathrm{BAT}} = 2.6$ V and $V_{\mathrm{OUT}} = 3.3$ V.

aspect ratio as the current mirror structure of M_3 and M_4, is added to provide a compensative current I_B. Consequently, the current-sensing signal is produced by the voltage signal V_S across the resistor R_1. On the other hand, V_S would be reset to V_{BAT} by the multiplexer and the MOSFETs M_{10} and M_{11} at the charging period of the boost operation to achieve the VCC method.

D. Dual-Mode PI Compensator

As shown in Fig. 14, the proposed internal dual-mode PI compensator can maintain a stable closed-loop response in both the buck and boost operations compared with a conventional PI compensator [26]. The capacitor multiplier technique utilized to on-chip compensation achieves with only a small capacitor C_p that reduces the silicon area [29]. It generates the system dominant pole to ensure stability in both the buck and boost operations. In addition, when the PTE-BB converter operates in the PCC method of the buck operation, the switch is turned off to generate a low-frequency compensation zero to cancel the effect of the system pole $\omega_{p1(\mathrm{buck})}$. Aside from this, the system load dependent pole in the boost operation $\omega_{p1(\mathrm{boost})}$ moves to higher frequencies compared with the buck operation under the same output load condition. The V_{BB} signal forces the switch on in order to reduce the compensation resistance at the PI compensator. This means that the compensation zero in the boost operation is tracked to the higher frequencies in order to achieve the pole-zero cancellation for improving system stability. Thus, in both the buck and boost operations, the proposed dual-mode PI compensator carries out the same crossover frequency to achieve better performance even at the mode transient period.

V. Experimental Results

The proposed PTE-BB converter with F-DVS function was fabricated by 0.25-μm CMOS process. Supply voltage V_{BAT} is set in the range of 2.5–4.5 V defined by the range of Li-ion battery. The typical output voltage is 3.3 V, regulated by the switching frequency of 5 MHz so that the off-chip inductor and capacitor can be utilized with 1 μH and 0.88 μF, respectively. The small-size off-chip output filter can minimize the volume of the power module in portable devices. Fig. 15 shows the steady-state operation of the proposed PTE-BB converter. The regulated output voltage of 3.3 V under 4.2 V input voltage supply with a 120-mA load current is shown in Fig. 15(a). The switching frequency is kept at 5 MHz with a duty cycle of 78%. The boost operation is demonstrated in Fig. 15(b) with a regulated output voltage of 3.3 V under input voltage of 2.6 V. With duty cycle of 21% and 220-mA load current, the 5-MHz high switching operation is achieved.

Fig. 16 shows the SPS mechanism in the buck operation with the PCC method. When V_{BAT} is close to V_{OUT} in the PTE-BB converter, the SPS mechanism can ensure the smooth transition response and avoid system instability resulting from high switching noise. When V_{BAT} is lowered to 3.5 V with a fixed V_{OUT} of 3.3 V as shown in Fig. 16(a), the SPS mechanism

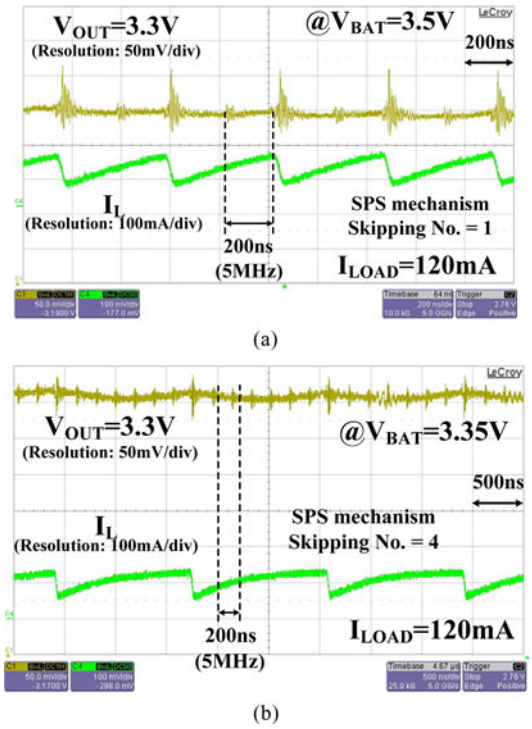

Fig. 16. Measured SPS mechanism in the buck operation with load current of 120 mA. (a) If $V_{\mathrm{BAT}} = 3.5$ V and $V_{\mathrm{OUT}} = 3.3$ V, the skipping number is 1. (b) If $V_{\mathrm{BAT}} = 3.35$ V and $V_{\mathrm{OUT}} = 3.3$ V, the skipping number is 4.

is activated to skip the switching numbers at the power stage in order to extend the effective duty cycle. At this time, the PTE-BB converter operates in the transition region from the buck operation to the boost operation. Similarly, if the V_{BAT} further decreases to 3.35 V as shown in Fig. 16(b), the number of the skip operation is increased during every effective switching cycle. Thus, the stable operation of the proposed high switching PTE-BB converter is guaranteed, and an adequate duty cycle is derived when the value of V_{BAT} is close to that of V_{OUT}.

Fig. 17 shows the SPS mechanism in the boost operation with the VCC method. The switching number is decreased when the PTE-BB converter enters the transition region from the boost operation to the buck operation. The smaller voltage difference between V_{BAT} and V_{OUT} is derived, the more skipping number of the SPS mechanism is achieved. The equivalent duty cycle can yield the correct operation for the high switching PTE-BB converter. If the skipping number exceeds the defined value in the mode detector circuit, the operation mode can be switched from the boost operation to the buck operation in order to achieve a smooth transition response and enhance efficiency.

Fig. 18 shows the F-DVS function for the SoC system. The up-tracking response shown in Fig. 18(a) demonstrates that V_{OUT} arises from 2 to 3 V with the settling time of 20 μs. The signal V_{control}, which is generated by the DAC according to the demand from processor in the SoC, activates the tracking response for F-DVS function. The maximum charging current control works in both pure buck and boost operations. It helps regulate the inductor peak current and avoid the overcharge at the up-tracking response. Fig. 18(b) shows the down-tracking response when

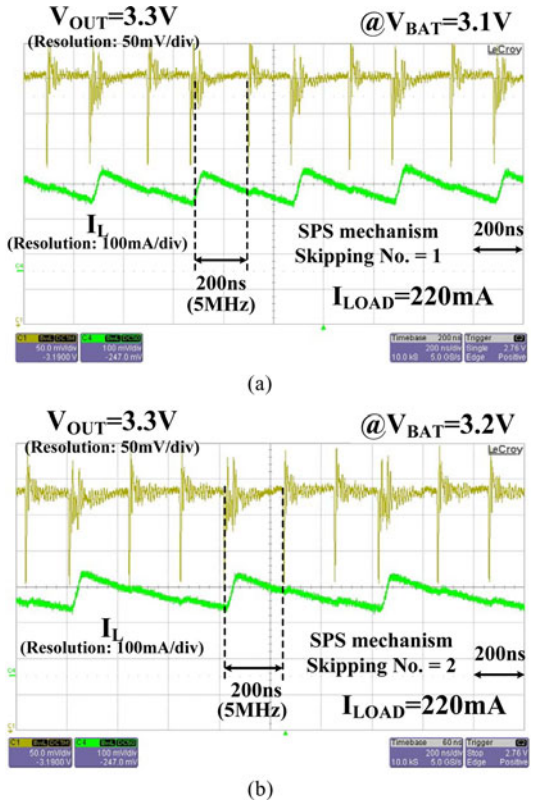

Fig. 17. Measured SPS mechanism in the boost operation with load current of 220 mA. (a) If $V_{\mathrm{BAT}} = 3.1$ V and $V_{\mathrm{OUT}} = 3.3$ V, the skipping number is 1. (b) If $V_{\mathrm{BAT}} = 3.2$ V and $V_{\mathrm{OUT}} = 3.3$ V, the skipping number is 2.

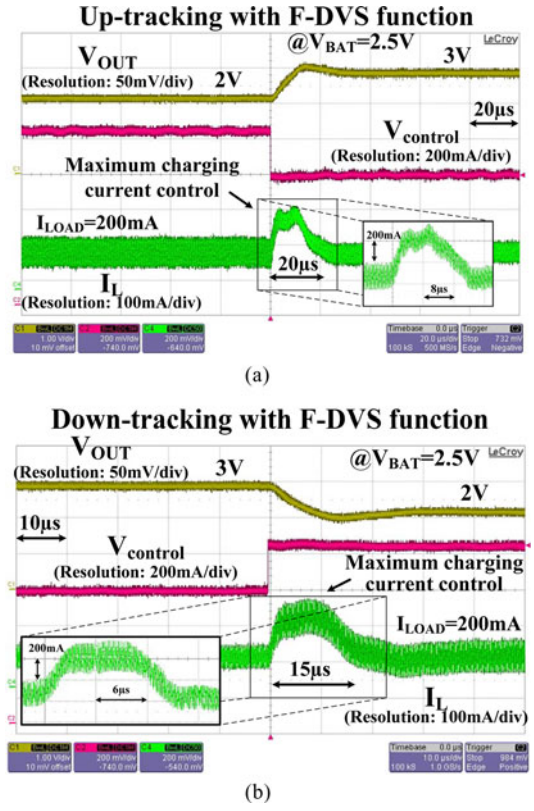

Fig. 18. Measured F-DVS function. (a) Up-tracking response. (b) Down-tracking response.

TABLE I
DESIGN SPECIFICATIONS OF THE PROPOSED PTE-BB CONVERTER

Technology	0.25 μm CMOS process
Inductor / DCR	1 μH / 100 mΩ (nominal)
Capacitor / ESR	0.88 μF / 50 mΩ (nominal)
Switching frequency	5 MHz
Input voltage (V_{BAT})	2.5 V – 4.5 V
Output voltage (V_{OUT})	2 V – 4 V
Load current range (I_{LOAD})	100 mA – 400 mA
Up-tracking (from 2 V to 3 V)	20 μs
Down-tracking (from 3 V to 2 V)	15 μs
Power conversion efficiency	Max. 91 %
Chip size	4.86 mm^2

TABLE II
COMPARISON OF THE PREVIOUS BB CONVERTER METHODOLOGIES

	This work	[1]	[10]	[14]
Technology	0.25 μm CMOS	Discrete components	0.25 μm CMOS	0.35 μm CMOS
Control scheme	Current-mode	Voltage-mode	Voltage-mode	Tri-mode
Inductor	1 μH	2.2 μH	4.7 μH	10 μH
Capacitor	0.88 μF	47 μH	47 μH	10 μH
Switching frequency	5 MHz	500 kHz	700 kHz	250 kHz*
Input voltage	2.5 V – 4.5 V	2.4 V – 3.4 V	2.7 V – 4.5 V	1.6 V – 3.3 V
Output voltage	2 V – 4 V	0.4 V – 4 V	3.3 V (nominal)	0.9 V – 3 V
Max. load current	400 mA	800 mA	500 mA	800 mA
Up-tracking	20 μs/V	N / A	N / A	150 μs/V
Down-tracking	15 μs/V	N / A	N / A	37 μs/V
Peak efficiency	91 %	62 %	96 %	96.5 %
Chip size	4.86 mm^2	N / A	3.14 mm^2	1.3 mm^2

* Switching frequency would vary according to the inductor current i_L in tri-mode control.

$V_{\rm OUT}$ decreases from 3 to 2 V with a settling time of 15 μs. The measured inductor current waveform indicates the work of reversed buck and boost operations to accelerate the tracking response. Additionally, the recycled energy procedure during the down-tracking period minimizes the power dissipation in the proposed PTE-BB converter.

Fig. 19 shows the chip micrograph and the prototype of the proposed PTE-BB converter. The occupied silicon area is about 4.86 mm^2 owing to the use of six power switches to achieve the F-DVS operation for the SoC system. Fig. 20 shows the measured output voltage ripple with different skipping numbers when the value of $V_{\rm BAT}$ is close to that of $V_{\rm OUT}$. The maximum skip number in the SPS mechanism is five in the proposed design. The output ripple in both the buck and boost operations is derived below the allowable value for improving the performance of the SoC system. Fig. 21 shows the power conversion efficiency with a peak value of 91%. The SPS mechanism skips the switching cycle in the mode transition period to extend the equivalent duty cycle, and thereby enhancing the power conversion efficiency. When $V_{\rm BAT}$ is very close to $V_{\rm OUT}$, the SPS mechanism can even achieve an almost direct conduction from $V_{\rm BAT}$ to $V_{\rm OUT}$. Thus, the switching number of power stage is reduced that the peak efficiency can be derived shown in Fig. 21. However, owing to the nonideal power loss, such as the conduction loss, in power stage, the actual mode transition point between the buck and the boost modes would become larger than that of the ideal value. Therefore, the measured peak efficiency of the proposed

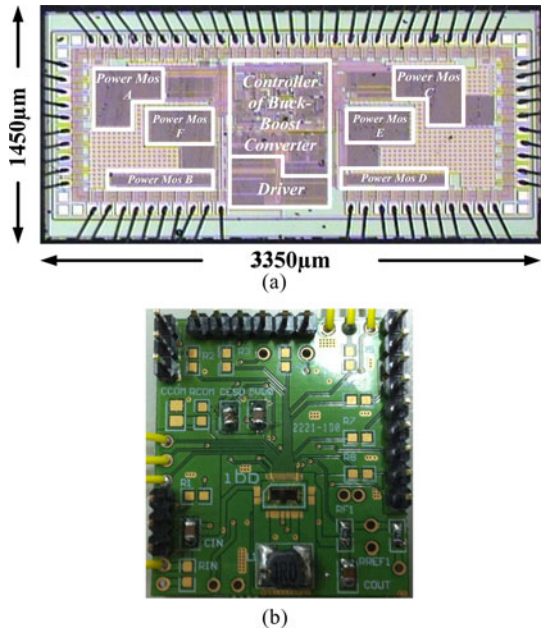

Fig. 19. (a) Chip micrograph. (b) Prototype of the proposed PTE-BB converter.

PTE-BB converter with $V_{\rm OUT} = 3.3$ V is derived at $V_{\rm BAT} = 3.6$ V, rather than that at $V_{\rm BAT} = 3.3$ V. The detailed design specifications are listed in Table I. Moreover, the comparisons of the prior BB converters are shown in Table II. The proposed

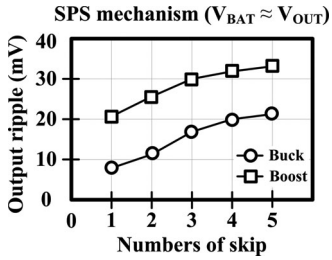

Fig. 20. Measured output voltage ripple with different skipping numbers in SPS mechanism.

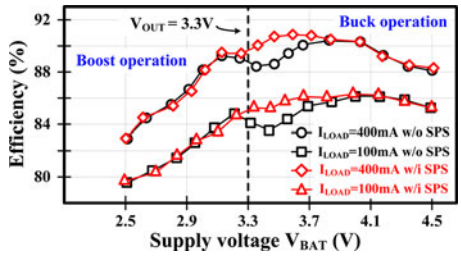

Fig. 21. Measured power conversion efficiency of the proposed PTE-BB converter.

PTE-BB converter with the current-mode control can achieve the F-DVS operation, which is suitable for the SoC system.

VI. Conclusion

The proposed high switching current-mode PTE-BB converter with F-DVS function was fabricated by 0.25-μm CMOS process. To effectively power the SoC system, the F-DVS function rapidly adjusts the output voltage value to meet the different power request. In addition, when a small voltage difference exists in V_{BAT} and V_{OUT}, the utilization of the PCC and VCC methods in the buck and boost operations, respectively, can eliminate the system instability caused by switching noise to ensure a stable voltage regulation. Moreover, compared with the traditional method, the SPS mechanism helps to extend the effective duty cycle using pulse skipping to obtain a regulated output voltage in mode transition and enhance power conversion efficiency. The DSC circuit and the dual-mode PI compensator are proposed to stabilize the system in both buck and boost operations. The fast-tracking response and the recycling energy are achieved in the F-DVS function with a switching frequency of 5 MHz.

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