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Electromigration Failure Mechanism in Sn-Cu Solder Alloys with OSP Cu Surface Finish

MING-HUI CHU,[1] S.W. LIANG,[1] CHIH CHEN,[1,3,4] and ANNIE T. HUANG[2]

1.—Department of Materials Science and Engineering, National Chiao Tung University, Hsin-chu 30010, Taiwan. 2.—Research Center for Applied Sciences, Academia Sinica, Taipei 11529, Taiwan. 3.—e-mail: chihchen98@yahoo.com. 4.—e-mail: chih@cc.nctu.edu.tw

Organic solderable preservative (OSP) has been adopted as the Cu substrate surface finish in flip-chip solder joints for many years. In this study, the electromigration behavior of lead-free Sn-Cu solder alloys with thin-film under bump metallization and OSP surface finish was investigated. The results showed that severe damage occurred on the substrate side (cathode side), whereas the damage on the chip side (cathode side) was not severe. The damage on the substrate side included void formation, copper dissolution, and formation of intermetallic compounds (IMCs). The OSP Cu interface on the substrate side became the weakest point in the solder joint even when thin-film metallization was used on the chip side. Three-dimensional simulations were employed to investigate the current density distribution in the area between the OSP Cu surface finish and the solder. The results indicated that the current density was higher along the periphery of the bonding area between the solder and the Cu pad, consistent with the area of IMC and void formation in our experimental results.

Key words: Electromigration, solder joints

INTRODUCTION

Electromigration failure of solder joints induced by high current density has been an important reliability issue in flip-chip packaging. Organic solderable preservative (OSP) surface finish has been extensively used in fabrication of flip-chip solder joints due to its many advantages including low cost, smooth interface, high bonding strength, low contamination, and ease of fabrication.[1,2] In addition, electromigration has become a critical reliability issue in flip-chip solder joints as the current density applied in them continues to increase.[3] Many efforts have been made to investigate the electromigration behavior of solder joints.[4–7] However, there are few studies addressing electromigration in solder joints with OSP Cu finish. Therefore, we focus on the failure mechanism in OSP Cu surface finish. In general, past studies paid more attention to damage in the under bump metallization (UBM) near the chip side, because this has been the predominant factor causing open circuits in solder joints. In these cases, electromigration failure was induced by current crowding,[8–11] which generated problems involving void formation and consumption of Cu UBM. In comparison with the chip side, the change of the microstructure on the substrate side had not seemed as critical. However, in our case, we found that the damage on the substrate side was considerably more serious.

When using tin-lead solder, OSP Cu surface finish has longer lifetime than Au/Ni.[12] The mean time to failure of solder joints with OSP Cu surface finish was six times that of Au/Ni surface finish.

In this study, when OSP and copper were used instead of electroless Ni/Cu metallization on the substrate side, we found that the failure on the substrate side was more serious than on the chip side after current stressing. The damage on the chip side was slight, and there was very little change of microstructure. These results were very different

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from what we have seen in the past. Three-dimensional (3D) finite-element analysis was employed to simulate the distribution of the current density in the solder joints, and the simulation results were able to explain the experimental observations of the failure sites.

EXPERIMENTAL PROCEDURES

99.3Sn-0.7Cu flip-chip solder joints were used for the electromigration test. The presolder was Sn-3.0Ag-0.5Cu alloy. The passivation/UBM opening diameter on the chip side was 90 μm/112 μm. The bump height was 112 μm. The UBM thin films on the chip side were Al ($\sim$0.3 μm)/Ni(V) ($\sim$0.3 μm)/Cu ($\sim$0.7 μm) as deposited by sputtering. The bond-pad metal layers on the substrate side were OSP Cu.

Solder joints were stressed with 0.8 A, 1.3 A, and 1.5 A current on a hot plate at 150°C. The current densities were 3.7 A/cm^2, 6.4 A/cm^2, and 7.4 $\times$ 10^4 A/cm^2, respectively, calculated based on the passivation opening diameter. The temperature increased due to the Joule heating effect by 17°C, so the temperature in the solder joint remained much lower than the melting point of 99.3Sn-0.7Cu (227°C). We used an infrared microscope to obtain the real temperature of the solder joints during current stressing. After current stressing, solder joints were polished to the middle of the bumps by using SiC papers and Al_2O_3 powders. We examined the microstructure change on the cross-section of the solder joints by scanning electron microscopy (SEM).

SIMULATIONS

In addition, finite-element analysis was used in this study to explain the failure mechanism of OSP Cu on the substrate side in the lead-free solder joints.[13] Three-dimensional models were established to simulate the current density distribution during current stressing in this study. A simplified UBM structure with opening diameter of 110 μm was used. The diameter of the contact opening on the substrate side was 175 μm. The dimensions of the Al trace were 65 μm wide and 1.5 μm thick, whereas the Cu line on the substrate side was 65 μm wide and 15 μm thick. The intermetallic compound (IMC) formed between the UBM and the solder was also considered in the simulation models. The electroplated Cu layer was assumed to consume 0.5 μm and to form 1.4 μm of Cu_6Sn_5 IMC. Layered IMCs were used in this simulation for both Cu_6Sn_5 and Ni_3Sn_4 to avoid meshing difficulties. In addition, eutectic Sn-Cu solder was used in this model. The resistivity values of the materials used in the simulation are listed in Table I. The effect of the temperature coefficient of resistivity (TCR) was considered, and the TCR values for the metals are also listed in Table I.

The model used in this study was based on SOLID69 eight-node hexahedral coupled field elements in ANSYS simulation software. The current applied in the simulation was 1.0 A.

RESULTS AND DISCUSSION

SEM images of solder joints after current stressing of 1.5 A at 150°C for 140 h are shown in Fig. 1. The solder bump in Fig. 1a had an upward electron flow. Damage is clearly observed around the Cu pad/solder interface. We could see that voids were formed at the edge of the solder joint and along the IMCs and the Cu pad because Cu atoms migrated due to the electron

Table I. The electrical properties of materials used in the simulation models

Materials	Resistivity at 20°C ($\mu\Omega$-cm)	TCR ($\times 10^{-3}$/K)
Al trace	2.7	4.2
Cu	1.7	4.3
Eutectic Sn-Cu	14.6	4.4
Cu_6Sn_5	17.5	–
Ni_3Sn_4	28.5	–

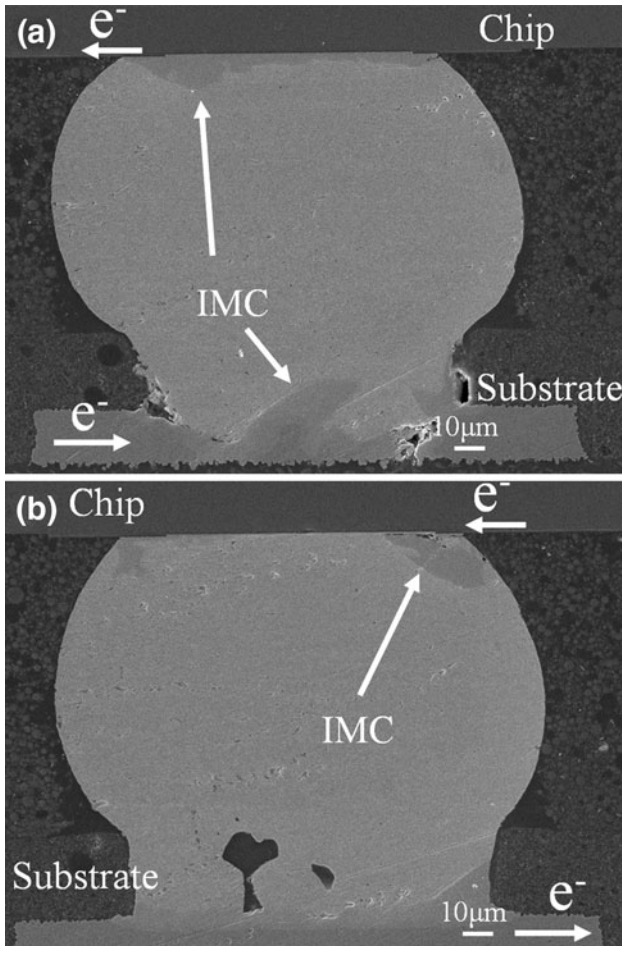

Fig. 1. SEM images of solder joints stressed with 1.5 A at 150°C for 140 h with (a) upward and (b) downward electron flow.

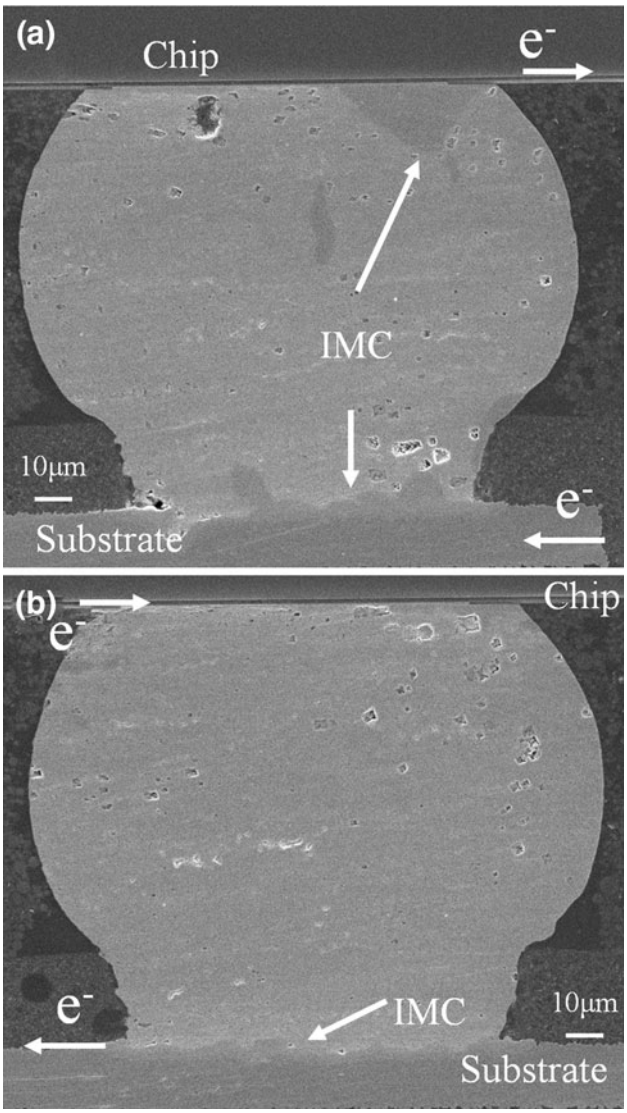

Fig. 2. SEM images of solder joints stressed with 0.7 A at 150°C for 480 h with (a) upward and (b) downward electron flow.

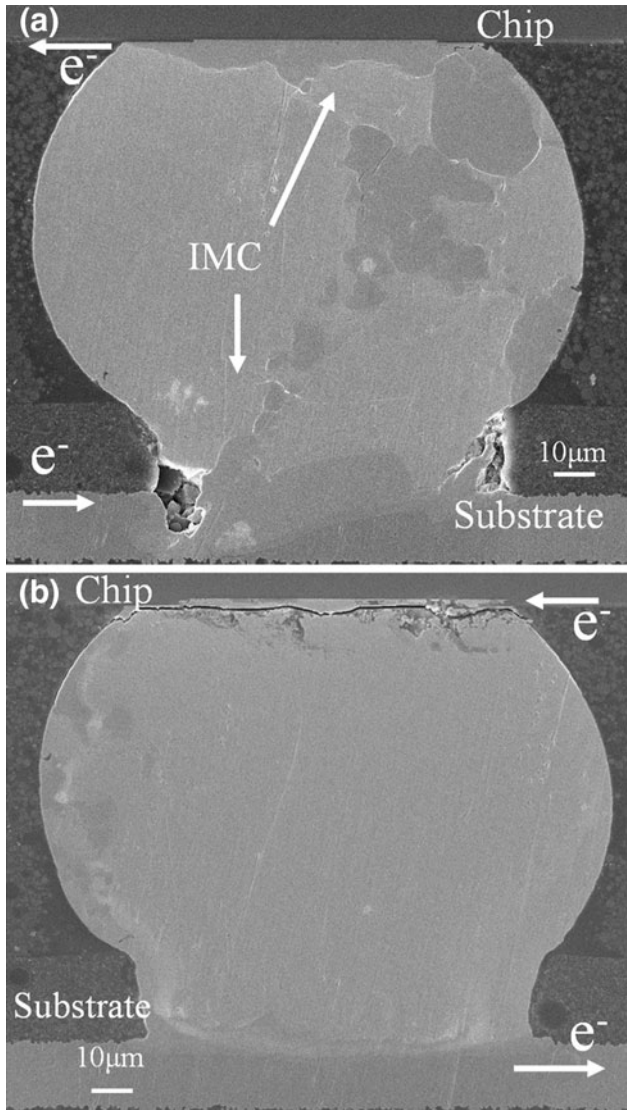

Fig. 3. SEM images of solder joints stressed with 0.8 A at 150°C for 552 h with (a) upward and (b) downward electron flow.

flow into the solder to form Cu-Sn IMCs. A large amount of Cu was consumed, and Cu_6Sn_5 IMC formed on both the chip and substrate sides. On the contrary, the solder bump in Fig. 1b with a downward electron flow shows no obvious failure, and the Cu stayed intact. The large voids in the solder on the substrate side may be attributed to defect voids formed during the reflow process, not due to electromigration. In addition, minimal IMC formation was observed on both sides, and only a small void was found at the upper right-hand corner of the solder bump. In general, the failure mode of the solder joint with thin-film UBM on the chip side has always been void formation at the current-crowding region in the UBM. The void propagated as current stressing continued and ultimately caused solder joint failure.[14,15] In this study, the void near the chip side was not the primary damage in the solder joint; on the contrary, the damage near the substrate side was the major issue. Figure 2 shows SEM images of solder joints that have been stressed with 0.7 A at 150°C for 480 h. The results reveal similar microstructure changes as in the solder joints with 1.5 A current stressing. The solder bump shown in Fig. 2a had void formation at the lower left-hand corner, and IMCs were formed at both the substrate and chip sides. The solder joint in Fig. 2b with a downward electron flow again showed almost no microstructure change. In these two cases, the current densities were 7.4×10^4 A/cm^2 and 3.5×10^4 A/cm^2 for stressing currents of 1.5 A and 0.7 A, respectively. From these results, void formation primarily appeared at the substrate side in the solder bump with an upward electron flow under both high and low current density. Figure 3a also shows clear damage near the substrate side. This sample was also stressed with low current, and in this image, the solder bump shown in Fig. 3b has a different microstructure. The

crack observed was due to mechanical polishing; however, the Al trace had disappeared and was replaced by IMCs with Sn. Failure resulted from dissolution of the Ni(V) layer induced by electromigration. The difference in the two microstructure changes for the two low-current-density cases provides evidence of dual failure modes; that is, damage occurred not only on the Cu pad on the substrate side but also on the UBM on the chip. Serious crowding takes place on the chip side, and the electromigration failure occurs mainly on the chip side due to this serious flux divergence.[8–11] However, when OSP Cu is adopted as the surface finish on the substrate side, the dissolution rate of Cu into the solder is very fast upon current stressing.[16–18] In the present study, the UBM on the chip-side is Ni(V)/Cu and the metallization on the substrate side is Cu. The dissolution rate of Cu into the solder is faster than that of Ni. Therefore, the substrate side is also vulnerable to electromigration damage, although there is no serious current crowding on the substrate side. Ke et al.[17] also reported that electromigration damage can also happen in OSP Cu, and they also provided a theoretical interpretation for the Cu dissolution. The combination of both modes could then result in solder joint failure. The other important finding was that we still saw no obvious void formation near the chip side in each case.

The above-mentioned results can be explained based on the results of the 3D simulations. Figure 4a shows the simulation results for the current density distribution in two solder joints connected by an Al trace. A serious current-crowding effect occurs in the solder bumps connecting to the wiring Al trace on the chip side. Figure 4b depicts a cross-sectional view of the distribution of the current density. The maximum current density in the solder joints was 2.81×10^5 A/cm^2, at the solder region near the entrance point of the Al trace on the chip side. From this picture, the current densities at the two opposite bottom edges (right-hand corner and left-hand corner) of the left-hand solder joint with upward electron flow were 1.37×10^4 A/cm^2 and 9.88×10^3 A/cm^2, respectively. We can also clearly see that the current density at these edges of the solder joint was higher than for other areas inside the solder joint on the substrate side. The current density ratio of the two edges on the chip side is large, whereas that of the two bottom edges is merely a twofold difference. From the simulation results, the current density of the whole Cu pad was higher than for the adjacent solder bump. It seems that electrons distributed evenly on the Cu pad first, then flowed into the solder bump. This phenomenon can be attributed to the lower Cu resistivity and larger Cu pad area compared with the contact area with the solder joint. The resistivities of Cu and Sn are 1.7 $\mu\Omega$ cm and 12.3 $\mu\Omega$ cm, respectively, almost one order of magnitude different. To calculate the resistance of the Cu pad and the solder bump, we

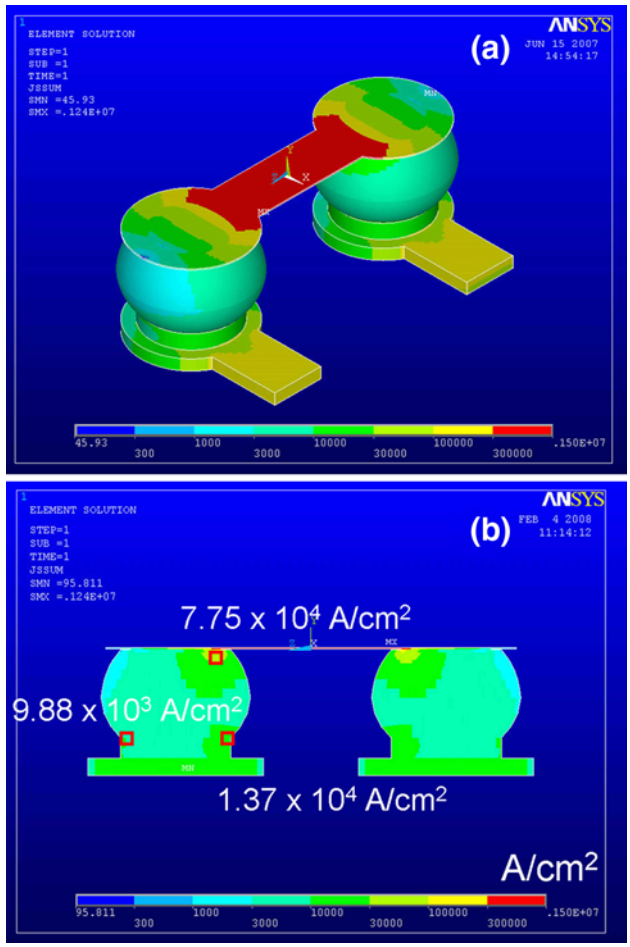

Fig. 4. Simulated current density distribution in the solder joints. (a) Tilted view of the two solder bumps connected by an Al trace. (b) Cross-sectional view showing the current density distribution in the two solder joints. Serious current crowding occurs on the chip side. Current crowding also takes place on the substrate side.

implemented the geometry of a cylinder as shown in the equation below:

$$dx = -dr\ \cos\theta = r\sin\theta d\theta$$

$$R = \rho\frac{L}{A} = \int_{\theta_1}^{\theta_2} \rho\frac{r\sin\theta d\theta}{r\sin\theta \times T} = \frac{\rho\theta}{T}\Big|_{\theta_1}^{\theta_2}$$

Based on this calculation, the resistance of the Cu pad was 16.8 mΩ and that of the solder bump was 21.3 mΩ. According to the experimental results, it also appeared that electrons first dispersed across the whole Cu pad and then went upward into the solder. Because the diameter of the Cu pad was 140 μm and the diameter of the contact area between the solder and the Cu pad was 110 μm, the electrons crowded along the edge of the solder bump. Therefore, the current density along the bottom edge of solder was higher compared with other regions at the bottom of the solder bump.

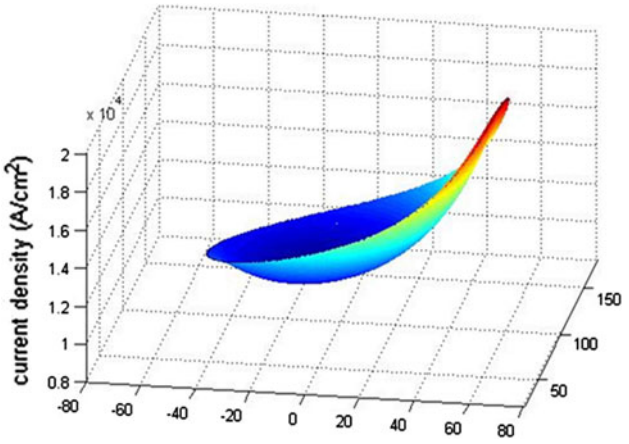

Fig. 5. Current density distribution at the bottom solder layer. The electron flow drifts into the solder joint from the right-hand side.

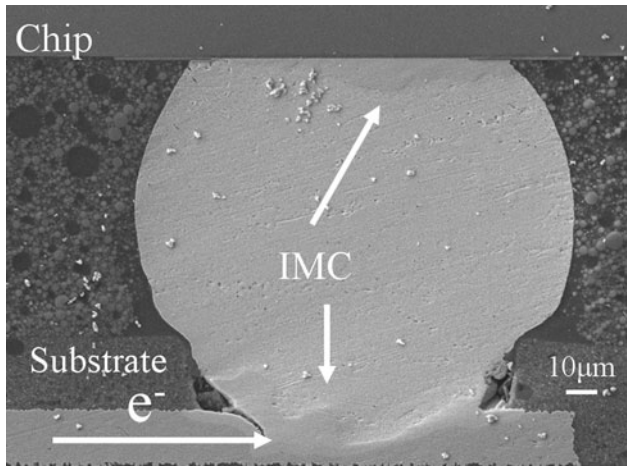

Fig. 6. Cross-sectional SEM image showing the microstructure of a solder bump stressed by 1.5 A at 150°C for 350 h. The electron flow went from the substrate side to the chip side.

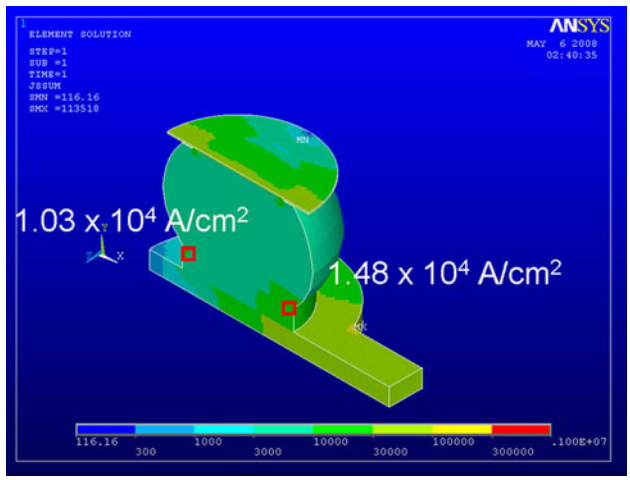

Fig. 7. Cross-sectional view of the current density distribution in a solder joint from finite-element simulations.

Three-dimensional simulations were again implemented to prove this assumption. Figure 5 shows the current density distribution at the bottom solder layer. The maximum current density value was 1.7×10^4 A/cm^2, at the entrance of the Cu pad, and the minimum value was 1.2×10^4 A/cm^2. The difference seemed to be minimal. Interestingly, because electrons went upward into the solder along a narrow path around the periphery of the bottom of the solder bump, the current crowded along this edge and the current density at the edge of the solder bump was higher, compared with other regions, as shown in the simulation results. As a result, the current crowding effect induced void formation and dissolution of Cu near the substrate side, as illustrated in Figs. 1a, 2a, and 3a.

The assumption can be further verified by changing the polishing direction. In other words, the new polishing surface is along the Cu trace and perpendicular to the polishing surfaces in Figs. 1, 2, and 3. Figure 6 shows a cross-sectional SEM image for a solder joint stressed by 1.5 A at 150°C for 350 h. The electron flow drifted from the Cu line on the left-hand side to the chip side. We can observe that voids formed at both bottom edges of the solder joint: one near the entrance of the Cu line, and the other far from the entrance. In addition, some of the Cu metallization was seriously consumed near the entrance of the Cu line. The simulated distribution of the current density is also shown in Fig. 7. It is interesting to see that void indeed formed at this faraway region. The current density at the Cu entrance was 1.48×10^4 A/cm^2, and the current density on the opposite side was 1.03×10^4 A/cm^2. These values were similar, so voids formed at both sides. Not only the entrance but also the opposite side has higher current. The 3D simulation results therefore clearly explain the experimental results.

The results also suggest that, when a thick UBM layer is adopted on the chip side, damage to the OSP Cu would dominate the electromigration failure. With a thick UBM layer, the current crowding and Joule heating effect would be reduced and become more electromigration resistant.

CONCLUSIONS

When the solder joint was current stressed, electrons first dispersed inside the Cu pad and then went up along the edge of the solder bump. Voids therefore formed all around the bottom periphery of the solder bump. On the contrary, at the bottom middle of the solder bump, because solder bonded to the Cu pad through IMCs, which have greater resistance to electromigration compared with Sn, the joint remained connected and no open failure was observed within our experimental timeframe. In this study, the OSP Cu interface on the substrate side was the weakest point in the solder joint even when thin-film UBM was used on the chip side. Regardless of high or low current density, damage

to the OSP Cu interface was clearly observed and more severe on the substrate side, which is different from past experience. In addition, we also found the existence of dual-mode failure with the OSP Cu finish. Damage was found to occur not only at the cathode end on the substrate side but also at the cathode end on the chip side in some cases.

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