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High Quality La_2O_3 and Al_2O_3 Gate Dielectrics with Equivalent Oxide Thickness 5-10Å

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Abstract

High quality La_2O_3 and Al_2O_3 are fabricated with EOT of 4.8 and 9.6Å, leakage current of 0.06 and 0.4A/cm ^{2} and D_{it} of both $3x10^{10}$ eV^{-1}/cm^2, respectively. The high K is further evidenced from high MOSFET 's I_d and g_m with low I_{off}. Good SILC and Q_{BD} are obtained and comparable with SiO_2. The low EOT is due to the high thermodynamic stability in contact with Si and stable after H_2 annealing up to 550°C.

Introduction

Although high K gate dielectrics have attracted much attention recently, further reduction of EOT may be limited by the interface reaction region between high K material and Si [1], [2]. Therefore, the search for thermodynamically stable high K dielectric directly on Si is important to meet future sub-10Å requirement. Besides the required good electrical properties such as low interface trap density (D_{it}), low leakage current, high breakdown field (E_{BD}) and good reliability, high K material must also be compatible with existing VLSI process. Thus, good stability with H_2 and high transition temperature from amorphous to crystal [2] are necessary to prevent dielectric degradation by H_2 and crystalline structure created defects or dislocations during strain relaxation in process. Previously, we have reported that amorphous Al_2O_3 directly on Si can meet near all the requirements and stable up to 1000°C [3], except that EOT (21Å) and D_{it} ($1x10^{11}$ eV^{-1}/cm^2) are still high. The high D_{it} is unacceptable for IC because of the increased noise [4]. In this paper, we have used amorphous La_2O_3 (K~27) to achieve 4.8Å EOT and reduced Al_2O_3 EOT to 9.6Å, where La_2O_3 has similar property as Al_2O_3 but with even better thermal stability on Si (Table 1). In addition to respective low leakage current of 0.06 and 0.4A/cm ^{2} for La_2O_3 and Al_2O_3, both dielectrics now have good D_{it} ($3x10^{10}$ eV^{-1}/cm^2), E_{BD}, SILC, and Q_{BD} as compared with SiO_2.

Experimental

To avoid any K value reduction, interfacial native oxide is suppressed by HF-vapor passivation and *in-situ* desorption [3] followed by an immediate La or Al evaporation. Because La or Al is highly reactive with O_2, low oxidation temperatures ≤400°C is used to reduce metal diffusion into Si. The formed oxides were further annealed in N_2 at 900°C. To reduce gate depletion, Al gate is used for MOS capacitor and transistor to evaluate the electrical characteristics. H_2 annealing at 450-550°C is performed to study the stability with H_2. Besides achieved higher K, suppression of native oxide is important to obtain a smooth interface, low D_{it}, and high reliability in our previously achieved atomically smooth ultra-thin oxides.

Results and Discussion

A. Gate capacitor:

Fig. 1 presents the J-V characteristics of La_2O_3 and Al_2O_3 capacitors. Comparable leakage current for La_2O_3 on Si or $Si_{0.3}Ge_{0.7}$ is obtained that is important for high mobility PMOS [5]. The stacked Al_2O_3/La_2O_3 is used to reduce leakage current for C-V to obtain D_{it}. In order to get accurate K and EOT , the oxide thickness is carefully examined by both ellipsometer and TEM in Fig. 2. The very uniform oxide and smooth interface are due to native oxide free surface and high thermal stability in Table 1 as contact with Si. Therefore, low EOT can be expected. Fig. 3 shows the cumulative values for high K oxides, and leakage current of 0.06A/cm ^{2} for La_2O_3 and 0.4 A/cm^2 for Al_2O_3 are obtained. Fig. 4 is the C-V curves and K values of 27 and 8.5 are measured for respective La_2O_3 and Al_2O_3 that gives the low 4.8Å and 9.6Å EOT (without QM correction). Small hysterisis of 11 and 22mV are measured for respective dielectrics that indicates good quality because of applied high annealing temperature without transition to crystal structure [2]. Fig. 5 shows the measured D_{it} of $3x10^{10}$ eV^{-1}/cm^2 from both capacitors. This low D_{it} close to thermal SiO_2 is extremely important for circuit to lower 1/f noise [4].

B. Transistor performance with 4.8Å EOT:

We have further fabricated wide gate MOSFETs with 4.8Å EOT. Figs. 6 shows the device I_d-V_d, and important I_d-V_g and g_m are plotted in Fig. 7. The very high current drive and g_m are due to high K that gives a K of ~27 consistent with C-V measurement. Good device pinch-off $I_{off}<10^{-10}$A/μm and small sub-threshold swing of 75mV/decade are observed, and the small swing also suggests the low D_{it}. The effective mobility is further plotted in Fig. 8. The electron mobility is comparable with published universal mobility data for thermal SiO_2 because of low D_{it}.

C. Reliability:

Fig. 9 shows the gate dielectrics under a -2.5V constant stress for 1hr with total Q_{inj} of $1.3x10^3$ and $1.2x10^5$C/cm^2 for La_2O_3 and Al_2O_3, respectively. No significant charge trapping is occurred during stress, and small SILC for both dielectrics is observed in Fig. 10. Good reliability for 4.8 Å EOT La_2O_3 is evidenced from the high Q_{BD} in Fig. 11 and comparable with current SiO_2 [6]. The good SILC and Q_{BD} may be due to the high lattice energy in Table 1. From the 50% failure time, an extrapolated max voltage of 2.3V is obtained for 10 years lifetime that suggests good reliability for VLSI application with 4.8Å EOT and small leakage of 0.06A/cm^2 at1V.

Conclusions

We have shown that La_2O_3 is good for EOT down to 5Å and Al_2O_3 is highly competitive for EOT ≥10Å.

References

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TABLE I. Physical properties for various high-K materials. La_2O_3 shows the best thermal stability when contact with Si.

	SiO_2	Al_2O_3	La_2O_3	HfO_2	ZrO_2
Contact stability with Si (KJ/mole) $Si+MO_x \rightarrow M+SiO_2$	stable	+63.4	+98.5	+47.6	+42.3
Lattice energy (KJ/mole)	13125	15916	12452	-	11188
Bandgap (eV)	9.0	8.8		5.7	5.2-7.8
Structure type	amorphous	amorphous	amorphous	crystal T>700°C	crystal T>400-800°C
Effective K value	3.9	8.5-10	27	~24	11-18.5

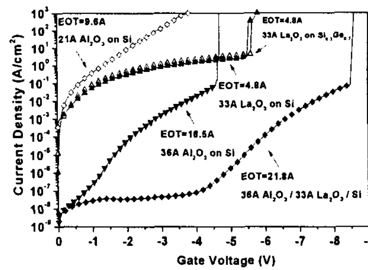

Fig. 1. J-V characteristics for Al_2O_3 (9.6 & 16.5Å EOT) and La_2O_3 (4.8Å EOT) capacitors. Stacked structure is adopted to reduce leakage current for D_{it} measurement.

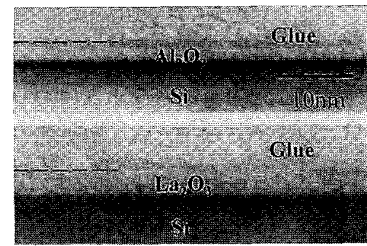

Fig. 2. Cross-section TEM of Al_2O_3 and La_2O_3. Very smooth interface is due to the high thermal stability and native oxide free surface. Both dielectrics are amorphous.

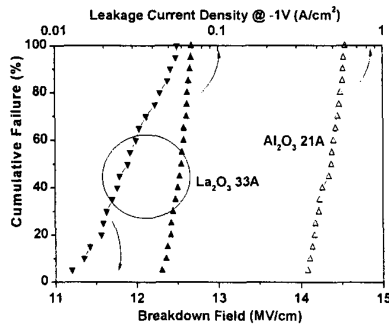

Fig. 3. Cumulative distribution of leakage current and breakdown field for Al_2O_3 and La_2O_3 gate dielectrics.

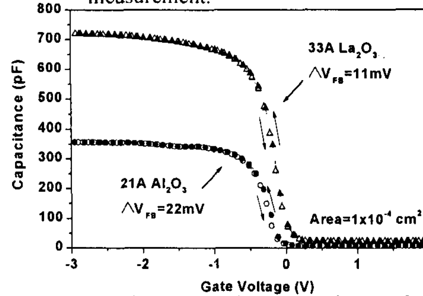

Fig. 4. Hysteresis curves for Al_2O_3 and La_2O_3 gate dielectrics.

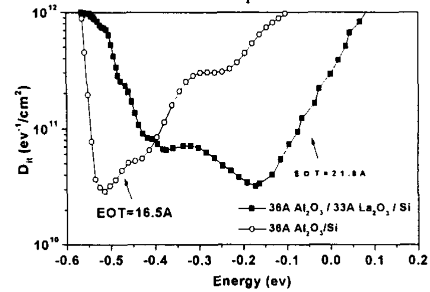

Fig. 5. Interface state density of Al_2O_3 and La_2O_3 on Si. Min D_{it} of $3x10^{10}$ eV^{-1}/cm^2 is obtained for both dielectrics and close to SiO_2/Si.

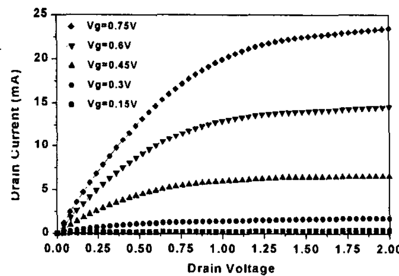

Fig. 6. I_d-V_d characteristics of 30μmx1200μm NMOSFETs with 33Å La_2O_3 gate dielectric.

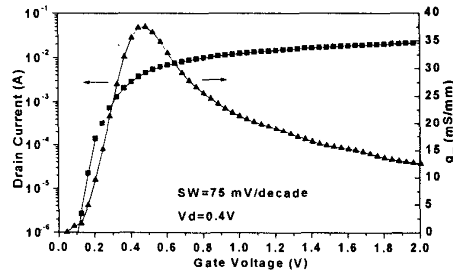

Fig. 7. Subthreshold characteristic and transconductance for 33Å La_2O_3 NMOSFETs as a function of gate bias.

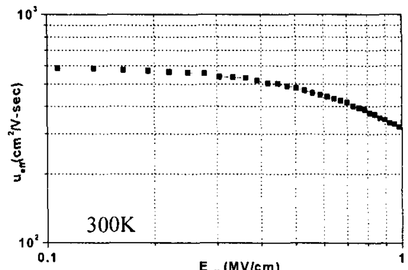

Fig. 8. Effective electron mobility versus electrical field for 33Å La_2O_3 NMOSFET.

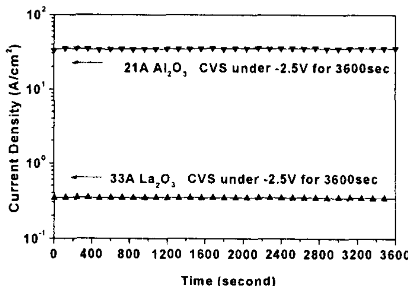

Fig. 9. Time evolution of I_g under -2.5V for 1hr with Q_{inj} of $1.3x10^3$ and $1.5x10^5$ C/cm^2 for respective La_2O_3 and Al_2O_3.

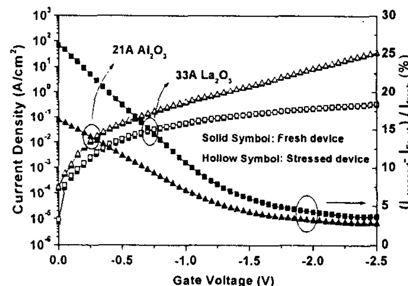

Fig. 10. Stress induced leakage current and current variation for Al_2O_3 and La_2O_3 under -2.5V for 1hr.

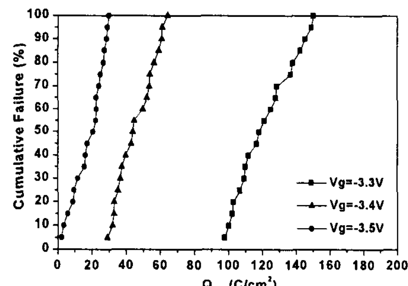

Fig. 11. Q_{BD} distribution of La_2O_3 dielectric with different V_g. For 50% MTTF and 10 years lifetime, a max operation voltage of 2.3V is obtained.