Highly Reliable Liquid-Phase Deposited SiO_2 with Nitrous Oxide Plasma Post-Treatment for Low Temperature Processed Poly-Si TFT's

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Abstract

Low temperature (~300°C) N_2O plasma annealing for liquid-phase deposited (LPD) gate oxide has been proposed for the first time. Physicochemical and electrical characterizations show that the N_2O-treated LPD-SiO_2 improves breakdown field, interface state density, and Si-rich phenomenon. This novel technology has been also successfully applied to LTP poly-Si TFT's, which reveal excellent characteristics and reliability. It is believed that the N_2O plasma post-treatment not only improves the oxide quality, but also passivates the trap states in poly-Si channel.

Introduction

The development of high-quality gate oxide film is an important issue for fabricating low temperature processed (LTP) poly-Si TFT's. Recently, The way of liquid-phase deposited oxide (LPD-SiO_2) has been accepted much attention for the advantages of room temperature process (< 30°C), plasma-damage free and inexpensive apparatus [1-3], as compared with that using CVD and PVD techniques. In the past, we had successfully applied LPD-SiO_2 to LTP poly-Si TFT's as the gate insulator [4] and improved the oxide quality by way of furnace annealing in O_2 ambient [5]. According to that reported in [6-7], nitridation of oxide can further improve Si/SiO_2 interface properties and provide superior electrical characteristics and oxide reliability. In this paper, we will first apply the low temperature (~300°C) N_2O plasma annealing technology to the LPD oxide. Results of physicochemical and electrical properties will be then compared with that by furnace annealing. Also, the poly-Si TFT's with the N_2O-treated LPD gate oxide will be fabricated and evaluated. Finally, it will be pointed out that the N_2O plasma post-treatment is important and indispensable for improving TFT performance and reliability.

Table 1 Basic characteristics for LPD-SiO_2 with different post-treatment conditions.

Annealing Condition	thickness (Å)	refractive index	P-etch rate (Å/s)	dielectric constant
As-deposited	352	1.395	20.7	3.459
Furnace(600°C O_2 1hr)	354	1.396	6.7	3.632
N_2O Plasma 5'	386	1.419	9.2	3.776
N_2O Plasma 15'	465	1.430	8.3	3.847
O_2 Plasma 5'	354	1.396	13.9	3.562
O_2 Plasma 15'	352	1.396	14.2	3.542

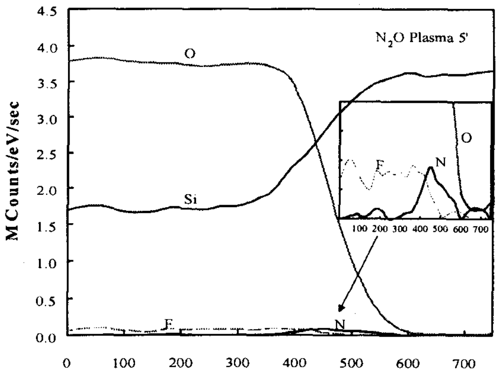

Fig. 1 AES depth profiles for N_2O-plasma (5 min) post-treated LPD-SiO_2.

Experiments

A. Preparation of N_2O plasma post-treated LPD-SiO_2

The chemical reaction for LPD-SiO_2 growth can be simply represented by the following equilibrium reaction:

$$H_2SiF_6 + 2H_2O \leftrightarrow 6HF + SiO_2 \qquad \Delta H < 0. \qquad (1)$$

The deposition rate of LPD-SiO_2 is controlled by change of H_2O quantity. First, Hydrofluorosilicic acid with saturated SiO_2 was prepared at 23°C for 17 hours and the Si substrates with native oxide were then immersed into the supersaturated solution at 18°C, where SiO_2 was deposited on the test samples by adding enough water. Finally, the LPD-SiO_2 samples were performed N_2O plasma treatment for 5-15 minutes.

B. Fabrication of LTP Poly-Si TFT's

Low temperature poly-Si TFT's are fabricated with a maximum processing temperature of 600°C. Undoped 1000Å-thick poly-Si film and 370Å-thick LTP-SiO_2 was deposited as the active layer and gate insulator, respectively. After deposition of the LPD gate oxide, the N_2O plasma was performed for 5-15 minutes to form the SiN_xO_{2-x} composition. The top-gate structures with self-aligned implantation were

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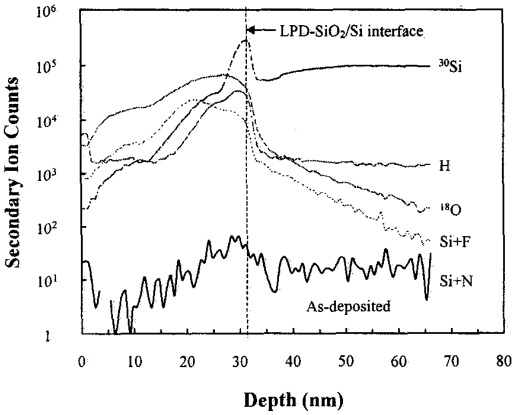

Fig. 2 SIMS depth profiles for as-deposited LPD-SiO_2.

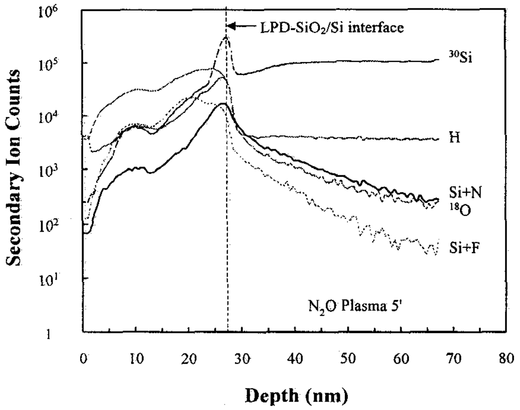

Fig. 3 SIMS depth profiles of LPD-SiO_2 after N_2O plasma post-treatment for 5 minutes.

adopted and 5000 Å-thick tetraethyl orthosilicate (TEOS) SiO_2 was deposited as the passivation layer. After contact holes were opened, a 5000 Å-thick aluminum layer was evaporated and patterned. Aluminum sintering was performed at 400°C for 30 minutes. The detailed fabrication procedures are described in the earlier report [8].

Results and Discussion

A. Physicochemical Characteristics of LPD-SiN_xO_{2-x}

Table 1 shows the basic characteristics of LPD-SiO_2 with O_2 and N_2O plasma post-treatments. The result of O_2 furnace annealing is also shown for comparison. After the N_2O plasma post-treatment, both refractive index and dielectric constant increase, which implies that the N_2O plasma re-oxidizes LPD-SiO_2 , and hence improves the oxide structure. The small p-etch rate also indicates the superior densification of LPD-SiN_xO_{2-x} film. Fig. 1 shows the AES depth profiles for the N_2O plasma post-treated LPD-SiO_2. The N_2O plasma improves the Si-rich phenomenon and reduces the fluorine concentration rather than the as-deposited LPD-SiO_2. In addition, it is found that nitrogen atoms are piled up at Si/SiO_2 interfaces. The result can be further verified by the SIMS experiments. Fig. 2 and Fig. 3 show the SIMS depth profiles for the as-deposited LPD-SiO_2 and the LPD-SiN_xO_{2-x}, respectively, where the concentration of nitrogen in the as-deposited LPD-SiO_2 is extremely low, while a pronounced increase of nitrogen concentration in the LPD-SiN_xO_{2-x} is observed. From the above results, it can be noted that most of the nitrogen atoms in the LPD-SiN_xO_{2-x} pile up at the Si/LPD-SiO_2 interface, and some of them exist in oxide bulk.

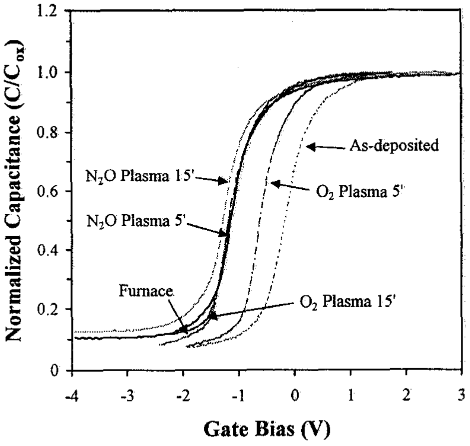

Fig. 4 C-V characteristics of the LPD-SiO_2 with different post-treatment conditions.

B. Electrical Characteristics of LPD-SiN_xO_{2-x}

Fig. 4 shows the C-V characteristics of LPD-SiO_2 with different post-treatment conditions, where curves of the LPD-SiN_xO_{2-x} samples are shifted toward left side as compared with that of the as-deposited and O_2 plasma samples. It implies the breaking of Si-OH and Si-F bonds, so OH^- and F^- ions are diffused out from the LPD-SiO_2 film. These escaped

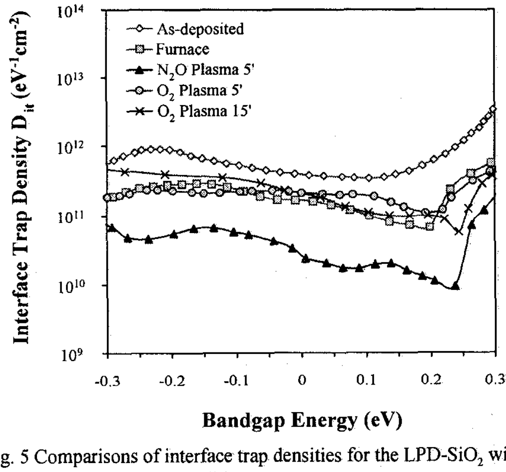

Fig. 5 Comparisons of interface trap densities for the LPD-SiO_2 with different post-treatment conditions.

negative ions will subsequently leave oxygen vacancies $O_3\equiv Si$ $Si\equiv O_3$, which can be thought as the positive charges, and therefore results in the left shift of C-V curves. Fig. 5 shows the comparisons of interface trap densities (D_{it}) for the LPD-SiO_2 with different post-treatment conditions. The N_2O sample has smaller D_{it} (~10^{10} $eV^{-1}cm^{-2}$) as compared with the as-deposited sample (7×10^{11} $eV^{-1}cm^{-2}$). It can be attributed to the excellent improvement of LPD oxide, which is due to the oxygen diffusion as well as the nitrogen incorporation into the Si/LPD-SiO_2 interface. The nitrogen incorporation forms a buffered layer, which is composed of Si≡N bonds within the first 10Å from the interface and Si=N-O bonds outside of the first 10Å region [9]. The buffered layer plays an important role in reducing the interface stress, caused by the Si lattice-mismatch between the Si bulk and the oxide overlayer. The lattice-mismatch mainly results from the incomplete bonding of Si^{+2} and Si^{+3}. The J-E characteristics of the LPD-SiO_2 with different post-treatment conditions are shown in Fig. 6. At lower electrical field, the leakage current density for all samples is nearly the same (~2×10^{-9} A/cm^2). However, after the N_2O plasma post-treatment for 5 minutes, the electrical breakdown field of the LPD-SiO_2 is obviously higher (~11.0MV/cm) than that of other samples. In addition, the onset-tunneling field of the N_2O sample is also larger than that of others. They can be attributed to that the N_2O plasma treatment effectively relieves the interfacial stress and improves the Si-rich phenomenon. The strong Si-N bonds prevent electrons from direct tunneling between Si islands. Fig. 7 shows the Weibull plots of electrical breakdown field for different LPD samples. As described in Fig. 6, the N_2O sample has the largest electrical breakdown field and best breakdown uniformity than other samples. Fig. 8 shows the Fowler-Nordheim plots for different LPD samples, where a linear relationship for all samples is obtained. The barrier height at the Si/LPD-SiO_2 interface is calculated from these linear plots. As shown in Fig. 8, the LPD-SiN_xO_{2-x} improves barrier height of the as-deposited LPD-SiO_2 from 1.78 to 3.36eV.

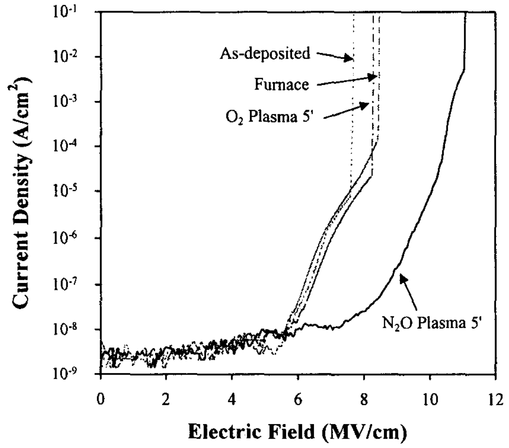

Fig. 6 J-E characteristics of LPD-SiO_2 with different post-treatments.

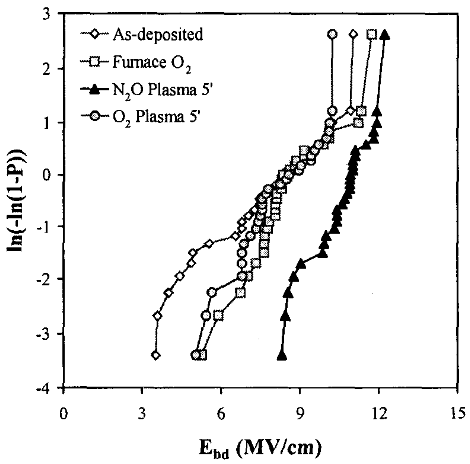

Fig. 7 Weibull plots of breakdown field for LPD-SiO_2 with different post-treatments.

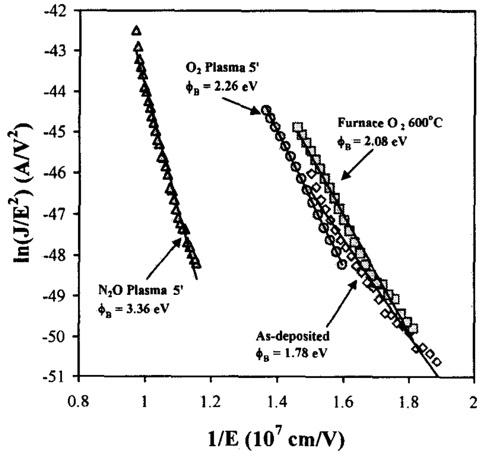

Fig. 8 Fowler-Nordheim plots of LPD-SiO_2 with different post-treatments.

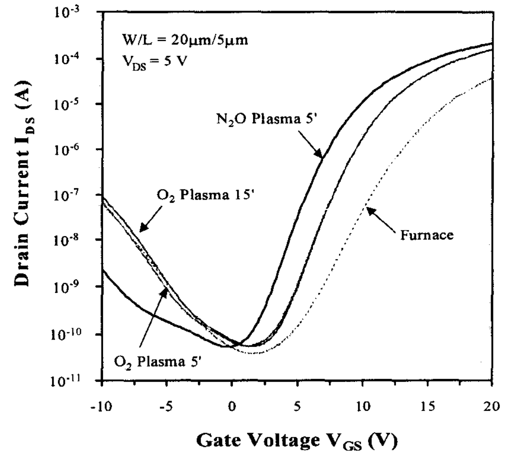

Fig. 9 Comparison of transfer characteristics for the LTP poly-Si TFT's with different post-treatment conditions.

C. Performance and Reliability for LTP poly-Si TFT's

Fig. 9 shows the transfer characteristics for the LTP poly-Si TFT's with different post-treated LPD gate oxide. It is clear that the N_2O sample much improves the electrical characteristics such as driving current, off-state current, subthreshold slope and threshold voltage rather than the furnace annealing and O_2 plasma samples. The calculated device parameters of all samples are summarized in Table 2. For the N_2O plasma sample (5 min), μ_{FE} increased from 7.71 to 16.31 $cm^2/Vsec$ and V_T decreased from 11.89 to 7.14 V. The superior device characteristics suggest that the N_2O sample has lower trap-state density and grain barrier height in the poly-Si channel. Fig. 10 shows the ON-current degradations as a function of stress time for different TFT samples under the stress of $V_{GS}=V_{DS}=15V$. The degradation of the N_2O sample is smaller than that of other samples. As it was known that the degradation of such an on-state stress is mainly due to the breaking of weak Si-Si and Si-H bonds, which generally forms the metastable trap states. The N_2O plasma treatment can effectively passivate trap states and replace these weak Si-Si bonds with the strong Si-N bonds. Fig. 11 shows the ON-current degradation as a function of stress time for different TFT samples under the stress of $V_{DS}=0V$ and $V_{GS}=20V$. The N_2O sample reveals much better stress endurance than other samples. It implies that the N_2O sample can prevent electrons from trapping in the gate oxide. From the above results, the excellent gate-oxide reliability in N_2O sample can be thought as the incorporation of nitrogen atoms at the LPD-SiO_2/poly-Si interface, which forms strong Si-N bonds and hence relieves the interfacial stress.

Conclusion

In conclusion, a highly reliable LPD-SiN_xO_{2-x}, deposition of LPD-SiO_2 followed by N_2O plasma treatment, has been developed for low temperature and high quality gate oxide. From the analysis of physico-chemical and electrical properties, the LPD-SiN_xO_{2-x} reveals improved oxide quality and interface characteristics such as dielectric constant, Si-rich phenomenon and interface trap density. As applied to LTP poly-Si TFT's, the device performance and reliability of the LPD-SiN_xO_{2-x} TFT are better than the furnace annealing and O_2 plasma TFT's.

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Table 2 Calculated device parameters for the LTP poly-Si TFT's with different post-treatment conditions.

Gate Oxide Post-Annealing	V_{th} (V)	Swing (V/dec)	I_{ON} (μA)	I_{OFF} (pA)	I_{ON}/I_{OFF}	μ_{FE} (cm^2/V·sec)	N_t (cm^{-2})
Furnace	11.89	1.708	37.06	45.70	8.11×10^5	7.71	1.29×10^{13}
N_2O Plasma 5'	7.14	1.250	194.6	59.05	3.30×10^6	16.31	7.55×10^{12}
N_2O Plasma 15'	7.57	1.398	132.1	113.8	1.16×10^6	13.92	6.62×10^{12}
O_2 Plasma 5'	8.94	1.304	146.5	99.85	1.46×10^6	14.55	8.01×10^{12}
O_2 Plasma 15'	8.93	1.285	148.4	56.10	2.65×10^6	14.80	8.10×10^{12}

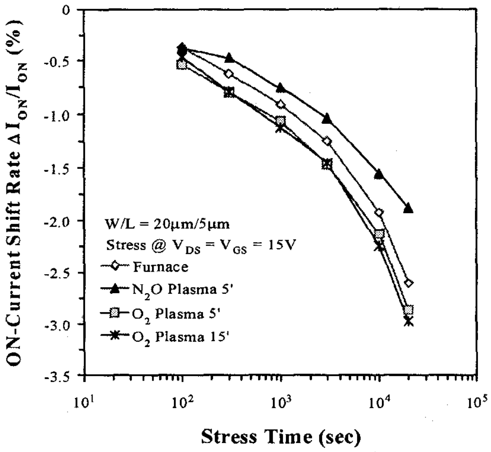

Fig. 10 ON-current degradation with stress time for the LTP poly-Si TFT's with different post-treatment conditions under the stress of $V_{GS}=V_{DS}=15V$.

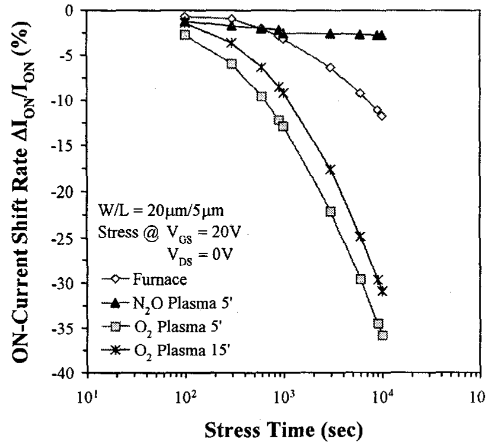

Fig. 11 ON-current degradation with stress time for the LTP poly-Si TFT's with different post-treatment conditions under the stress of $V_{DS}=0V$, $V_{GS}=20V$.