A 78 ∼ 102 GHz Front-End Receiver in 90 nm CMOS Technology

Hsuan-Yi Su, Robert Hu, and Chung-Yu Wu

***Abstract*—In this letter, a 78 ∼ 102 GHz front-end receiver designed in 90 nm CMOS technology is presented. It consists of an ultra-wideband low-noise amplifier, a subharmonic mixer, and an IF buffer. This receiver has a peak gain of 11.8 dB at 94 GHz with the noise figure of 13.4 dB. The measured input-referred 1 dB compression point is −14.5 dBm and the total power dissipation is 18.6 mW. The chip size is $680 \times 1020\ \mu\mathrm{m}^2$.**

***Index Terms*—CMOS receiver, low noise amplifier (LNA), subharmonic mixer, ultra wideband (UWB), W-band.**

I. Introduction

MILLIMETER-WAVE receivers have been widely used in applications such as radars, radiometers and scientific instrumentations. Recently, we have seen the surging of novel 60 GHz silicon-integrated circuits proposed for high definition multi-media interface (HDMI), and their prototypical commercial products are also presented [1]–[7]. This, therefore, prompts us to the challenge of using similar process technology to design an even higher 78 ∼ 102 GHz receiver circuit so that both reliability and affordability can be achieved for W-band data and multimedia communications, either narrow-band or wideband, in the near future.

Designed in 90 nm CMOS technology, the proposed receiver is made of three sub-circuits: the first is an ultra-wideband low noise amplifier (LNA), the second is a subharmonic mixer with wide intermediate frequency (IF), and the last is an open-drain IF buffer to facilitate direct measurement. As shown in Fig. 1, the incoming millimeter-wave signal is sent to a matched three-stage LNA first. The amplified 78 ∼ 86 GHz RF signal is then transformed to its $\mathrm{DC} \sim 8-\mathrm{GHz}$ IF counterpart when the local-oscillation (LO) frequency of the subharmonic mixer is set to 39 GHz. By setting the LO to 43, 47, and 51 GHz, respectively, the 86 ∼ 94 GHz, 94 ∼ 102 GHz, and 102 ∼ 110 GHz RF signals can be down-converted consecutively. The proposed receiver demonstrates comparable performance with other receivers designed in more advanced process technologies [8], [9], but it has a wider bandwidth and consumes less power. Description of the LNA, mixer, and IF buffer as well as measurement results will be given in the following.

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The authors are with the Department of Electronics Engineering, National Chiao Tung University, Hsinchu 300, Taiwan (e-mail: hillo.ee91g@nctu.edu.tw).

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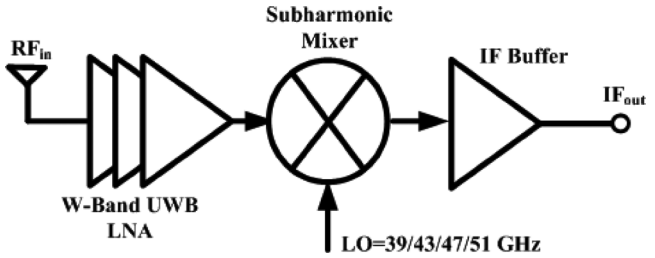


Fig. 1. Block diagram of the W-band receiver. With 39 GHz LO, the 78 ∼ 86 GHz RF is transformed to the $\mathrm{DC} \sim 8-\mathrm{GHz}$ IF. When the LO is shifted to 43, 47, and 51 GHz, respectively, the 86 ∼ 94 GHz, 94 ∼ 102 GHz and 102 ∼ 110 GHz RF signals can be down-converted consecutively.

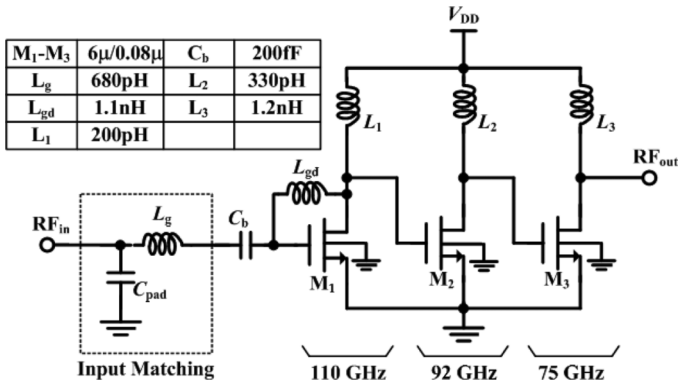
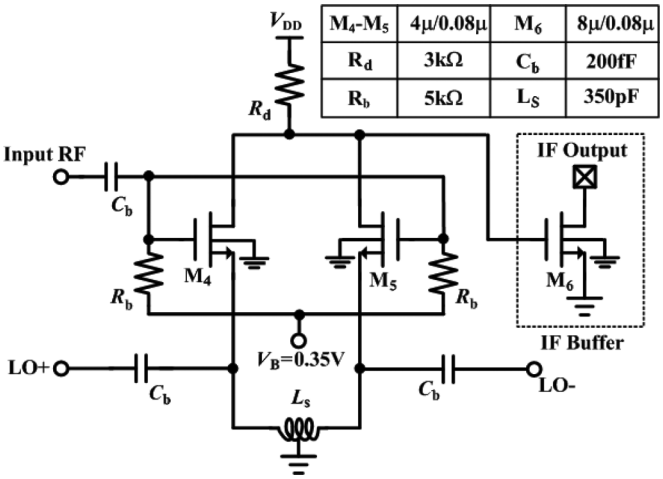


Fig. 2. Schematic of the LNA. The inductor L_{gd} is used to resonate out the gate-drain capacitor of transistor M_1.

II. Circuit Design

The schematic of the CMOS W-band LNA is shown in Fig. 2. It is composed of three common-source amplifying stages where the frequency for maximum gain in each stage is set at three different frequency points. Thus overall bandwidth in the LNA design can cover 78–102 GHz. To obtain a nearly flat gain over the bandwidth, the maximum gain of each stage is kept almost the same, which is around 18 dB in post-layout simulation. All the transistors in Fig. 2 are made of three 2 μm-wide 80 nm-long fingers, with the corresponding unity-gain (cutoff) frequency f_{T} being 144 GHz under drain bias voltage of 1.2 V and drain bias current of 3.2 mA.

The input matching circuit consists of a pad capacitor C_{pad} and a gate inductor L_{g}. The minimum input reflection coefficient occurs at around 95 GHz. As the first stage of the LNA needs to reach its maximum gain at a very high frequency, a feedback inductor L_{gd} is inserted between the drain and gate nodes of the transistor M_1 so as to resonate its gate-drain capacitance C_{gd} and boost its gain performance at 100 GHz and above. Since the maximum-gain frequencies of 92 GHz and 75 GHz designated for the second and third stages, respectively, are well below f_T of 144 GHz, no such inductor is needed, and therefore



M_4-M_5	4μ/0.08μ	M_6	8μ/0.08μ
R_d	3kΩ	C_b	200fF
R_b	5kΩ	L_S	350pF

Fig. 3. Schematic of the subharmonic mixer and IF buffer.

compact chip size can be retained. Through the drain inductor $L_1(L_2)$ and $L_{\rm gd}$, the gate bias voltages of $\rm M_2(M_3)$ and $\rm M_1$ can be set to the system voltage $V_{\rm DD}$, respectively. Thus extra gate bias circuits and the inter-stage DC-blocking capacitors can be avoided to completely remove their effects on the gain degradation.

Fig. 3 shows the subharmonic mixer used in the proposed receiver where the RF signal is connected to the gate nodes of the mixing transistors $\rm M_4$ and $\rm M_5$, the LO is applied to their source nodes, and the down-converted IF is extracted from the common drain node. Mathematically, the LO modulated transconductance $G_{\rm m}(\rm t)$ can be expressed as

$$G_m(t) = G_{m0} + G_{m1}\cos(\omega_{LO}t) + G_{m2}\cos(2\omega_{LO}t) + G_{m3}\cos(3\omega_{LO}t) + \cdots$$

where $\omega_{\rm LO}$ is the LO frequency. The down-converted upper-side-band IF voltage $V_{\rm IF}$ can be derived as

$$V_{IF}(t) = V_{RF}R_dG_{m2}\cos\left[(\omega_{RF} - 2\omega_{LO}t)\right]$$

where $V_{\rm RF}$ and $\omega_{\rm RF}$ are the voltage and frequency of the applied RF signal, respectively. The desired IF signal $V_{IF}(\rm t)$ is selected by the low-pass output characteristics of the mixer circuit in Fig. 3. The center-tapped inductor $L_{\rm s}$ is used to resonate the parasitic source capacitance of $\rm M_4$ and $\rm M_5$. Thus a high input impedance between 39 $\sim$ 51 GHz at the LO port can be achieved. In Fig. 3, the three DC-blocking capacitors $C_{\rm b}$ are 200 fF, the two gate bias resistors $R_{\rm b}$ are 5 kΩ, and the drain bias resistor $R_{\rm d}$ is 3 kΩ. The post-layout simulation results show that the proposed mixer has a gain of 3.8 dB. The buffer transistor $\rm M_6$ with its drain node connected to an external bias-Tee is used to facilitate the measurement. Photograph of the receiver chip is shown in Fig. 4.

III. Measurement Results

In the measurement setup shown in Fig. 5, the W-band source module (Agilent S10MS-AG) is used to shift the frequency of the RF signal from the signal generator (Agilent E8257D) to the W-band. The W-band attenuator is used to adjust the corresponding power level and its output is connected to the chip through the adapter (WR-10) and cable. The 180-degree hybrid power divider is used to generate the differential LO signals.

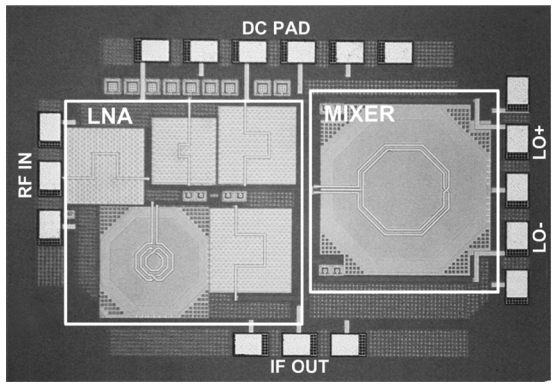


Fig. 4. Photograph of the W-band CMOS receiver chip. The chip size is $680 \times 1020\ \mu\rm m^2$.

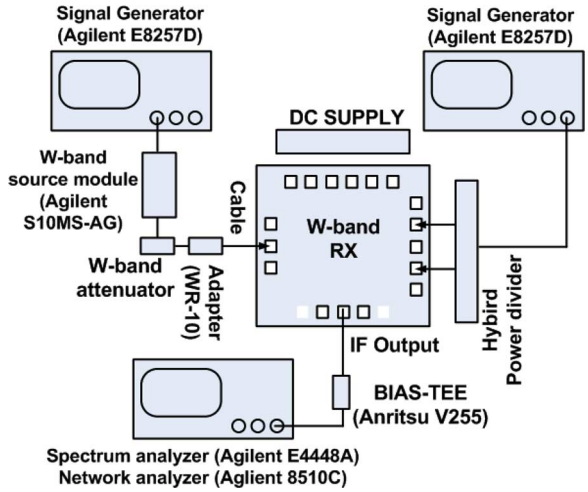


Fig. 5. Measurement setup for the fabricated W-band CMOS receiver.

As mentioned, a bias-Tee (Anritsu V255) is connected to the IF output of the fabricated chip to allow direct measurement using a network analyzer (Agilent 8510C) or spectrum analyzer (Agilent E4448A). To calibrate the power loss of RF input signal to the chip under test, a self-calibrated W-band harmonic mixer (Agilent 11970W) is used to measure the input RF power through the cable before the chip measurement. Thus the power loss is calibrated and it does not affect the measured results.

The measured gain and noise figure are shown in Fig. 6, where a fixed 39 GHz LO is employed to obtain the 78 $\sim$ 86 GHz RF response. By moving the LO frequency to 43, 47, and 51 GHz, respectively, the 86 $\sim$ 94 GHz, 94 $\sim$ 102 GHz and 102 $\sim$ 110 GHz RF responses can be successively measured. The low (high) boundary of 1 dB gain ripple is at 80 GHz (96 GHz) where the gain is 10.6 dB (11.4 dB) and the noise figure is 14 dB (12.7 dB). At a much higher frequency, discernible performance degradation is observed in the measurement, which can be attributed to the uncertainties of both active and passive device modeling [10]. Fig. 7 shows the measured input reflection coefficient $S_{\rm RF}$ at the RF port. It can be seen that $S_{\rm RF}$ is smaller than -5 dB between 85 $\sim$ 102 GHz and it can be as low as -19 dB at 94 GHz. To achieve the broadband matching where $S_{\rm RF}$ is kept low over a wide bandwidth, a more complicated input matching circuit considering the effect of $L_{\rm gd}$ is required. The input-referred 1 dB compression point, i.e., P1 dB, of the fabricated receiver

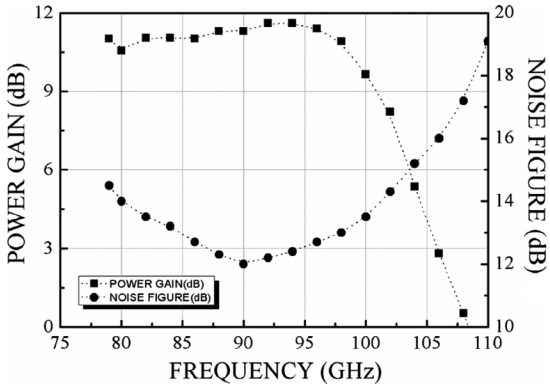


Fig. 6. Measured gain and noise figure of the fabricated receiver. The gain is 10.6 dB (11.4 dB) and the noise is 14 dB (12.7 dB) at 80 GHz (96 GHz).

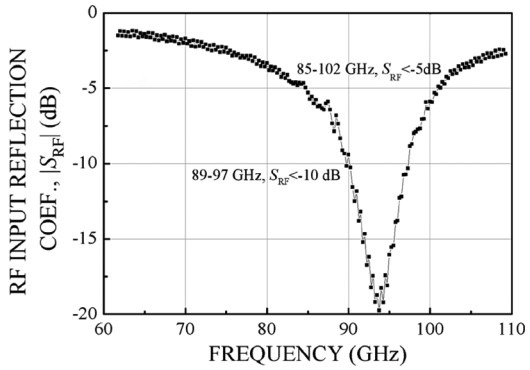


Fig. 7. Measured input reflection coefficient $|S_{\rm RF}|$ at the RF port. Between 85 $\sim$ 102 GHz, $S_{\rm RF}$ is small than -5 dB. Between 89 $\sim$ 97 GHz, $S_{\rm RF}$ is smaller than -10 dB.

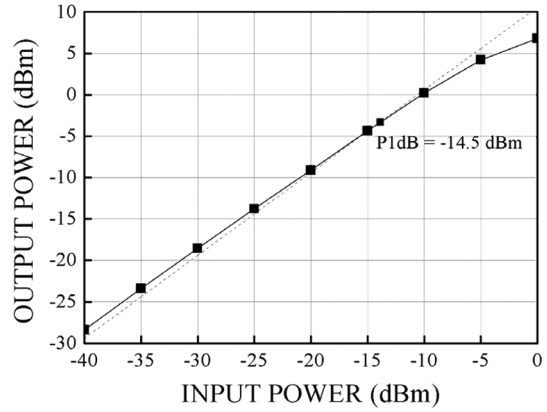


Fig. 8. Measured output IF power versus input RF power where the input-referred P1 dB is -14.5 dBm at 93 GHz.

at 93 GHz is -14.5 dBm, as determined from Fig. 8. The performance comparison with other W-band CMOS receivers is given in Table I where the values of power dissipation for all the receivers includes those of LNA and mixer only. The proposed receiver in 90 nm CMOS technology rather than the more advanced 65 nm CMOS technology, has a slightly larger noise figure. However, it has a much wider RF and IF bandwidth while consuming only 14.4 mW. When the IF buffer is taken into account, the total power consumption of the proposed receiver is 18.6 mW.

TABLE I
PERFORMANCE COMPARISON OF W-BAND CMOS RECEIVERS

	[8]	[9]	THIS WORK
RF (GHz)	75-91	75-95	78-102
Gain (dB)	13	12	11.8
P1dB (dBm)	-16	-18	-14.5
Noise Figure (dB)	7.5	7	11.6
Supply Voltage (V)	1.5	1.2	1.2
Power (mW)	47*	48*	14.4* (18.6)
Chip Area (μm^2)	0.23	0.66	0.69
CMOS Porcess	65-nm	65-nm	90-nm

* These values only include the power dissipation of LNA and mixer for a fair comparison.

IV. CONCLUSION

In this letter, a W-band CMOS front-end receiver is presented. It has been successfully designed and measured in 90 nm CMOS technology. The receiver is made of an ultra-wide-band three-stage LNA, a subharmonic mixer, and an IF buffer. With 8 GHz IF bandwidth, it can easily cover the frequency range of 78 $\sim$ 102 GHz by shifting the LO signal in steps. The proposed receiver has a peak gain of 11.8 dB at 94 GHz with noise figure of 13.4 dB. The total power consumption is 18.6 mW.

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