Liquid Crystal Display (LCD) Supplied by Highly Integrated Dual-Side Dual-Output Switched-Capacitor DC-DC Converter With Only Two Flying Capacitors

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***Abstract*—This paper proposes a highly integrated dual-side dual-output (DSDO) switched-capacitor (SC) converter with only two flying capacitors. Generally, a dual-phase voltage doubler and an inverter are used to supply positive and negative voltages for thin film transistor-liquid crystal display (TFT-LCD) gate drivers, respectively. Four flying capacitors, eight pin-outs for the four flying capacitors, and 16 power switches are necessary for their operations in the driver integrated chip (IC). The proposed DSDO SC converter combines both dual-phase voltage doubler and inverter converter in one channel through the use of time multiplexing technique with minimal performance degradation. As a result, the proposed converter not only reduces the number of flying capacitors from four to two, but also removes four IC pin-outs for lower cost and more compact size. Moreover, the 16 required power switches are reduced to 12, resulting in an approximated 27% decrease of the silicon area.**

***Index Terms*—Constant frequency regulation, DC-DC power converter, dual phase voltage doubler, dual-side dual-output, inverter, switched-capacitor converter.**

I. Introduction

IN RECENT years, because of its brightness, rich color depth, low cost, and long life span, the thin film transistor-liquid crystal display (TFT-LCD) panel has become the most popular display for mobile or handheld devices such as cell phones, MP3 players, digital cameras, personal digital assistants (PDAs) and laptops. Fig. 1 shows the block diagram of a QVGA TFT-LCD driver that is mainly composed of a source driver, a gate driver, VCOM reference voltage, Gamma reference voltage, timing control, and a power generation unit [1]–[4]. The power generation unit can supply the VCORE voltage to the timing control block for sequence control, the VCL voltage for VCOM reference, the VGH and VGL voltages (equal to $4\times$ VCI and $-2\times$ VCI, respectively) for pixel on/off control, and the DDVDH voltage for source driver, and Gamma and VCOM references.

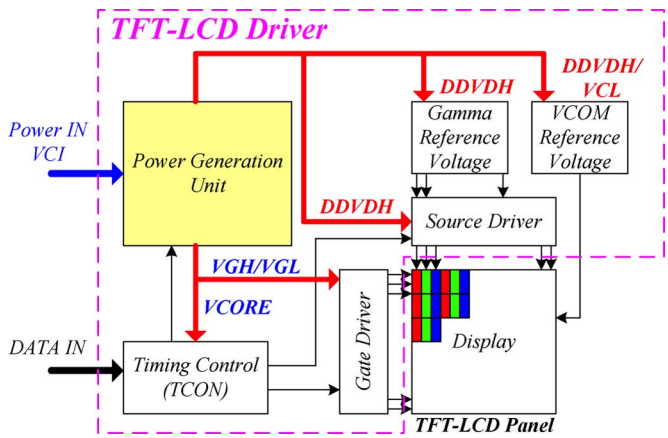

Fig. 1. Simple block diagram of a TFT-LCD driver.

The power supply requirements vary according to the panel driving method, the panel size, and the panel characteristic. In addition, the basic load current requirement in a QVGA panel is in the range of several milliamperes. Thus, the inductive switching converters, such as the boost and inverter, can be used separately to supply the bias requirements for better performance in terms of having a smaller ripple and larger driving capability. However, the two inductor components, which have high costs and large footprint areas compared to the SC converter design, are used. In contrast, many control methods, such as single-inductor dual-output (SIDO) or single-inductor multiple-output (SIMO) controls are used to reduce cost [5]–[10]. However, an inductor is still required, and the control methods remain too complicated. In a load range of 1–2 mA, these inductor-based methods may operate in the discontinuous conduction mode (DCM) or in the continuous conduction mode (CCM) mode with a large inductor. These methods are overdesigned and are not suitable for such application.

According to the conventional power generation unit design, the SC voltage converters, also called charge pumps, are most commonly used in hand-held TFT-LCD drivers. As shown in Fig. 1, these voltage converters are used to convert the system input voltage level, *VCI*, to a higher voltage level (doubler) or a negative voltage level (inverter) for use in certain function

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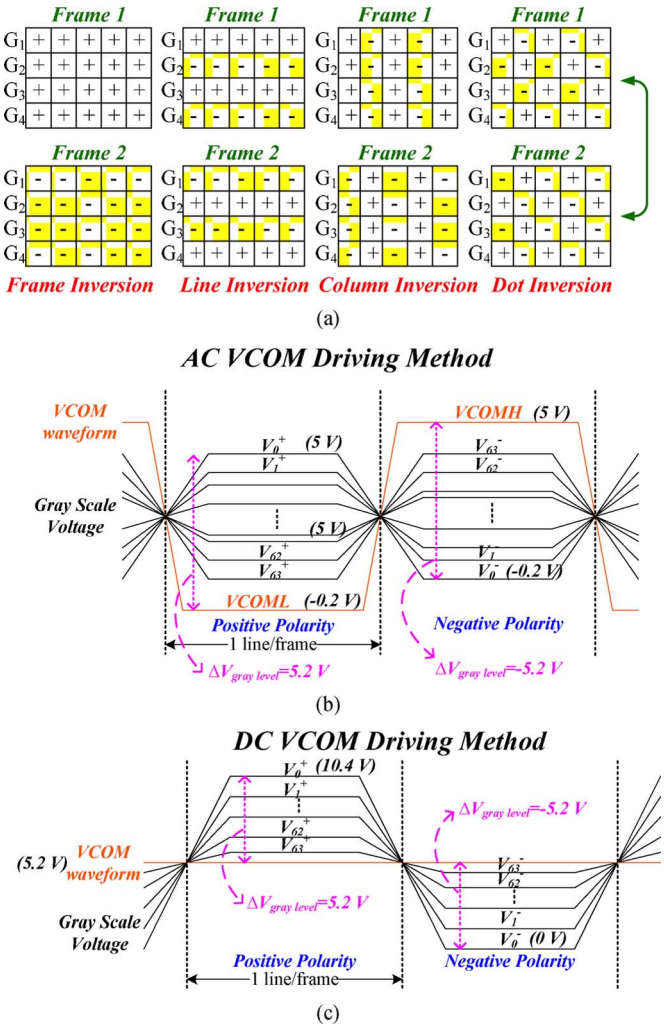

Fig. 2. (a) Operation of the inversion-based techniques. (b) AC VCOM driving control. (c) DC VCOM driving control.

blocks in the TFT-LCD driver, such as the gate, source and VCOM drivers [1].

The flicker issue in the TFT-LCD driver can be effectively solved using inversion-based techniques, such as frame inversion, line inversion, or dot inversion [1]–[4]. The theory of the inversion-based techniques is based on having different polarities for liquid crystals between the previous and succeeding frames. The polarity reverse control is shown in Fig. 2(a). The net effective voltage across the liquid crystals or pixels is zero. Frames 1 and 2 (i.e., the previous and the succeeding states, respectively) alternate by cycle. Basically, the control methods used for LC polarity reversion function can be divided into two parts, namely, the AC VCOM and the DC VCOM driving controls. The operations of these control methods are illustrated in Figs. 2(b) and (c), respectively. According to the control topology, the AC VCOM control is suitable for use in frame and line inversion-based drivers. The main advantage of the AC VCOM control is that it reduces the maximum rating of a device without using high voltage, unlike the DC VCOM technique [3], [4]. In general, to have both high-resolution and gray-level performance, the gray-scale voltage is set to 4–5 V. As a result, 12 V high-voltage devices are used for the DC VCOM control. In contrast, with proper design, the AC VCOM control merely requires a 5-V device. Thus, the AC VCOM control is preferred for a small-sized or QVGA TFT-LCD driver. As shown in Fig. 2(b), the VCOM voltage is set to a range between -0.2 V and 5 V. Smaller voltage stress requirement can result in lower-cost chip design showing that the SC converter is suitable for the LCD driver.

Many SC techniques and papers have been published for commercial products [11]–[21]. Usually, the SC converter requires a dual-side voltage doubler and a dual-side inverter for TFT-LCDs in commercial products. The voltage doubler uses two flying capacitors to generate the output voltage with a value two times the input voltage, *VCI*. Similarly, the inverter also uses two flying capacitors to generate the negative output, which is the inversion of *VCI* [13]–[19]. Prior works have proposed an integrated step up/down SC converter or bidirectional charge pump [20], [21]. However, without a negative supply, an independent inverter is still required.

In this paper, the dual-side dual-output (DSDO) switched capacitor (SC) converter needing only two flying capacitors is proposed to generate two voltages, but with the values doubled and a negative system input voltage. The proposal saves over 27% IC layout area and four flying-capacitance pin-outs, compared with conventional designs. The proposed converter is described in Section II. Operation and circuit implementation are described in Section III. Experimental results are shown in Section IV. Finally, a conclusion is made in Section V.

II. The Proposed DSDO SC Converter

Fig. 3 shows the power system of a TFT-LCD driver and its related off-chip capacitors. In a conventional power generation unit, four flying capacitors, C_1–C_4, with eight pins are necessary. The *VCI* supplies the analog module in the range of 2.5–3.6 V. *DDVDH* supplies positive voltage to the source driver. VCOM is a reference voltage of 4.7–6 V, whereas the *VCL* also supplies negative voltage for the VCOM in the range of -2.4 to -3 V. *VGH* and *VGL* are usually in the range of 10 to 20 V and -5 to -15 V, respectively. The *VGH* and the *VGL* channels operate at high-voltage stress (>6 V) and are, therefore, not included in the current study. The specifications of the power generation unit are listed in Table I.

As shown in Fig. 4(a), $\Phi 1P$ and $\Phi 2P$ are non-overlap clocks used for the control of 16 power switches, P1–P8 and N1–N8, with off-chip flying capacitors, C_1–C_4, in a dual-side converter. The advantage of the dual-side voltage converter is its lower voltage ripple compared with the single-side voltage converter. The application of the dual-side voltage converter is shown in Fig. 4(a). However, the dual-side voltage doubler and the dual-side inverter need two extra flying capacitors and four pin-outs compared with the single-side voltage doubler and the single-side inverter. The detailed operation is explained in Section III. Considering the on-resistance of the power switches and the parasitic resistance of the power path during each charge/discharge period, a dual-side converter may not be the most economically

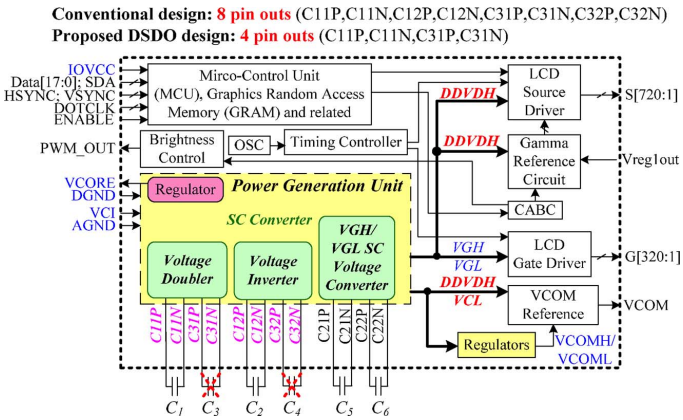

Fig. 3. TFT-LCD driver and its related off-chip capacitors.

TABLE I
VOLTAGE SPECIFICATIONS OF POWER GENERATION UNIT

VCI	**2.5-3.6 V**
DDVDH	**4.7-6 V**
VCL	**-2.4 to -3 V**
VGH	**10-20 V**
VGL	**-5 to -15 V**

and optimal size design. The cost and the volume of conventional power generation units need to be reduced for high integration and compact size.

The proposed DSDO SC converter is presented in Fig. 4(b). Only two off-chip flying capacitors (C_1 and C_2) and four pin-outs ($C11P, C11N, C12P$ and $C12N$) are needed. The clock signals $\Phi1$–$\Phi4$ are non-overlap clocks used for power switches control. The proposed DSDO SC converter supplies two different polarity outputs at the same time without adding external off-chip components. Using the dual-side control, the output ripple can be reduced to meet the requirement of the TFT-LCD panel. Because of the lower effective switching frequency and higher output impedance, the driving capability of the proposed DSDO SC converter is lower than that implemented using an independent dual-side doubler and inverter at the same time.

III. OPERATION OF THE PROPOSED DSDO SC CONVERTER

A. Operation

The operation of the DSDO SC converter is shown in Fig. 5. The operation sequence refers to Phases 1, 2, 3, and 4. During Phase 1, ($\Phi1$ = high and $\Phi2 = \Phi3 = \Phi4$ = low), the transistors (P21 and N21) and (P23 and N22) are turned on to charge the flying capacitors, C_1 and C_2, respectively, as shown in Fig. 5(a).

During Phase 2 ($\Phi2$ = high and $\Phi1 = \Phi3 = \Phi4$ = low), the transistors, P22 and P25, are turned on to pump the stored charge from the capacitor C_1 to the output capacitor C_7 to generate the voltage, *DDVDH*. Meanwhile, the transistors, N25 and N26, are turned on to transfer the negative charge from the capacitor C_2 to the output capacitor C_8 to generate the negative voltage, *VCL*. During the Phase 2, both *DDVDH* and *VCL* receive energy from the converter. Fig. 5(b) illustrates the operation.

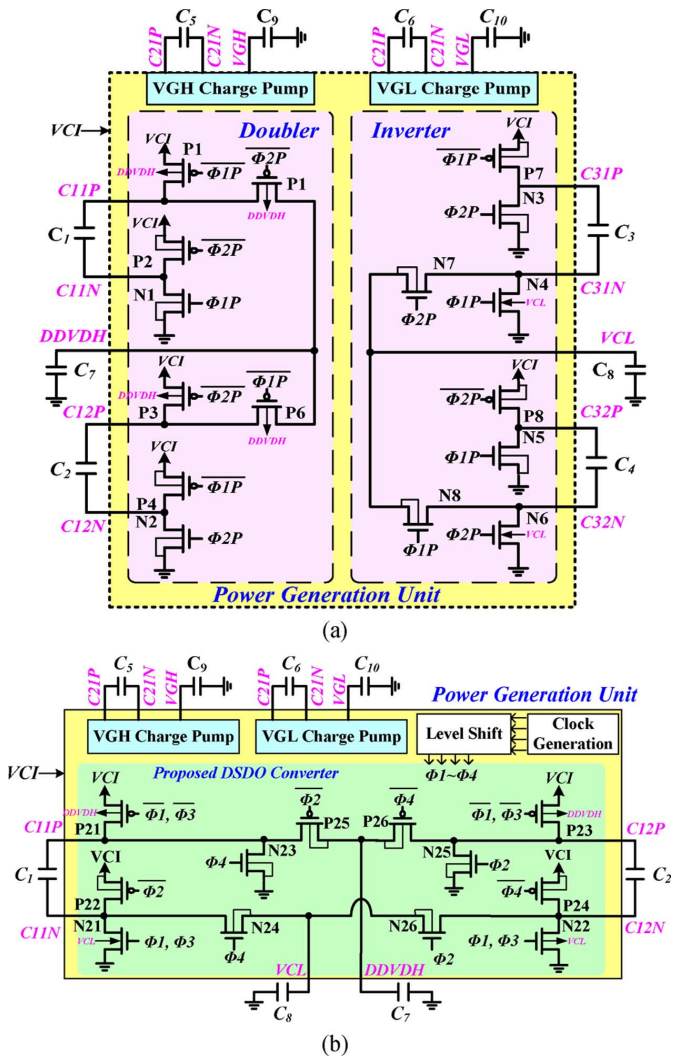

Fig. 4. (a) Dual-side doubler and inverter converters at transistor-level. (b) Proposed DSDO SC converter.

During Phase 3, the operation is the same as that in Phase 1, and the flying capacitor is recharged again. Transistors, N23 and N24, are turned on to transfer the negative charge from the capacitor C_1 to the output capacitor C_8 during Phase 4. Simultaneously, the transistors, P24 and P26, are turned on to pump the charge from the capacitor C_2 to the output capacitor C_7. After the above operation, both *DDVDH* and *VCL* receive energy from the converter. Using the dual-side control, the ripple can be effectively reduced to an acceptable range.

B. Output Voltage Drop

The voltage drop due to the power switches and the impedance of the flying capacitor are very important for the driving design of the TFT-LCD. Although the above operation is divided into four phases, it can be treated as one charge cycle and one discharge cycle from the viewpoint of output capacitor. For example, the *DDVDH* output capacitor receives energy during Phase 2 and Phase 4, and supplies current during Phase 1 and Phase 3. In a steady state, the energy of the charge cycle is equal to that of the discharge cycle.

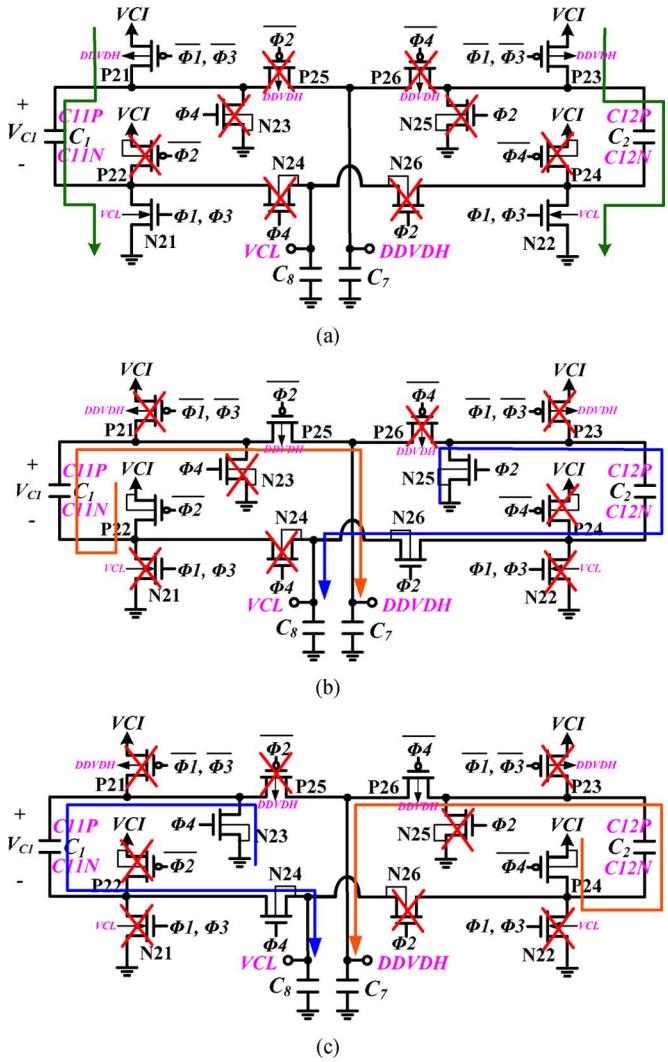

Fig. 5. (a) Operation of the proposed DSDO SC converter during phase 1 and phase 3. (b) Operation during phase 2. (c) Operation during phase 4.

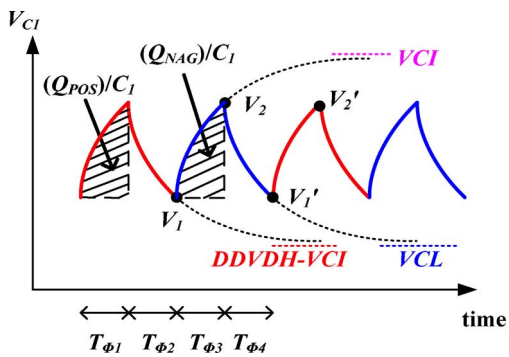

Fig. 6. Voltage waveform of flying capacitor C_1.

For simplification, the on-resistance of each power switches is assumed to be of the same value as $(R_{\rm SW})/2$. In addition, $C_1 = C_2 = C_{\rm FLY}$. If the load currents at the *DDVDH* output and the *VCL* output are defined as $I_{\rm LOAD(DDVDH)}$ and $I_{\rm LOAD(VCL)}$, respectively, the charge delivered to the *DDVDH* output from the flying capacitor C_1 during each switching period is $Q_{\rm POS}$, which is equal to $C_1 \times (V_2 - V_1)$, and the supplied charge during the period of $(T_{\Phi 1} + T_{\Phi 2})$ is equal to $(T_{\Phi 1} + T_{\Phi 2}) \times I_{\rm LOAD(DDVDH)}$. If the loading at each output is equivalent and the mismatch condition diminishes in a steady state, according to the theorem of charge conservation at the flying capacitance $C_1, V_1 = V_1'$ and $V_2 = V_2'$. Here, $V_1, V_1' V_2$ and V_2' are the voltage drops between the node $C11P$ and the node $C11N$ at the end of each period. In addition, $C_1 \times (V_2 - V_1)$ is equal to $(T_{\Phi 1} + T_{\Phi 2}) \times I_{\rm LOAD(DDVDH)}$, as expressed in (1). The charge and discharge curves can be expressed as (2) and (3) during the periods $T_{\Phi 1}$ and $T_{\Phi 2}$, respectively. The value of *DDVDH* is derived from (4) through (1)–(3) in a steady state. Fig. 6 shows the waveform of flying capacitor C_1.

$$\begin{aligned} Q_{\rm POS} &= C_1 * (V_2 - V_1) \\ &= I_{\rm LOAD(DDVDH)} * (T_{\Phi 1} + T_{\Phi 2}) \quad (1) \\ V_1 &= V_2 + (V_{\rm DDVDH} - VCI - V_2) * (1 - e^{-\beta}) \quad (2) \\ V_2 &= V_1 + ({\rm VCI} - V_1) * (1 - e^{-\beta}) \quad (3) \\ V_{\rm DDVDH} &= 2 * VCI - \frac{I_{\rm LOAD(DDCDH)}}{2 * F_{\rm OSC} * C_{\rm FLY}} \frac{1 + e^{-\beta}}{1 - e^{-\beta}} \quad (4) \end{aligned}$$

where

$$\beta = \frac{1}{4 * F_{\rm OSC} * R_{\rm SW} * C_{\rm FLY}} \quad (5)$$

and

$$F_{\rm OSC} = \frac{1}{T_{\Phi 1} + T_{\Phi 2} + T_{\Phi 3} + T_{\Phi 4}}. \quad (6)$$

The value β in (5) is the charge/discharge time constant. Similarly, the value of *VCL* can also be derived from (7), where $F_{\rm OSC}$ is the switching frequency:

$$V_{\rm VCL} = -{\rm VCI} + \frac{I_{\rm LOAD(VCL)}}{2 * F_{\rm OSC} * C_{\rm FLY}} \frac{1 + e^{-\beta}}{1 - e^{-\beta}}. \quad (7)$$

However, if the on-resistance of the power switches, $R_{\rm SW}$, is much larger than $1/2(F_{\rm OSC} \times C_{\rm FLY})$, the values of *DDVDH* and *VCL* can be simply derived as (8) and (9), respectively, when the average method is applied and the switching ripple is ignored:

$$\begin{aligned} V_{\rm DDVDH} &= 2 * {\rm VCI} - 4 * (I_{\rm LOAD(DDVDH)} * R_{\rm SW}) \quad (8) \\ V_{\rm VCL} &= -{\rm VCI} + 2 * (I_{\rm LOAD(VCL)} * R_{\rm SW}). \quad (9) \end{aligned}$$

The proper selection of $R_{\rm SW}$ can ensure that the DSDO SC converter in compact in size and has no serious performance degradation. In the current study, the maximum output impedance is 150 Ω. A proper value of $R_{\rm SW}$ can be selected to achieve a compact size. Designing the $R_{\rm SW}$ value to an order of milliohm at the cost of silicon area is unnecessary.

C. Output Ripple

The output ripple voltage, which may cause the water ripple on the panel, needs to be suppressed. As shown in Fig. 7(a) and (b), the voltage ripple of a single-side doubler and inverter is obtained similarly as in (10):

$$\begin{aligned} V_{\rm RIPPLE} &= V_{\rm RIPPPLE1} + V_{\rm RIPPLE2} \\ &= 2I_{\rm OUT} * {\rm ESR}_{\rm OUTPUT\_CAP} + \frac{I_{\rm OUT}}{2f_S * C_{\rm OUTPUT}}. \end{aligned} \quad (10)$$

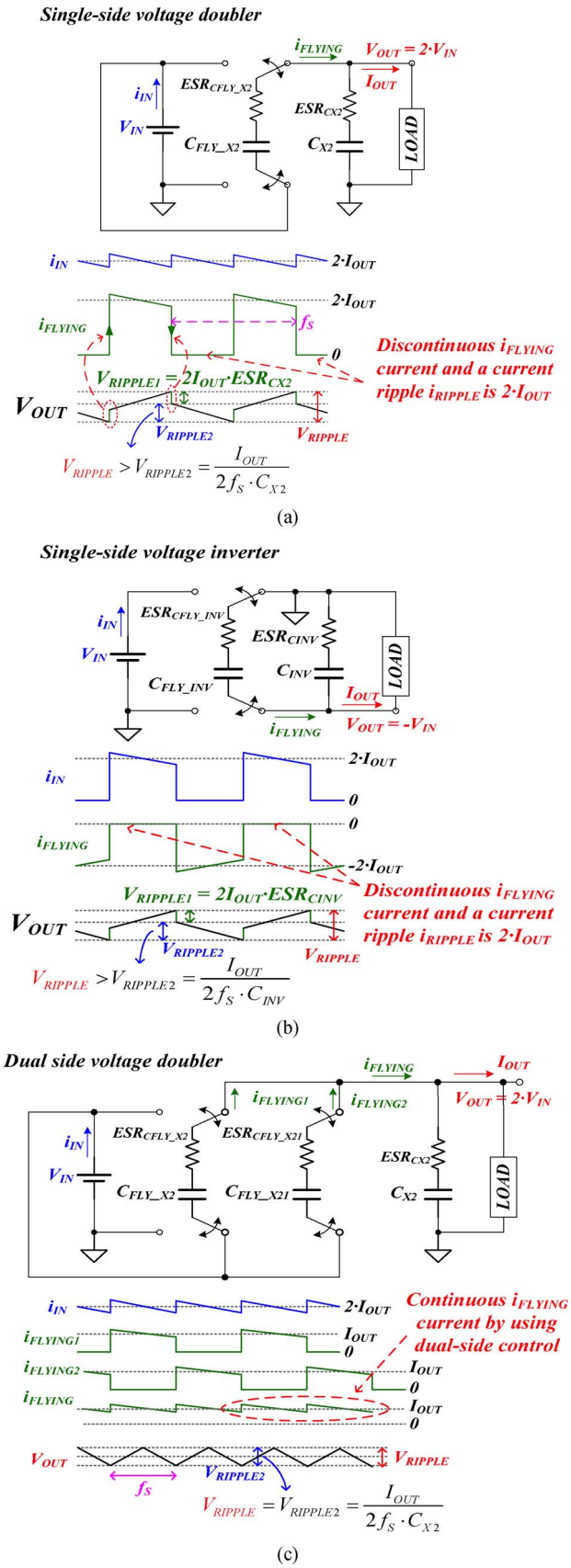

Fig. 7. (a) Waveforms of the single-side voltage doubler. (b) Waveforms of the single-side voltage inverter. (c) Waveforms of the dual-side voltage converter.

It contains the ripple V_{RIPPLE1} from the parasitic resistance between the output capacitor and the output node, and the ripple V_{RIPPLE2} from the charging/discharging of the output capacitor.

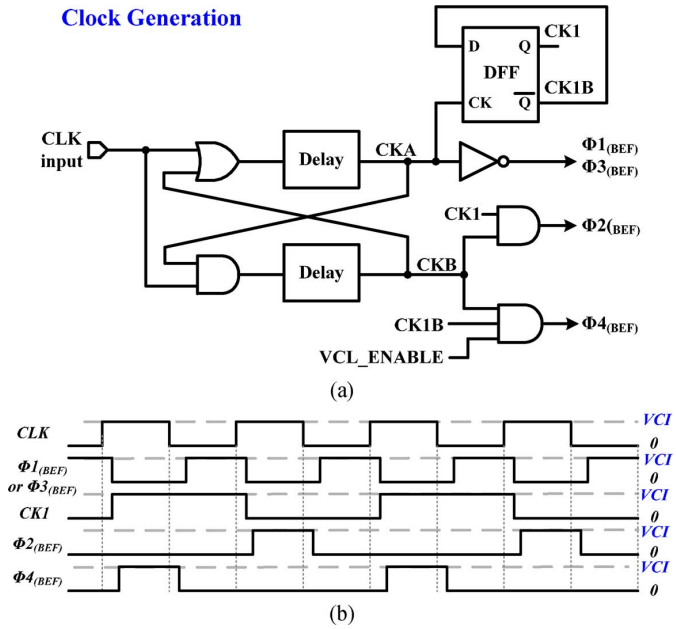

Fig. 8. (a) Clock generation block and start-up control. (b) Waveforms of the clock generation.

Here, f_S is the switching frequency, I_{OUT} is the load current, and $\mathrm{ESR}_{\mathrm{OUTPUT\_CAP}}$ is the summation of the equivalent series resistance (ESR) of the output capacitor, C_{OUTPUT}, and the parasitic resistance of the power path. When a dual-side control is applied, the V_{RIPPLE} voltage can be reduced to only V_{RIPPPLE2}, because the current ripple i_{FLYING} is continuous during the charge/discharge phase, unlike with the single-side voltage doubler and inverter. Fig. 7(c) shows the waveforms of the dual-side voltage doubler. The ripple voltage of a dual-side voltage doubler is approximated as in (11).

$$V_{\mathrm{RIPPLE\_dual}} = V_{\mathrm{RIPPLE2}} = \frac{I_{\mathrm{OUT}}}{2 f_S * C_{\mathrm{OUTPUT}}} \tag{11}$$

According to the DSDO operation, a dual-output can be achieved by just a single-side operation with two flying capacitors. However, the unacceptable ripple voltage is four times larger than that in a dual-side doubler. This is equivalent to one-fourth equivalent charge/discharge period compared with the dual-side voltage doubler and inverter when a single-side operation is applied in the proposed converter.

Using the time-multiplexing control, the DSDO can reduce the ripple voltage to half without adding any flying capacitors; the ripple voltage has the same value as a conventional single-side doubler or inverter as expressed in (10).

IV. Circuit Implementation

The four-phase clock generation is shown in Fig. 8(a) and the waveforms of each non-overlap clock signal from $\Phi 1_{(\mathrm{BEF})}$ to $\Phi 4_{(\mathrm{BEF})}$ are shown in Fig. 8(b). The key to generating those non-overlap clocks is that the *CK1* signal produced by the *CKA* signal after the frequency dividing operation through the use of a D-Flip-Flop (DFF). The start-up sequence is the output *DDVDH* voltage first, and the *VCL* voltage is permitted to output after the

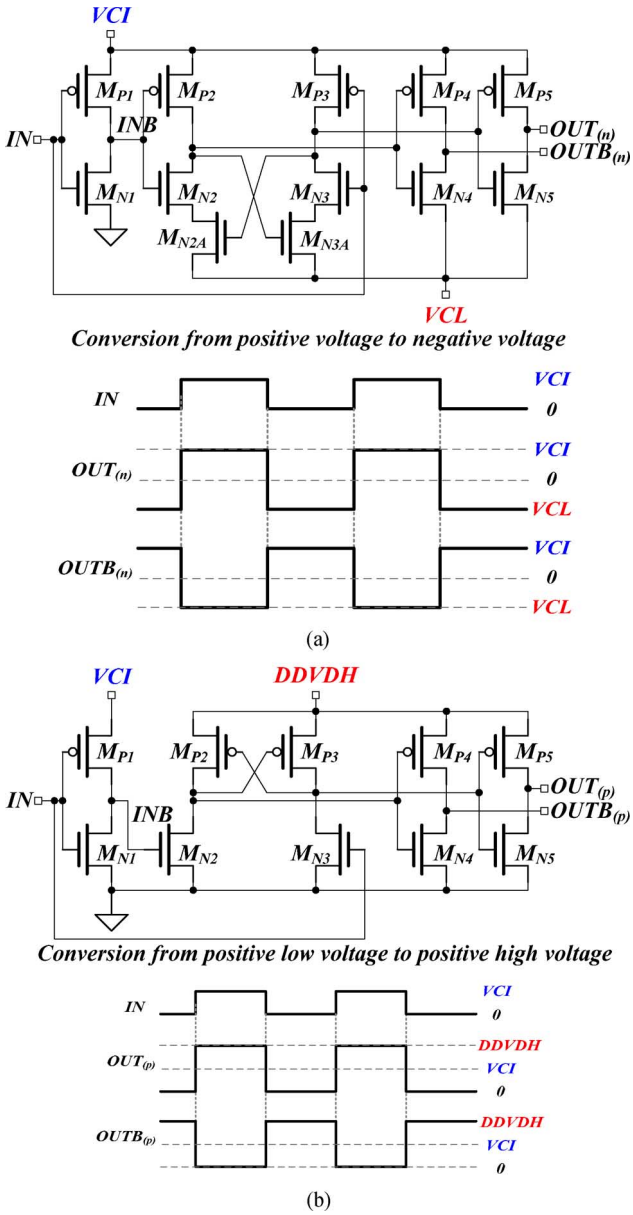

Fig. 9. Level shifters. (a) Conversion from positive voltage to negative voltage. (b) Conversion from positive low voltage to positive high voltage.

delay of 30 ms. A VCL_ENABLE control signal is used to turn on the clock $\Phi 4_{(\mathrm{BEF})}$ and permit the *VCL* to output.

Level shifter blocks are shown in Fig. 9. According to bipolar outputs topology, both level shifters that convert positive low voltage to positive high voltage and positive voltage to negative voltage are needed. The gate driver is shown in Fig. 10. According to the polarity of the output voltage, the power supply of the gate driver needs to be shifted to the same or the highest voltage level in the chip all the time. A simple inverter chain is applied as the gate driver.

V. Experimental Results

The proposed DSDO SC converter was fabricated in a 0.13 μm 1.8 V/5 V/32 V CMOS 2P5M process. The *DDVDH* output voltage was set to $2 \times$ VCI and the *VCL* output was set to $-$VCI. Fig. 11 shows the chip micrograph of a TFT-LCD driver with the layout of the proposed DSDO SC converter.

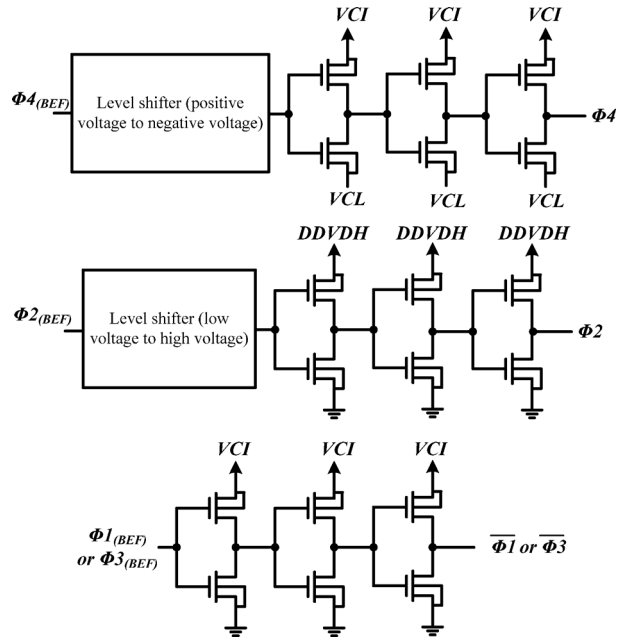

Fig. 10. Gate driver of the proposed converter.

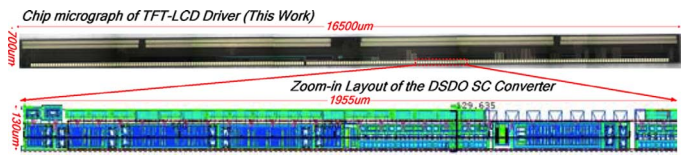

Fig. 11. Chip micrograph of a TFT-LCD driver and the zoom-in layout of the DSDO SC converter.

The total area of TFT-LCD was 16500×700 μm^2 and the die area of the proposed converter was 1955×130 μm^2. In the current study, the on resistance of each power switches were designed to approximately 15 Ω for a compact-size design. The clock frequency was 20 kHz and the flying capacitors and the output capacitors were all equal to 1 uF with ESR was 50 mΩ.

Fig. 12(a) shows the simulation results of the proposed DSDO converter. Fig. 12(b) shows the zoom-in of the *DDVDH* and the *VCL* in Fig. 12 (a). The load current of each output is 2 mA and the *VCI* input voltage is approximately 2.5 V. The simulation results show that the dual outputs are supplied at the same time with 2 mA load at each output.

The measurement result of the proposed DSDO converter is shown in Figs. 13 and 14. Fig. 13 is the start-up waveform of the proposed converter. The positive output of the *DDVDH* is 4.81 V and the negative output of the *VCL* is -2.31 V, whereas the *VCI* is approximately 2.5 V. The ripple voltages of the *DDVDH* and *VCL* output are 95 mV and 85 mV, respectively when the load current is 2 mA. Table II shows the specifications of the proposed converter. Switching frequency of 20 kHz was selected because the impendence of the flying capacitance is approximately 8 Ω, which is the same order of the power switch.

Higher switching frequency is better for lower output voltage ripple. However, if a large parasitic resistance at the power path exists between the output node and the output capacitance, the output ripple is slightly related to the ripple that is contributed by the charging/discharging output capacitor. That is, the value

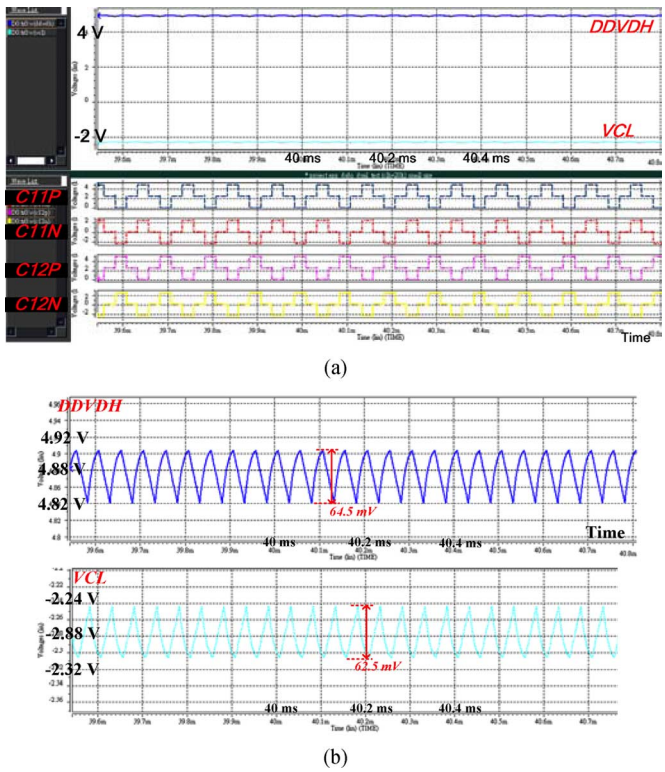

Fig. 12. (a) Simulation waveform of the proposed DSDO converter. (b) Zoom-in of the *DDVDH* and *VCL*.

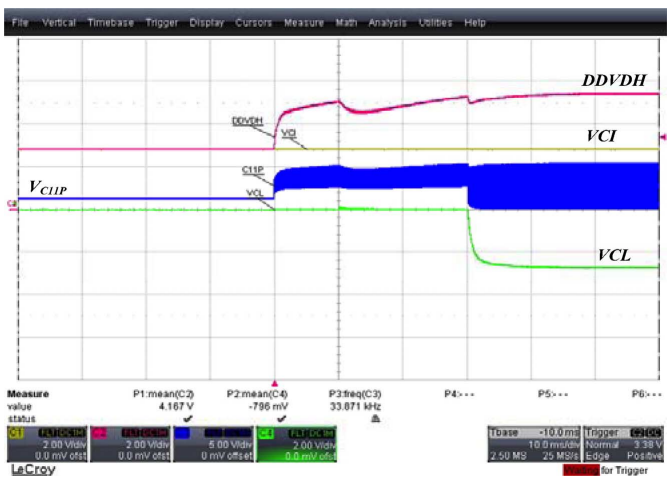

Fig. 13. Measured start-up waveforms of the proposed DSDO converter.

of V_{RIPPLE1} is much larger than that of V_{RIPPLE2} in (10). The ripple reduction is small even if the switching frequency continues to increase. On the other hand, the output voltage drop can be decreased if the resistance of the power switches/power path is decreased or the switching frequency is increased.

Table III shows the comparison between the proposed converter and the conventional design with two independent channels (doubler and inverter). The measured voltage ripples of the proposed and conventional design are 95 mV and 58 mV, respectively. Fig. 15 shows the measurement efficiency of the proposed converter when the switching frequency of the proposed converter is 20 kHz.

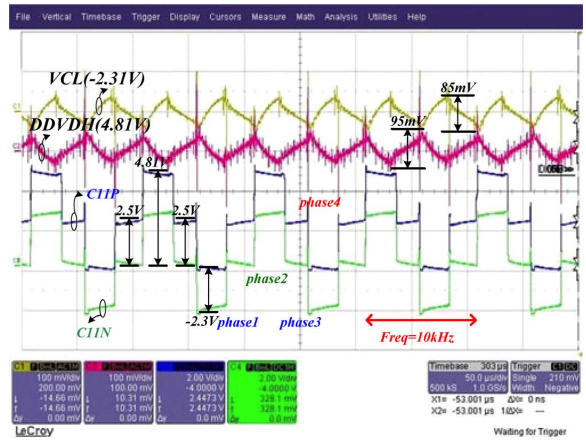

Fig. 14. Measured output waveforms of the DSDO converter.

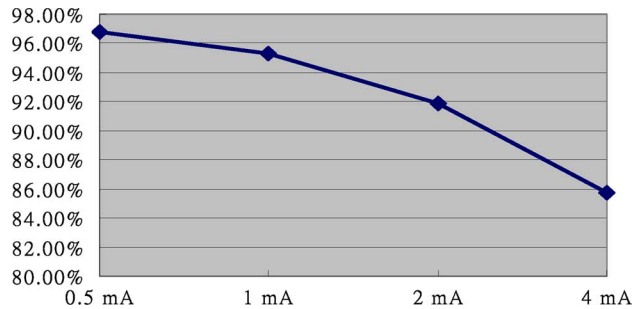

Fig. 15. Measurement efficiency of the DSDO converter when the switching frequency is 20 kHz.

TABLE II
SPECIFICATIONS OF THE PROPOSED CONVERTER

	Proposed converter
Input voltage (*VCI*)	2.5 V
Output voltage (Dual)	4.81 V and -2.31V
Flying capacitors (C_1/C_2)	1 μF /1 μF
Output capacitors (C_7/C_8)	1 μF /1 μF
Switching Frequency	20 kHz
Ripple voltage (*DDVDH* /*VCL*)	95 mV/85 mV
Load current (*DDVDH* /*VCL*)	2 mA/2 mA
Switching frequency	20 kHz
ESR of output capacitor	50 mΩ

TABLE III
COMPARISON BETWEEN THE PROPOSED AND THE CONVENTIONAL TOPOLOGIES

Topology	Proposed	Conventional dual-side converter
Flying capacitor	2	4
Output capacitor	2	2
Pin-outs	6	10
Power switches	12	16
Chip area (normalization)	77%	100%
Ripple voltage	95 mV	58mV

VI. CONCLUSION

In this paper, the DSDO SC converter is proposed to successfully provide a simple topology to reduce the number of power switches, and thereby decreasing the number of flying capacitors (from four to two) and the pin-outs (from eight to four). The DSDO topology can effectively integrate two independent

channels (doubler and inverter) in one channel, and has the advantages of having a compact size and a small layout of PCB. The test chip uses 0.13 μm CMOS technology. The results of the experimental demonstrate that the combination doubler and the inverter can correctly drive the TFT-LCD panel with a chip reduction of 23%.

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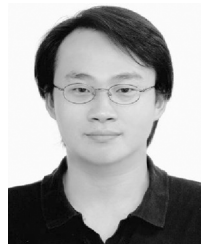

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